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Horizontally-split-drain MAGFET – a highly sensitive magnetic field sensor

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Abstract. We propose a novel magnetic field sensitive semiconductor device, viz., Horizontally-Split-Drain Magnetic-Field Sensitive Field-Effect Transistor (HSDMAGFET) which can be used to measure or detect steady or variable magnetic fields. Operating principle of the transistor is based on one of the galvanomagnetic phenomena and a Gradual Channel Detachment Effect (GCDE) and is very similar to that of Popovic and Baltes's SDMAGFET. The predicted absolute sensitivity of the new sensor can reach as high value as 1000 V/T. Furthermore, due to its original structure, the spatial resolution of the new MAGFET is very high which makes this device especially useful in reading magnetically encoded data or magnetic pattern recognition.

Key words: magnetic field-effect transistor (MAGFET), magnetic field measurement, magnetic pattern recognition.

1. Introduction

Density of magnetically written information on disk storage devices, magnetic field patterns, transaction cards, etc. is getting higher and higher therefore development of magnetic field sensors and systems reading magnetically encoded data requires continued improvement in MAGFET performance [1-3]. Spatial and magnetic resolutions of the MAGFET are parameters of crucial importance [1,2].

To meet requirements for the key parameters of the magnetotransistor, a conception of a novel semiconductor device, viz., Horizontally-Split-Drain Magnetic-Field Sensitive Field-Effect Transistor (HSDMAGFET) is proposed in this work. In the next section, the structure and operating principle of the new magnetotransistor are described. In Section 3, magnetic sensitivity of the new transistor is assessed, respectively, from first principles, and by comparing with experimental results for the SDMAGFET.

2. The new MAGFET and its operation

Figure 1 depicts the basic structure of the Horizontally-Split-Drain Magnetic-Field Sensitive Field-Effect Transistor with n-type channel [4,5]. The new device is a two-drain and two-gate enhancement-mode MOS-type transistor in which the drain regions are placed one under the other and isolated from each other with horizontal insulator layer. Positive voltages of the gates G_1 and G_2, V_{GS1} and V_{GS2}, induce an n-type channel in the transistor, and positive drain voltages, V_{DS1} and V_{DS2}, cause electrons to flow from the source S to the drains D_1 and D_2, which is displayed in Fig. 1. This source current splitting between

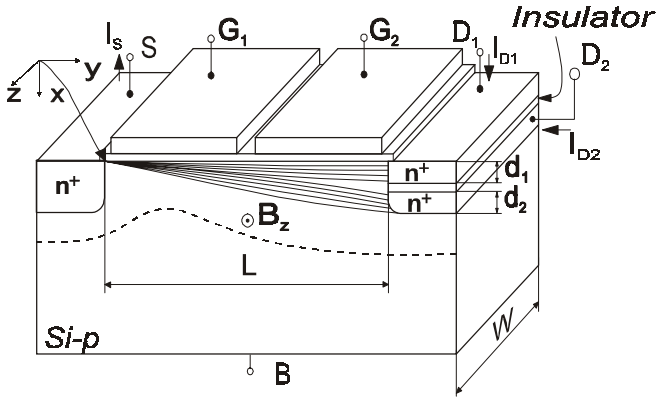

Fig. 1. Basic structure of the new transistor after Refs. 4 and 5

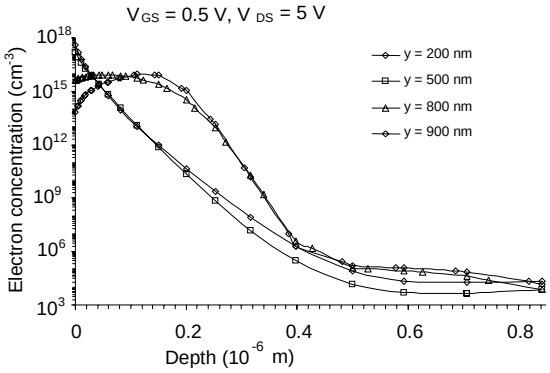

Fig. 2. Simulated electron concentration profiles for various cross sections of the transistor channel of an n-MOSFET with the channel length L = 1 μm after Ref. 8; effective gate-source voltage V_{GS} - VT = 0.5V, V_{DS} = 5V, and y is the distance from the transistor source

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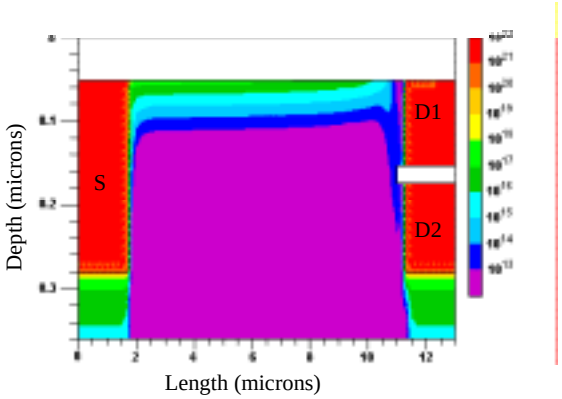
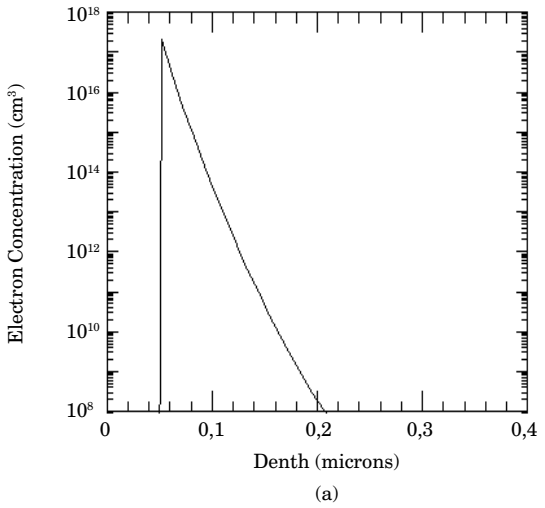


Fig. 3. Dimensions of a simulated HSDMAGFET and calculated electron concentration distribution (in cm-3) in the transistor; $V_{DS1}=V_{DS2}=9.2$ V, $V_{GS}=1$ V, Bz=0, $t_i=20$ nm



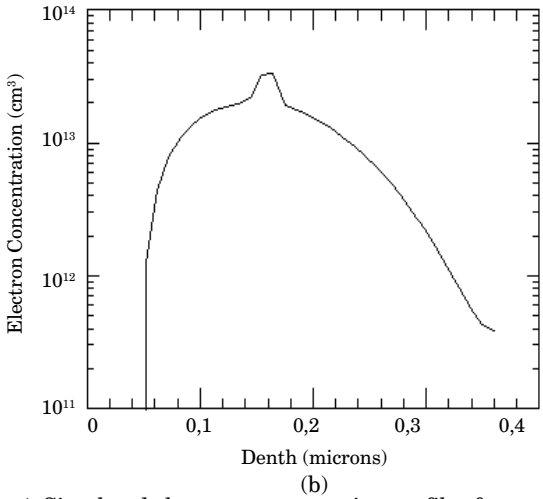


Fig. 4. Simulated electron concentration profiles for two cross sections of the transistor channel of the HSDMAGFET of Fig. 3 made at abscissas $X_1=4$ μm (a), and $X_2=11$ μm (b)

electron streams flowing in the drains D_1 and D_2 is a consequence of a Gradual Channel Detachment Effect (GCDE). This phenomenon is to gradually thicken and move away the electron stream from the semiconductor surface as values of the drain voltages are increasing. The effect stems from self-diffusion of moveable carriers and two-dimensional electric field distribution in the transistor channel and was demonstrated for the MOSFET, for example, in [6-8]. The GCDE is illustrated in Fig. 1 and clearly presented for MOS transistor in Fig. 2 where electron concentration profiles for various cross sections of the transistor channel are depicted.

We have simulated an HSDMAGFET structure with the use of PISCES IIB program. A two-dimensional picture

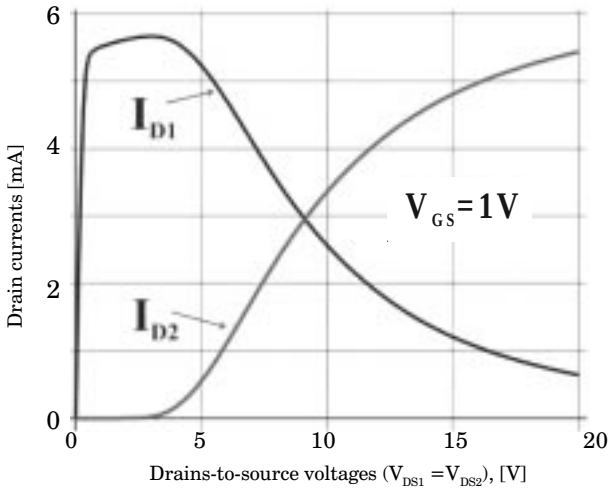


Fig. 5. Simulated output characteristics for the HSDMAGFET of Fig. 3; the channel width W=10 μm, $V_{DS1}=V_{DS2}$

of the electron distribution in a simulated HSDMAGFET with one gate is presented in Fig. 3 where dimensions of the device are also displayed. The results are obtained under the following biasing conditions: drain-to-source voltages $V_{DS1}=V_{DS2}=9.2$ V, gate-to-source voltage $V_{GS}=1$ V, an external magnetic induction z-component $B_z=0$ T; thickness of the splitting insulator layer t_i is equal to 20 nm. Fig. 4 depicts more precisely simulated electron concentration profiles for two cross sections made at abscissas $X_1=4$ µm and $X_2=11$ µm of the transistor channel of the HSDMAGFET of Fig. 2. For that specific bias of 9.2V at both drains, the drain currents I_{D1} and I_{D2} are equal to each other, which can be observed on simulated current-voltage output characteristics demonstrated in Fig. 5.

Referring to Figs. 1 to 4, we can assume the charge carriers in the channel to flow in the form of thin current layers. Each of the layers is becoming thicker and thicker as the distance from the source is increasing while Gauss's law and current continuity equation are fulfilled within each layer. Thicknesses of the drain regions, d_1 and d_2, and the splitting insulator layer are as small as possible.

The basic equation for terminal currents of the device is as follows:

$$I_S = I_{D1} + I_{D2} \tag{1}$$

where I_S is the current injected into the channel through the source potential barrier, and I_{D1} and I_{D2} are currents flowing into, respectively, the drain D_1 and D_2. Potential of

the gate G_1 with respect to the source, V_{GS1}, determines the magnitude of I_S, and potential of the gate G_2, V_{GS2}, has an impact on the ratio of current partition I_{D1}/I_{D2}. Thus the balance between drain currents can be achieved by changing the voltage V_{GS2}.

If we place the HSDMAFET in an external magnetic field, the Lorentz force acts on electrons moving in the channel [3]. Consequently, a magnetic induction z-component B_z, see Fig. 1, causes the current layers in the channel region to deflect up or down, depending on the direction of B_z. This leads to an asymmetry in the terminal drain currents, which is a measure of the magnetic field strength. An imbalance between the drain currents, defined as I_{D1}-I_{D2}, is a function $f(...)$ of the transistor channel width W, channel length L, biasing voltages V_{GS1}, V_{GS2}, V_{DS1}, V_{DS2}, and magnetic induction $\boldsymbol{B}$, which can be expressed as

$$I_{D1} - I_{D2} = f(W, L, V_{GS1}, V_{GS2}, V_{DS1}, V_{DS2}, B). \quad (2)$$

As to the structure and principle of operation, the new MAGFET is very similar to Popovic and Baltes's SDMAGFET, [3,9], which is presented in Fig. 6. The

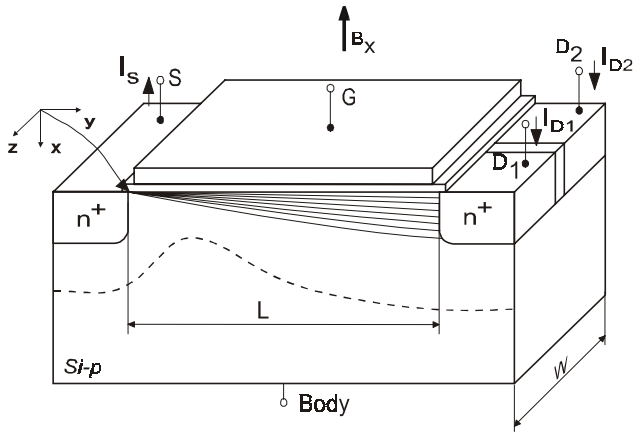


Fig. 6. SDMAGFET after Refs. 3 and 9

SDMAGFET also comprises two drains, but they are placed side-by-side and vertically isolated, cf. Figs. 1 and 6. In Popovic and Baltes's sensor, the x-component B_x of a magnetic field deflects current lines in the plane y-z and finally an imbalance between I_{D1} and I_{D2} occurs, so the SDMAGFET is a sensor of the perpendicular-to-gate component of a magnetic field, and its spatial resolution is determined by the channel width W and length L.

3. Sensitivity of the HSDMAGFET

Magnetic sensitivity of the new transistor is assessed in two ways in this section. First, the sensitivity is predicted from first principles, and finally by relating it to experimental results for the SDMAGFET available in the literature.

The relative magnetic sensitivity S[%/T] of the split-drain devices at small magnetic induction is defined as follows [3]:

$$S = \left| I_S^{-1} \frac{\partial (I_{D1} - I_{D2})}{\partial B_z} \right|_{B_z = 0} \quad (3)$$

i.e., the partial derivative of the relative current imbalance with respect to the magnetic induction, taken at zero induction, which, for small B_z, can be replaced by [10,11]

$$S = \left| \frac{I_{D1} - I_{D2}}{(I_{D1} + I_{D2}) B_z} \right| . \quad (4)$$

Due to horizontally split drains, manufacturing the new HSDMAGFET needs a modified CMOS technology that is not available to us therefore we are not able to present experimental results of the new device's magnetic sensitivity. However, the sensitivity can be predicted theoretically.

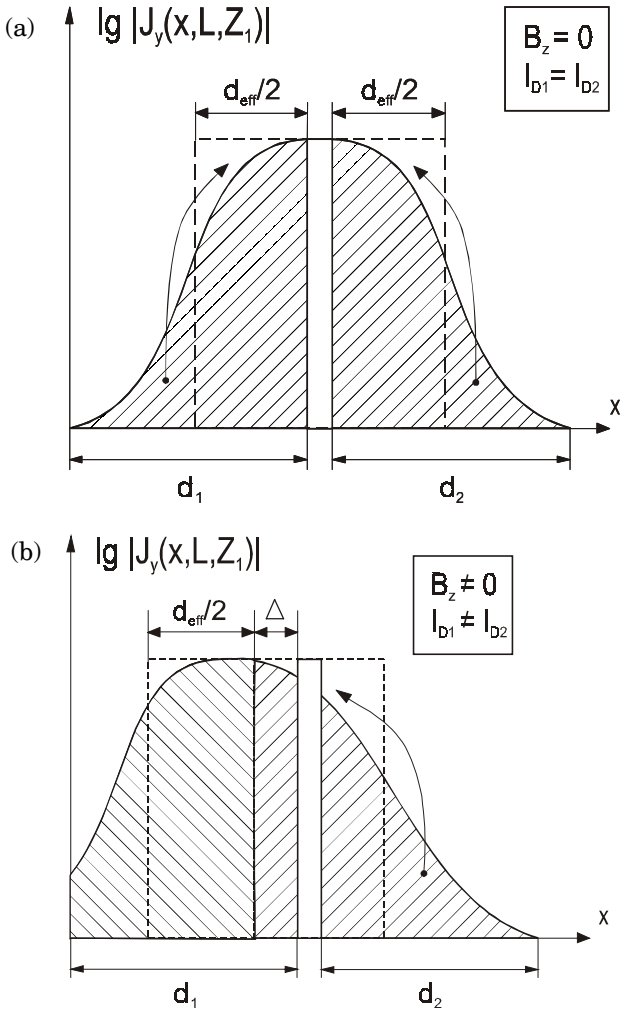


Fig. 7. Illustration of current density distribution in a near-drain cross section of the channel of a hypothetical HSDMAGFET: (a) $B_z = 0$, (b) $B_z \neq 0$. Arrows show a method of calculating the effective near-drain channel thickness d_{eff}, where d_1 and d_2 are, respectively, the thickness of the drain D_1 and drain D_2

Let us consider an idealized picture of the current density y-component distribution $J_y(x,L,z)$ in near-drain cross section of an HSDMAGFET displayed in Fig. 7a. In general, channel direct current I_{ch} through an arbitrary surface A perpendicular to the drawing plane in the transistor channel region can be expressed by

$$I_{ch} = -q \iint_A n(x,z)\, \boldsymbol{v}(x,z) \cdot d\mathbf{A} \quad (5)$$

where, q is electronic charge (magnitude), $n(x,z)$ – electron density distribution in xz-plane (see Figs. 1, 2, and 4, and $\boldsymbol{v}(x,z)$ – the velocity vector of electrons in the channel. Particularly, referring to Fig. 7a, and assuming that the velocity y-component $v_y(x,L)$ of current carriers (electrons) in appropriate regions of the plane $y=L$ is independent of x and equal to v_y, we can write formulas for drain currents in the form

$$I_{D1} = q v_y W \int_0^{d_1} n(x,L)\, dx, \quad (6)$$

$$I_{D2} = q v_y W \int_{d_1+t_i}^{d_1+t_i+d_2} n(x,L)\, dx. \quad (7)$$

where t_i stands for thickness of the insulator separating the drains.

Introducing an average current density in the neighborhood of the splitting insulator, J_i (see Fig. 7a),

$$J_i = \left(J_y(d_1,L) + J_y(d_1+t_i,L) \right)/2, \quad (8)$$

we can define an effective channel thickness at the HSDMAGFET drain, d_{eff}, as

$$d_{eff} = \left(\int_0^{d_1} J_y(x,L)\, dx + \int_{d_1+t_i}^{d_1+t_i+d_2} J_y(x,L)\, dx \right) / J_i. \quad (9)$$

Assuming again that velocity y-component $v_y(x,L)$ of current carriers in appropriate regions of the plane $y=L$ is independent of x, equations (8) and (9) can be rewritten in the form:

$$J_i = q v_y \left(n(d_1,L) + n(d_1+t_i,L) \right)/2, \quad (10)$$

$$d_{eff} = \frac{2\left(\int_0^{d_1} n(x,L)\, dx + \int_{d_1+t_i}^{d_1+t_i+d_2} n(x,L)\, dx \right)}{n(d_1,L)+n(d_1+t_i,L)}. \quad (11)$$

As an external magnetic field acts on the HSDMAGFET, the Lorentz force causes the current layers in the channel region to deflect up or down (Fig. 1), depending on the direction of B_z. Introducing after [11] an effective current line deflection Δ, measured at the MAGFET drains (see Fig. 7b), and defined as [11]

$$\Delta = L \mu_n |B_z| \quad (12)$$

where μ_n is the electron mobility in the channel, we can calculate the magnitude of the drain currents imbalance, $\Delta I = I_{D1} - I_{D2}$, produced by magnetic field z-component B_z, viz.,

$$|\Delta I| = |I_{D1} - I_{D2}| = \frac{2L\mu_n B_z}{d_{eff}} \left(I_{D1} + I_{D2} \right). \quad (13)$$

Inserting (13) into (4) and making use of (10) and (11) lead to the relative sensitivity S[%/T] of the HSDMAGFET

$$S = \frac{2\,\mu_n\, L}{d_{eff}}, \quad (14)$$

or, alternatively,

$$S = \frac{\mu_n L \left[n(d_1,L) + n(d_1+t_i,L) \right]}{\int_0^{d_1} n(x,L)\, dx + \int_{d_1+t_i}^{d_1+t_i+d_2} n(x,L)\, dx}. \quad (15)$$

The mobility μ_n in (12)-(15) is an electric-field-dependent parameter and its dependence on the longitudinal electric field component in the channel can be described as follows [12]:

$$\mu_n = \frac{\mu_{n0}}{\left[1 + \left(\frac{E_0}{E_C} \right)^b \right]^{\frac{1}{b}}}, \qquad \left(E_0 = \frac{V_{DS}}{L} \right) \quad (16)$$

where μ_{n0}, E_C, and b are, respectively, low-field mobility, characteristic electric field, and a parameter ($1 \le b \le 5$).

From (15) it follows, that the relative sensitivity S, reaches its maximum value when the current carrier concentration at the cross-section plane for $y=L$ gets its maximum in the neighborhood of the splitting insulator. Strictly speaking, S reaches its maximum if the drain currents are balanced, $I_{D1} = I_{D2}$. This result converges well with the experimental results obtained for standard SDMAGFETs [10,11].

Based on the theoretical analysis outlined in this section, and also on the numerical simulation results (Fig. 4b) we can estimate the expected sensitivity of the proposed HSDMAGFET. Taking some additional realistic data: μ_{n0}=1000 cm²/(Vs), E_C=10³ V/cm, b=2, L=10 μm, V_{DS}=9.2 V, the calculated sensitivity value can reach 100%/T, that is 50 times more than the experimental value 2-3 %/T obtained for the standard SDMAGFET [3,9-11].

The relative sensitivity S of the HSDMAGFET can also be related to that of known SDMAGFETs. Namely, based on experimental results for a complementary SDMAGFET pair given in Popovic and Baltes's work [9], we are able to estimate the predicted magnetic sensitivity of the device. In order for the estimation to be fairly reliable, the following assumptions are taken: both dimensions and working configuration of two complementary HSDMAGFETs are the same as those of the two complementary SDMAGFETs of work [9], current deflecting in the transistor channels is an isotropic phenomenon, and a parameter Δ, see Fig. 7b, keeps the same value in either case (as it was mentioned above, Δ is an effective current line deflection measured at the MAGFET drains and produced by variation in appropriate magnetic field components, respectively, ΔB_z for the HSDMAGFET and ΔB_x for the SDMAGFET). Taking the above assumptions and results of [9] into account, referring to Figs. 1 to 4, 6 and 7, making a linear analysis, and neglecting some calculations, it can be shown that an arbitrarily defined sensitivity of MAGFET sensors to magnetic field satisfies an equation

$$S_{HSD} = \left(W / d_{eff}\right) S_{SD} \tag{17}$$

where d_{eff} is an effective channel thickness defined by (11), see also Fig. 7, S_{HSD} and S_{SD} are sensitivities defined in the same way but relating, respectively, to the HSDMAGFET sensor and the corresponding SDMAGFET sensor. Obviously, this is true if the z-component B_z of the magnetic field, see Fig. 1, is uniformly distributed in the transistor channel.

Thus, an arbitrarily defined sensitivity of a HSDMAGFET sensor can be hundreds or thousands of times higher than that of the SDMAGFET sensor working in the same configuration because the factor W/d_{eff} in (17) can take such a great value. For instance, an absolute measured sensitivity of the complementary SDMAGFET pair reported in [9] was of 1.2 V/T therefore the sensitivity of the analogous complementary HSDMAGFET pair can be of the order of 1000 V/T and more if the channel width W equals to 200 μm and d_{eff} is of 0.2 μm, cf. Fig. 2 and 7 as well as [6,7]. Such a high sensitivity of the new sensor seems to be possible to obtain due to the fact that the current line deflection Δleads to much bigger change in the current imbalance (2) in the case of the HSDMAGFET than that of the SDMAGFET.

Owing to its high geometrical resolution determined by W and d_{eff}, the HSDMAGFET can be very suitable for the purpose of reading high-density magnetically encoded data.

4. Conclusions

Due to its high magnetic sensitivity and high spatial resolution, the conception of the new HSDMAGFET structure proposed in this paper is very promising for applications in magnetometry and reading magnetically encoded data of high density. However, developing a modification of standard CMOS technology is crucial to manufacture various magnetic field sensors based on the new HSDMAGFET.

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