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Programmable Feedforward Linearized CMOS OTA for Fully-Differential Continuous-Time Filter Design

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Abstract. In this paper, a feedforward linearization method for programmable CMOS Transconductance Operational Amplifier (OTA) is described. The proposed circuit technique is developed using simple source-coupled differential pair transconductors, a feedback-loop amplifier for self-adjusting transcoductance (g_m) and a linear reference resistor (R). As a result, an efficient linearization of a transfer characteristic of the OTA is obtained. SPICE simulations show that for 0.35 μm AMS CMOS process with a single +3 V power supply, total harmonic distortion (THD) at 1 V_{pp} and temperature range from –30°C to +90°C is less than –49.3 dB in comparison to –35.8 dB without linearization. Moreover the input voltage range of linear operation is increased. Power consumption of the linearized OTA circuit is 0.86 mW. Finally, the OTA is used to design a third-order elliptic low-pass filter in high-frequency range. The cutoff frequency of the Operational Transconductance Amplifier-Capacitor (OTA-C) filter is tunable in the range of 322.6 kHz – 10 MHz using the feedforward linearized OTAs with the digitally programmable current mirrors.

Index terms: CMOS OTA, linearized OTA, feedforward linearization, fully-differential OTA.

1. INTRODUCTION

Programmable, highly linear CMOS Operational Transconductance Amplifiers (OTAs) with wide dynamic range and excellent high frequency performance are useful building blocks for the design of many analog circuits and mixed signal systems. Applications such as high-frequency continuous-time (CT) analog OTA-C filters provide solutions for various signal processing tasks [1]-[11]. In recent years also the Field Programmable Analog Arrays

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(FPAAs) based on the tunable (programmable) OTAs and integrating capacitors (C) have been developed sucessfully to built reconfigurable hardware platforms (e.g., for CT analog filter rapid-prototyping) [15]-[21].

One of the simplest and most widely used MOS transconductors for high-frequency operations (e.g., active filters) is a source-coupled differential pair. However, it can be observed that while offering low noise, its large signal characteristics are extremally nonlinear. Therefore, the dynamic range and the efficiency of the differential pair using MOS transistors are limited [5], [12]-[14]. A number of techniques for improving the linear properties of CMOS transconductance elements based on the source-coupled differentional pairs have been proposed [22]-[38]. These techniques employ MOS transistors operating both in saturation in triode regions. Methods such as adapting biasing (e.g., [27]), source degeneration (e.g., [30]), and current differencing/current addition (e.g., [26]) lead to effective linearization. However, the performance improvement is obtained at the expense of the power consumption increase, reduced transcondutance factor as well as the power factor defined here as the maximum linear output current divided by the total bias current [5].

It is well known that an application of the feedforward technique enables us to improve performance of many analog signal processing circuits. For example, this technique is widely used to reduce nonlinear distortion in amplifiers [40]-[48]. Moreover, it is successfully employed to frequency compensation of operational amplifiers (Opamps) and OTAs [49]-[53].

In this work, a novel highly linear programmable CMOS operational transconductance amplifier is proposed. The OTA circuit developed here uses, as basic building blocks, simple differentional-pair transconductors, a reference resistor and digitally programmable current mirrors. The linearization follows by employing an active-error feedforward scheme. The error signal is generated using an additional differential-pair transconductor and a resistor

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which is assumed to be linear. This resistor can be an external one or it can be implemented as a monolitic element, e.g., using a highly-resistive poly layer.

The proposed technique gives effective linearization and it is free of drawbacks mentioned in the previous paragraph. In particular, it allows us to implement the OTA circuit which has extremely low power consumption, extended linear range operation as well as good transconductance programming (tuning) capability. Moreover, the feedforward linearized OTA offers excellent high frequency performance, which makes the developed circuit suitable for OTA-C filter applications at higher frequencies.

The paper is organized as follows. In Section 2, a description of the proposed feedforward linearization method is presented. In Section 3, the design of the complete circuit of the programmable linearized differential CMOS OTA and its parameter comparison is performed. Section 4 presents the third-order OTA-C elliptic filter design with the simulation results. Section 5 concludes the paper.

2. DESCRIPTION OF FEEDFORWARD LINEARIZATION METHOD

For the purpose of the subsequent analysis, the nonlinear transfer characteristic of the transconductance elements will be characterized using power series expansion. Let i_G denotes the output current of the transconductor in Fig. 1, and its power series dependence is given by

$$i_G = G\left[\left(v_{ID}\right)\right] = \sum_{n=1}^{\infty} g_n v_{ID}^n(t) \tag{1}$$

where v_{ID} is the differential input voltage and the coefficients g_n are defined as

$$g_n = \frac{1}{n!}\frac{d^n G\left[\left(v_{ID}\right)\right]}{dv_{ID}^n}\bigg|_{v_{ID}=0} \tag{2}$$

By definition, first-order coefficient g_1 of (2) is the transconductance g_m of the amplifier.

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Consider a simple CMOS differential pair transconductor shown in Fig. 2. Using the square-law MOS transistor modeling, its normalized transfer characteristic around zero can be written as follows [12]

$$i(x) = 2I_S x\sqrt{1-x^2} \tag{3}$$

where x is a normalized input voltage defined as

$$x = \frac{v_{id}}{2(V_{GS} - V_T)} \tag{4}$$

with V_{GS} being the quiescent value of the gate-source voltage of both M1 and M2, V_T being their threshold voltage, and I_S being the biasing current of the differential pair. Actually, formula (3) is valid for $|x| \le \sqrt{2}/2$. For larger x, the transfer characteristic saturates. Then, the corresponding power series expansion of (3) is given by

$$i(x) = 2I_S\left(x - \frac{1}{2}x^3 - \frac{1}{8}x^5 - \frac{1}{16}x^7 - \frac{5}{128}x^9 \cdots\right) \tag{5}$$

Fig. 3 shows the circuit concept of transconductance amplifier linearization based on active-error feedforward method [49], [53]. Amplifiers $G^{<1>}$, $G^{<2>}$ and $G^{<3>}$, modeled as in Fig. 1, are assumed to be identical. Their transfer characteristics are described by the power series expansion (1). Additionally, it is assumed that the resistor R in Fig. 3 is perfectly linear and its resistance is equal to $1/g_m$. In practice, e.g., in integrated circuits implementations, some technologies offer high resistive poly which can be used to realize resistor R. Alternatively, such a resistor can be treated as an external (discrete) element.

Using (1), the output current of the overall circuit in Fig. 3 can be written as follows

$$i_{OUT}(t) = \sum_{n=1}^{\infty} g_n v_{IN}^n(t) + \sum_{n=1}^{\infty} g_n \left[v_{IN}(t) - v_R(t)\right]^n \tag{6}$$

where

$$v_R(t) = g_1^{-1} \sum_{n=1}^{\infty} g_n v_{IN}^n(t) \tag{7}$$

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This means that the voltage at the input of the transconductor $G^{<3>}$ (working as an error amplifier) is expressed as

$$v_{IN}(t) - v_R(t) = v_{IN}(t) - g_1^{-1}\sum_{n=1}^{\infty} g_n v_{IN}^n(t) = -g_1^{-1}\sum_{n=2}^{\infty} g_n v_{IN}^n(t) \tag{8}$$

Hence, we obtain

$$i_{OUT}(t) = \sum_{n=1}^{\infty} g_n v_{IN}^n(t) + \sum_{n=1}^{\infty} g_n \left[-g_1^{-1}\sum g_k v_{IN}^k(t) \right]^n \tag{9}$$

Normally, the value of $[v_{IN}(t) - v_R(t)]$ is much smaller than the values of the input voltages of transconductors $G^{<1>}$ and $G^{<2>}$, which allows us to neglect the higher order terms in the output current of $G^{<3>}$. This leads to the following approximation

$$i_{OUT}(t) \cong \sum_{n=1}^{\infty} g_n v_{IN}^n(t) - \sum_{n=2}^{\infty} g_n v_{IN}^n(t) = g_1 v_{IN}(t) \tag{10}$$

which shows the perfect cancellation of nonlinearities of the overall transconductance amplifier in Fig. 3.

One can calculate THD for both original and linearized circuit assuming the transfer characteristic (3) for all transconductors (in particular, we no longer neglect higher order terms in the output current of $G^{<3>}$ as in (10)). The results of numerical calculations are presented in Figs. 4, 5 and 6. Fig. 4 shows theoretical THD characteristics for the considered circuits. Figs. 5 and 6 show theoretical transfer and transconductance characteristics, respectively. It is worth noting that using the active-error feedforward technique one can obtain not only significant reduction of THD but also considerable increase of linear range of operation (recall that the transfer characteristic for differential pair transconductor saturates for $x \approx 0.7$; for linearized circuit it happens for $x \approx 1.2$).

The proposed OTA (Fig. 3) has a higher linearity range, but due to increased current consumption and devices count noise is also increased compared to the simple differential pair. If we denote v^2_{Gnoise} as total input referred power spectral density noise of a single

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transconductor G from Fig. 3, then the input referred three-block feedforward transconductance amplifier power spectral density noise is equal to:

$$v_{noise}^2 = 3v_{Gnoise}^2 + \frac{4kTR}{(g_m R)^2}\Big|_{R=1/g_m} = 3v_{Gnoise}^2 + 4kTR \tag{11}$$

where $4kTR$ is the thermal noise of resistor R, k is the Boltzman's constant, T is the absolute temperature, and R is resistance of resistor which is due to nonlinearity cancellation condition also equal to $1/G=1/g_m$.

According to [5], input referred noise of a single MOS pair assuming medium range of frequency can be approximated by:

$$v_{pair\_noise}^2 = \frac{16}{3} kT \frac{1}{g_m} \tag{12}$$

Using (11) and (12), the noise increase of the linearized transconductance amplifier can be approximated as

$$\frac{v_{noise}^2}{v_{pair\_noise}^2} = \frac{15}{4} = 3.75 \tag{13}$$

Note that equation (12) is an underestimated approximation of real MOS pair (without taking into account current mirrors noise and body noise), which means that the noise increase given by (13) is overestimated. The actual noise of the amplifier is also slightly smaller because the contribution of other devices (not only the differential pair) to the total noise makes the thermal noise of resistor R less visible for linearized amplifier. In particular, if the resistor noise is assumed to be negligibly small comparison to the noise of a single amplifier G then value of noise ratio would be equal 3. Thus, (13) describes a worst case scenario. The degradation of dynamic range from below for the actual amplifier will be then somewhere between 4.76dB to 5.74dB.

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The main advantage of proposed amplifier is its increased linearity comparing to the simple reference CMOS differential pair. As it is shown at the Figs. 4 and 5 input voltage for –40dB THD is 0.86 while for simple pair is 0.27. Thus, dynamic range increases by 10.1dB and thus total dynamic range of the linearized amplifier is at least 4.32dB better than for the amplifier based on simple MOS pair. Linearized amplifier works also better for higher signals and due to this is a good alternative for today needs with continuous decrease of power supply voltages and problems with high amplitude signals processing.

Another general problem concerning CMOS amplifiers is the input referred offset voltage. Since proposed amplifier does not use current differentiation, its performance is not degraded comparing to the simple MOS pair. Moreover, improved linearity makes it usable even at the presence of relatively high mismatches and offsets. Of course, for instrumentation amplifier applications offset have to be cancelled using specialized sub-circuits which are not considered here [55].

3. PROGRAMMABLE DIFFERENTIAL PAIR CMOS OTA

Fig. 7 shows a programmable fully differential OTA implementation using the active-error feedforward concept discussed in Section 2. The OTA is realized using AMS 0.35μm technology with highly-resistive POLY option. MOS dimensions and resistances are summarized at the end of the section. Resistors were designed using high resistive POLY layer. Note that presented circuit is a differential-input two-output OTA, which follows from the fact that such a circuit configuration is more suitable for filtering applications. Thus, there it is a slight modification of the basic concept presented in Fig. 3. In Fig. 7(a) input stage is presented, which realizes idea from Fig. 3. The transistors M1, M2 and M7, M8 form classical source-coupled differential pairs with current sink realized by transistor M14. Actually, the pair M1 and M2 implements two-output counterpart of transconductor $G^{<1>}$ in Fig. 3. Transistors M7, M8 implement the counterpart of transconductor $G^{<2>}$ loaded by resistor

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$1/2g_m$. Differential pairs M3, M4 and M5, M6 with current sinks M13 and M15, respectively, realize error amplifiers corresponding to $G^{<3>}$ in Fig. 3. The transistors M9-M12 and M16 work in saturation and implement simple current-mirror circuits. Difference of currents i_A and i_B is the output current from the input stage and is equivalent to i_{OUT} from Fig. 3. Two capacitors C_C realize phase compensation at higher frequencies, however, we omit the detailed description of the compensation mechanism here.

Output stage of the OTA is presented in Fig. 7(b) and forms a programmable current mirror array with common mode feedback circuitry (CMFB), which is similar to stage presented in [19]. Note that alternatively, programmable current mirror array can be replaced by programmable current divider [56], [57]. CMFB block works in classical two MOS pair configuration. Programmable current mirror works in cascade configuration with extra MOS devices M4a, M2a, M4b, M2b which improve high frequency response of the mirror [39]. Devices Mo1 and Mo2 are output transistors of the cascaded current mirror, while devices denoted as Ms act as switches that connect biasing voltage V_{BIAS1} to the upper output transistors. Voltages $V_{SP\_4} - V_{SP\_0}$ control actual multiplication ratio of the output stage. If voltage V_{SP_X} is set to V_{DD} then V_{BIAS1} is present on the gate of corresponding device Mo1 and this output current flows to the output of OTA. Otherwise, i.e., if V_{SP_X} is set to 0, the corresponding output current is equal zero as well. There are two MOS switches connected to all upper transistors Mo1. Second switch reloads C_{GS} capacitance to zero and, due to this, control voltages V_{SN_X} should be always inverted versions of corresponding V_{SP_X} voltages. Output stage indexed 0 consists of one set of Mo1 and Mo2 devices. The number of output sets in each subsequent stage is doubled in comparison to the previous stage. There are five output stages indexed from 0 to 4 altogether, and due to this one can obtain 31 different final transconductances of the OTA.

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Unfortunately, in order to obtain a linear correspondence between the output current of the input stage presented at Fig. 7(a) and the input differential voltage, precise resistors of values equal to $1/(2g_{m1,2})$ are required, where $g_{m1,2}$ is transconductance of the differential pairs M1, M2 and M7, M8. Otherwise, high nonlinearities may occur and linearization schema explained in Section 2 will not work correctly. Therefore, a special circuit performing self-adjustment of the differential MOS pairs is introduced and presented in Fig. 7(c). This gm-adjusting block is based on master-slave concept usually applied in automatic circuit parameters control e.g. in intergraded filters design [1-3]. Thus, circuit changes constant polarizing current flowing to the MOS pair Mt1, Mt2 (which should be identical as stabilized MOS pairs M1, M2 and M7, M8). The change of this current causes the corresponding change of transconductance of the MOS pair. Devices Mt6-Mt9 form simple operational amplifier, which works in a closed loop. The result is that the voltage across resistance R_1 and the sum of voltages on R_2 and R_3 are stabilized to the same values. Assuming this equality as well as the MOS pair Mt1-Mt2 working in the linear region, the final transconductance of this differential stage is equal to:

$$g_{m1,2} \approx g_1 = \frac{R_2 + R_3}{R_1 R_2} = \frac{1}{R} \tag{14}$$

If the same polarizing current is then flown to another identical MOS pair, that pair will have the same transconductance. This is realized by the current mirror with devices Mt5 and M13-M16 from the input stage in Fig. 7(a). Any change in power supply value, temperature, or any change in run to run deviation in the realized resistors can be now easily compensated. This requires extra devices and power but this circuit can be implemented only once for all OTAs in the whole integrated circuit. To obtain the desired value of final transconductance $g_m=1/R$, the resistances of R_1, R_2 and R_3 should be chosen so that:

$$\frac{R_2 + R_3}{R_1 R_2} = \frac{1}{R} \tag{15}$$

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Simulation results of proposed OTA (Fig. 7) are presented in the Table 1 and in Figs. 8 and 9. The results are presented for both versions of OTA, i.e., with and without the g_m-adjusting circuitry. It is shown that both OTA circuits work well but only the amplifier with the g_m-adjusting circuitry gives high linearity of the transfer characteristics in case the temperature change occurs. THD of the OTA with g_m-adjusting for 0.5 V amplitude sine of 10 kHz, and the temperature change from -30 °C to 90 °C is lower than -49.3 dB while for the OTA without g_m-adjusting THD degrades to -35.8 dB. MOS dimensions (W/L) and resistors of our OTA circuit are given in Table 2.

Table 1. Feedforward linearized OTA parameter comparison (V_{DD} = 3V and I_{BIAS} =15 μA)

Parameter	**OTA without g_m-adjusting**	**OTA with g_m-adjusting**
Maximum transconductance g_m [μS]	64.5	64.5
Minimum transconductance [μS]	2.081	2.081
Power dissipation [mW]	0.76	0.86
Open loop voltage gain [dB]	78	77.5
3dB bandwidth [kHz]	58.5	62.8
Differential input capacitance [fF]	16.4	16.4
Differential output capacitance [fF]	22.1	22.1
CMRR for 3% deviation in V_T and 0.5% in K of MOS devices, worst case for 100 Monte Carlo analyzes [dB]	26.5	*
PSRR for 3% deviation in V_T and 0.5% in K of MOS devices, worst case for 100 Monte Carlo analyzes [dB]	25.6	*
THD @ input sine with amplitude of 0.5V and at temperatures of –30°C, 30°C and 90°C, respectively [dB]	-35.8 -53.3 -40.2	-49.3 -64.0 -57.6

* The simulation of CMRR and PSRR parameters with the g_m-adjustment circuit turned on was not feasible; however, the properly designed adjustment circuit does not change the values of CMRR and PSRR factors significantly when compared to the version of OTA without g_m-adjustment circuit.

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Table 2. MOS dimensions (W/L) and resistors for the OTA circuit of Fig. 7

Stage	Device	Value
OTA input stage	M1-M8	4µm/1µm
	M9-M11	10µm/1µm
	M12, M13, M15	30µm/1µm
	M14	60µm/1µm
	M16	15µm/1µm
	Resistors	20.4kΩ
	C_C	10fF
Programmable output stage with the CMFB circuit	M21-M24	70µm/2µm
	M25, M26	4µm/1µm
	M27-M30	2µm/1µm
	M31, M32	10µm/1µm
	Ma1, Mb1	6µm/1µm
	Ma2, Mb2	4µm/1µm
	Ma3, Mb3	9µm/9µm
	Ma4, Mb4	12µm/0.5µm
	Mo1	4µm/1µm
	Mo2	1µm/2µm
	Ms	0.7µm/0.35µm
Self-adjusting circuitry for g_m	Mt1-Mt4	4µm/1µm
	Mt5	30µm/1µm
	Mt6, Mt7	4µm/1µm
	Mt8, Mt9	15µm/1µm
	Mt10-Mt12	2µm/2µm
	R_1	59.5kΩ
	R_2	2.88kΩ
	R_3	11.52kΩ

4. PROGRAMMABLE OTA-C FILTER DESIGN

Consider an elliptic filter prototype with rejection in stop band equal to 53.2 dB [54]. De-normalization was carried out for $g_m = 64.5$ µS and cut-off frequency of 10 MHz. Final filter schematic is presented in Fig. 10. After subtracting OTA's input and output capacitances, filter capacitor values are following: $C_1 = 2.21$ pF, $C_2 = 2.16$ pF, $C_3 = 2.25$ pF and $C_4 = 49.9$ fF. As OTAs, amplifiers with and without g_m-tuning were used. Simulation results are summarized in the Table 3. Frequency responses of the filter are presented in the Fig. 11. It can be observed that the filter works well and the zero rejection is higher than 66 dB. Frequency response complies with the theory for frequencies up to 100 MHz. Filter with the g_m-tuning circuitry presents much lower THD distortion if temperature changes occur as shown in Table 3.

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Table 3. Performance parameters of the filter in Fig. 10

Parameter	Filter built using OTAs without g_m-adjusting	Filter built using OTAs with g_m-adjusting
Maximal cut-off frequency [MHz]	10	10
Minimal cut-off frequency [kHz]	322.6	322.6
Power dissipation [mW]	5.05	5.28
THD @ sine with 0.5 V of amplitude and frequency 10 kHz for temperatures equal to –30 °C, 30 °C and 90 °C, respectively [dB]	-39.8 -53.4 -41.8	-47.1 -63.9 -61.8

5. CONCLUSIONS

A programmable fully differential feedforward CMOS OTA with excellent linearity for high-frequency applications is described and its performance simulated. The circuit is developed using a three-differential-pair transconductor operating in feedforward configuration together with a two-resistor load for introducing the error signal in the active feedforward path. Also a self-adjusting g_m circuitry operatig in the feedback-loop is developed. The wide range g_m-programmability is obtained using a programmable current mirror array technique. As an application example, a third-order elliptic OTA-C low-pass filter with cutoff frequency up to 10 MHz is implemented in the AMS 0.35 μm CMOS process.

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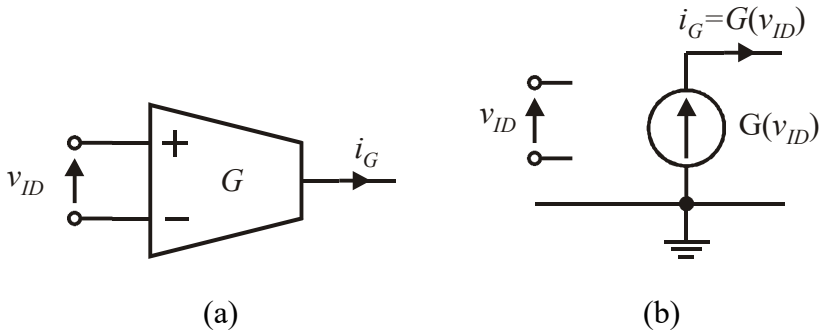

Fig. 1. Nonlinear model of transconductance element: (a) Symbolic representation. (b) Nonlinear incremental equivalent circuit.

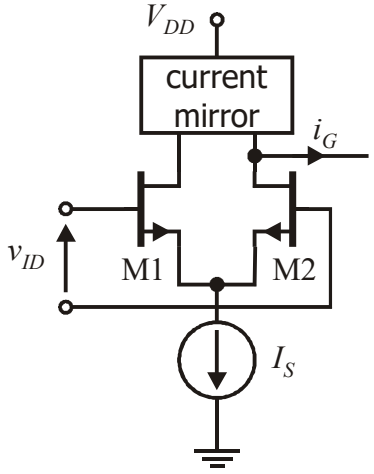

Fig. 2. Simple CMOS differential pair transconductor.

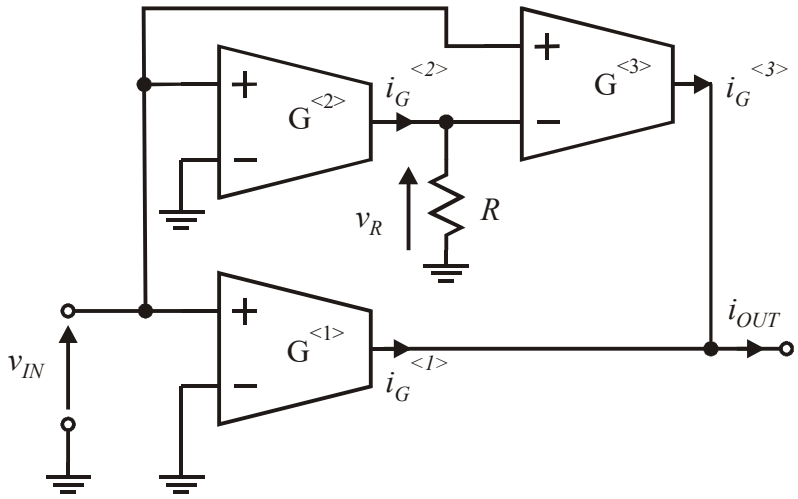

Fig. 3. Three-block feedforward transconductance amplifier [49], [52].

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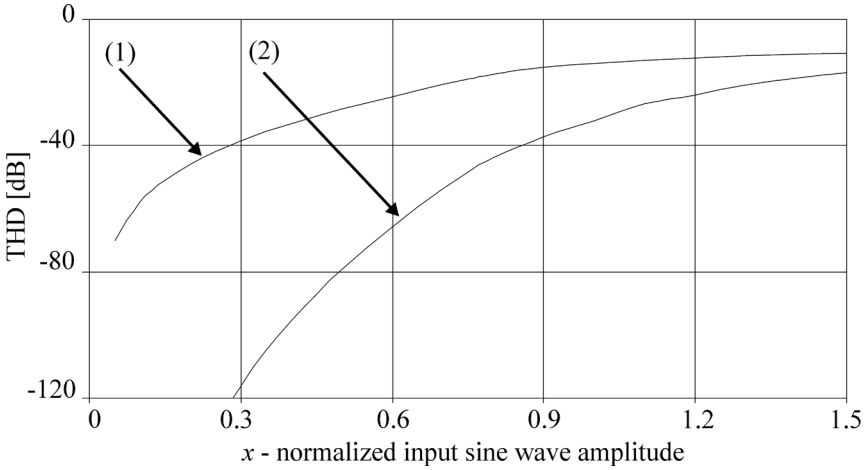

Fig. 4. Theoretical THD characteristics for (1) simple differential-pair transconductor, and (2) linearized transconductor.

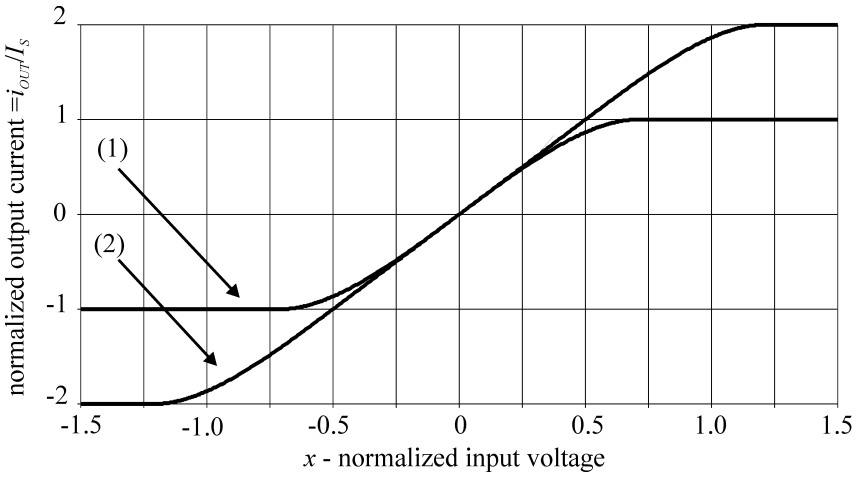

Fig. 5. Theoretical transfer characteristics for (1) simple differential-pair transconductor, and (2) and linearized transconductor (2).

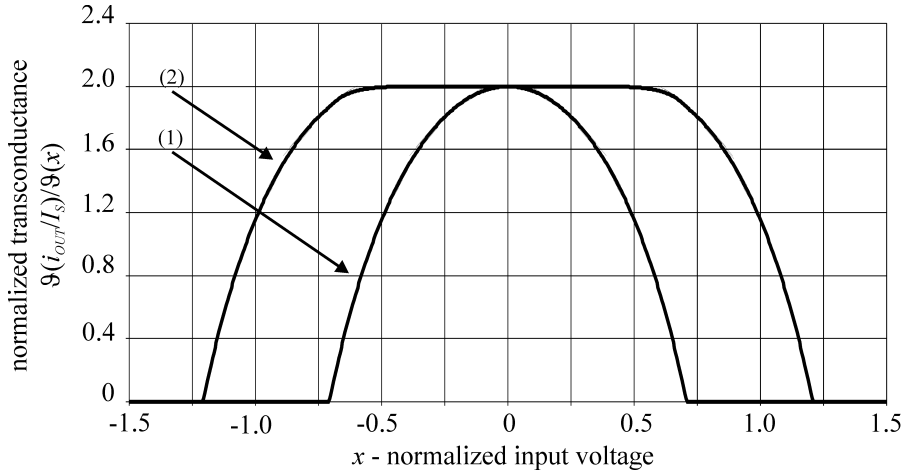

Fig. 6. Theoretical transconductance characteristics for (1) simple differential-pair transconductor, and (2) linearized transconductor.

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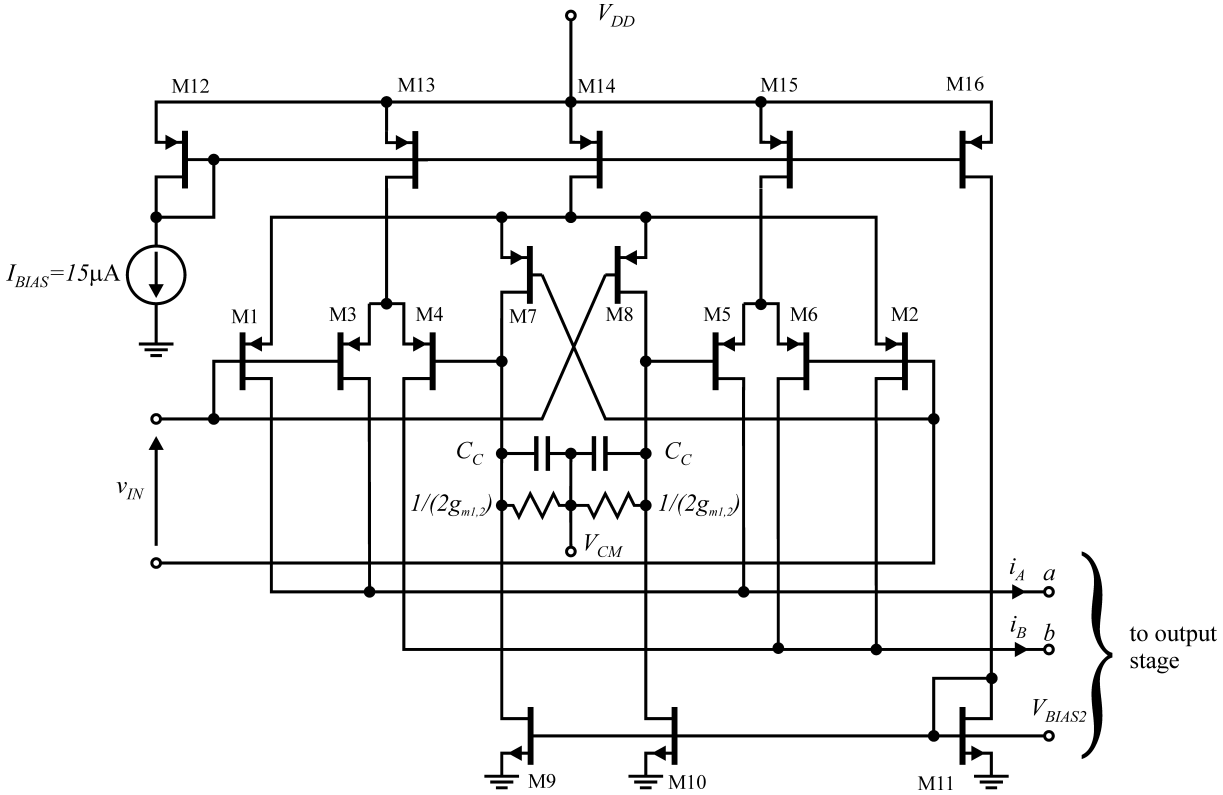

(a)

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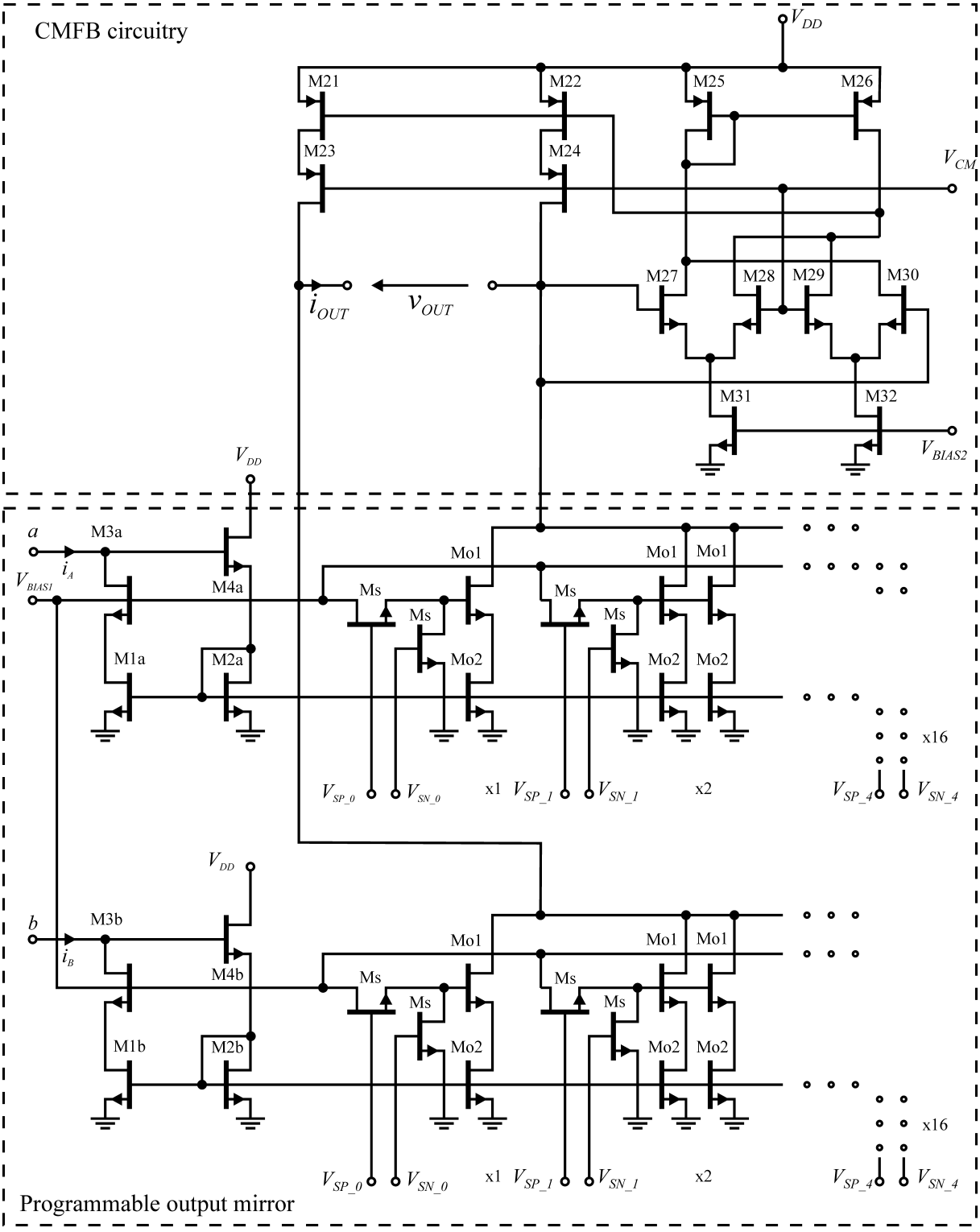

(b)

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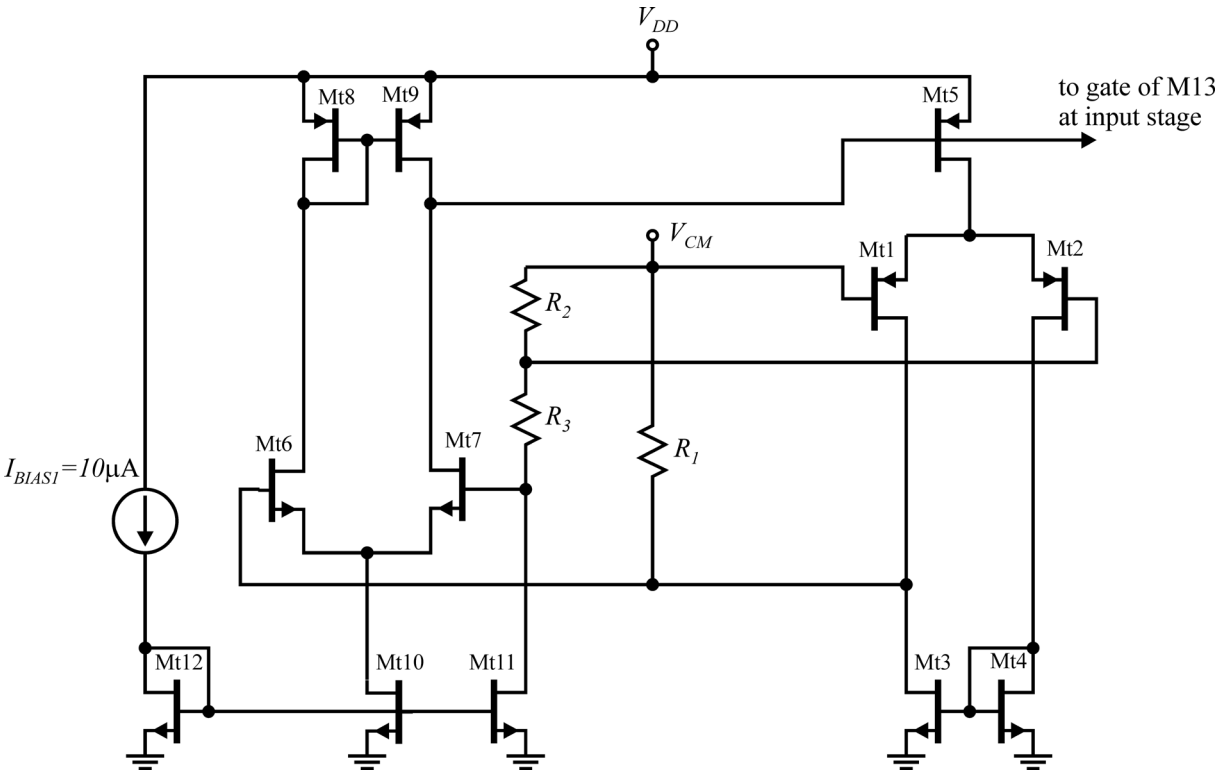

(c)

Fig. 7. Complete diagram of the linearized CMOS OTA: (a) Feedforward fully differential input stage. (b) Programmable output stage with the CMFB circuit, (c) Self-adjusting g_m circuitry.

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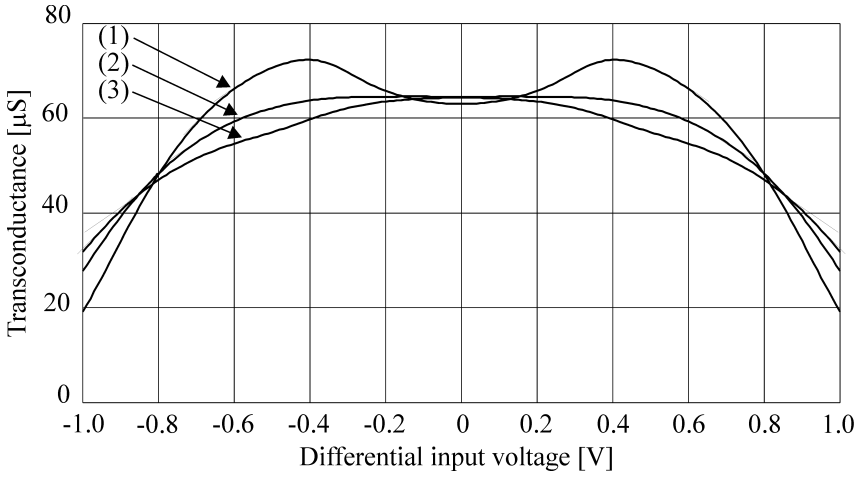
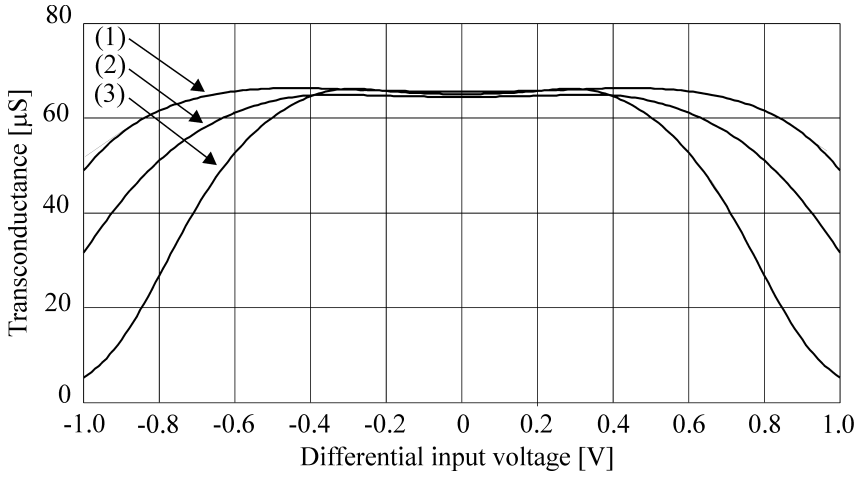
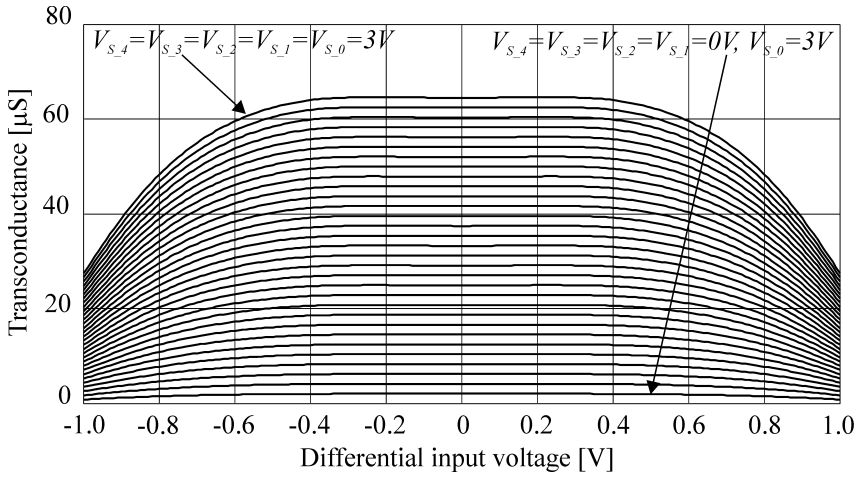


(a)



(b)



(c)

Fig. 8. Simulated transconductance of OTA from Fig. 7: (a) without g_m-adjusting, and (b) with g_m- adjusting for three operating temperatures: (1) -30 °C, (2) +30 °C, and (3) +90 °C, and (c) change of transconductance g_m parameters by digital programming word at lines [V_{S_4} : V_{S_0}].

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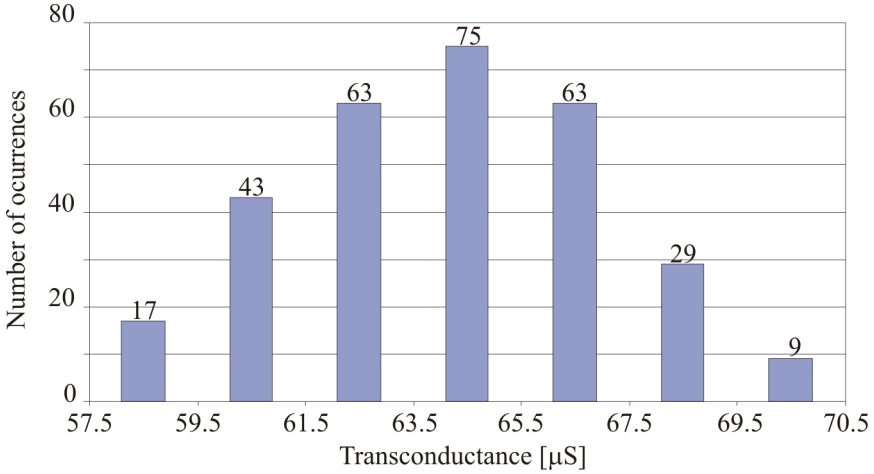

Fig. 9. Monte-Calro simulation results for transconductance of OTA from Fig. 7 without g_m-adjusting circuitry for 3% deviations in threshold voltage and 0.5% in transconductance parameter of MOS devices. Results for 300 random simulations.

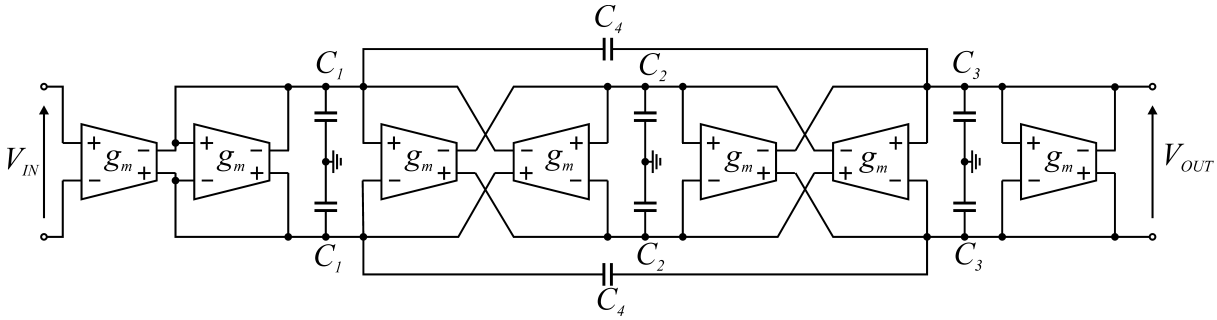

Fig. 10. Third-order low-pass OTA-C elliptic filter.

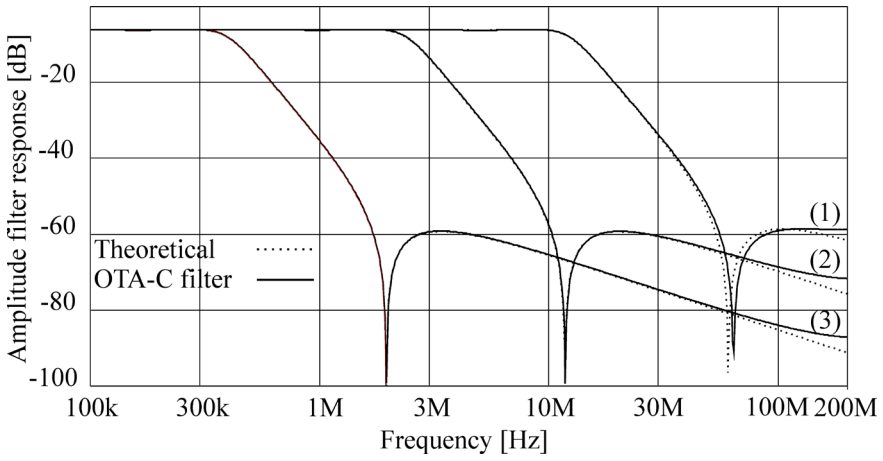

Fig. 11. Simulated response of OTA-C filter from Fig. 10 for OTA transconductance g_m = 64.5 µS (1), g_m = 12.48 µS (2) and for g_m = 2.081 µS (3). Change of transconductance was carried out through voltages applied to V_{SP_4} - V_{SP_0} and V_{SN_4} - V_{SN_0}.

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