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Ultra-low power analogue CMOS vision chip

Abstract. *The paper presents a project and results of testing of an analogue vision chip, which performs low-level convolutional image processing algorithms in real time. The prototype chip is implemented in 0.35 μm CMOS technology, contains SIMD matrix of analogue processing elements of size 64 x 64. The dimensions of the matrix topography is 2.2 mm x 2.2 mm, giving the density of 877 processors per mm^2. Matrix dissipates less than 0.4 mW of power under 3.3 V supply and at the speed of image processing 100 frames/s.*

Streszczenie. *W artykule przedstawiono projekt i wyniki badań scalonego analogowego układu wizyjnego, który wykonuje splotowe niskopoziomowe algorytmy przetwarzania obrazu w czasie rzeczywistym. Układ prototypowy został wykonany w technologii CMOS 0,35 µm i zawiera matrycę SIMD procesorów analogowych o rozmiarze 64 x 64. Wymiary topografii matrycy wynoszą 2,2 mm x 2,2 mm, co daje gęstość 877 procesorów na mm^2. Matryca pobiera moc mniejszą niż 0,4 mW ze źródła zasilającego 3,3 V przy szybkości przetwarzania obrazów 100 kl/s. (**Mikromocowy procesor analogowy CMOS do wstępnego przetwarzania obrazu**).*

Keywords: CMOS analogue circuits, image processing, analogue processors.
Słowa kluczowe: układy analogowe CMOS, przetwarzanie obrazu, procesory analogowe.

Introduction

The vision sensors integrated together with a specialized microprocessor on a common silicon substrate, called vision chips, find applications in many technical areas, like: robotics, biomedical implants, systems controlling the road traffic, and automatic navigation systems. The main role of the vision chips is image detection and low-level, early-vision image processing, which typically includes: smoothing, edge detection, noise reduction, sharpening, etc. For autonomous systems, like robots or biomedical implants, the low-power operation is very important, because such systems are typically battery-powered. There are two main methods of the vision chips silicon implementation, analogue and digital. The digital implementations guarantee high accuracy of image signal processing, but need more supply power, and area on a silicon substrate, and therefore its implementation is more expensive [1-3]. The analogue vision chips consume less supply power for similar speed of image processing, and their accuracy is sufficient for aforementioned applications, therefore they are a better choice for low-cost system realizations. The analog vision chips have been under intensive research for the last decade, resulting in several prototype realizations reported in the literature [4-8]. The prototypes have very large throughput reaching 20 giga operations per second, but they characterize relatively big power consumption.

In this paper a description of an ultra-low power prototype integrated circuit is presented. One of the most important goal of the prototype circuit fabrication was practical verification of a new vision chip architecture and testing innovative circuit solutions. The presented ultra-low power vision chip is dedicated to low-cost low-power portable applications. The presented prototype consumes very small power due to elimination of all signal conditioning circuits, typically placed between the photo-diode and an analog processor. As a result a very simple processor with ultra-low power consumption based on a capacitance matrix is achieved. Due to the simplicity of the processor it is placed in a light-sensitive-matrix together with a photo-diode making an integrated analogue processing element (APE).

Vision chip architecture

The main part of the prototype integrated circuit is a matrix of APEs, as shown in Fig. 1. Each APE consists of a photo-detector and an analogue circuit calculating a convolution using 9 vision signals coming from its own and 8 neighboring photo-detectors. All APEs are controlled by the same signals, so they perform the same algorithms, working in parallel, according to a single instruction multiple data (SIMD) paradigm.

The final results of image signal processing are send outside the chip via 4 parallel outputs. The sequence of the rows and columns readout is controlled by two shift registers: a single 128-bit long used for the columns readout, and four 16-bit long for the rows readout.

In order to reduce the cost of a prototype fabrication a relatively small matrix (64 x 64 pixels) was design. On the other hand, the matrix size was selected big enough to be able to test its performance on practical images. It should be stressed that the matrix size can be easily extended to industrial standards, like for example VGA-resolution, by simple replication of APEs.

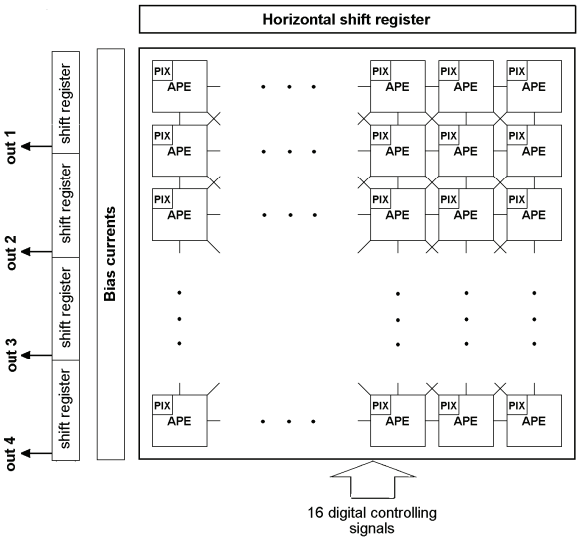

Fig.1. General architecture of the developed vision chip

Principle of APE operation

A simplified schematic of APE, shown in Fig. 2, explains the main principle of the convolution calculation performed by a single APE. In the figure the currents: i_N, i_{NE}, i_E, i_{SE}, i_S, i_{SW}, i_W, i_{NW}, and i_C represent the image signals coming from 8 neighboring photo-detectors and the photo-detector located inside the considered APE. Each current can be switched on and off by activation of a proper switch placed between a photo-diode and the integrating capacitor C_{int}.

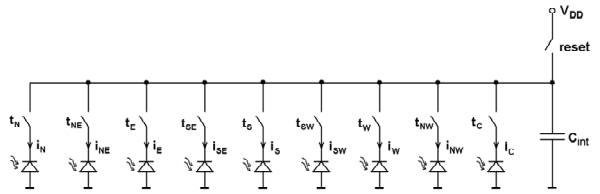

Fig.2. Simplified APE architecture

In the circuit each switch plays a twofold role, it selects the proper component in 3x3 convolution kernel, and also controls its magnitude. Each single switch can be independently switched on for a specific time interval, denoted in Fig. 2 by t_N, t_{NE}, t_E, t_{SE}, t_S, t_{SW}, t_W, t_{NW} and t_C. In a single cycle of APE operation, the switches are switched on sequentially in such a way that only one switch is on at a time. A relatively high sensitivity of the photo-diodes allows using short time intervals for an image reception, which results in almost unchanged magnitudes of all the currents during a single APE cycle. Because of that, there is no need for any additional analog memory for storing image signals during the time needed for completing APE cycle. Under such working conditions, the voltage change ΔV across C_{int} is related to magnitude of the currents generated by the photo-diodes and the switching-on time interval lengths:

$$\Delta V = \frac{1}{C_{\text{int}}}(t_N \cdot i_N + t_{NE} \cdot i_{NE} + t_E \cdot i_E + t_{SE} \cdot i_{SE} + t_S \cdot i_S + t_{SW} \cdot i_{SW} + t_W \cdot i_W + t_{NW} \cdot i_{NW} + t_C \cdot i_C) \quad (1)$$

The basic structure presented in Fig. 2, allows realization of the convolution calculation with only positive coefficients, because the time intervals can only have positive values. In order to realize negative coefficients an additional integrating capacitor of the same capacitance is also placed inside APE. The photo-diode currents related to the positive coefficients, in convolution kernel, are processed by one capacitor, whereas the signals related to the negative ones in the other capacitor. At the final stage of vision signal processing the convolution result is achieved by means of reading the difference between the voltages on both capacitors.

The method of the convolution calculation discussed above is optimized from power consumption point of view, because: (i) there is no need for implementation of an additional active circuit for negative coefficients realization, (ii) each APE only consumes power during a short resetting time interval. When the reset key is closed, the integration capacitor is charged to the supply voltage V_{DD}, and only during this time the supply power is consumed. For image acquisition speed of 100 fr/s and typical integrating capacitance C_{int} = 100 ÷ 1000 fF, the estimated supply power consumption related to C_{int} charging can be as small as $10^{-9} \div 10^{-10}$ W.

APE implementation

For the experimental integrated circuit realization a standard CMOS 0.35 μm technology offered by Austriamicrosystems (AMS) is selected. The technology allows fabrication of high quality linear capacitors using two layers of poly-silicon, which is crucial for APE realization. The topography of a single APE is depicted in Fig. 3. Most of the area (23 %) occupies the photo-diode, whereas the remaining area is divided between two integrating capacitors, analog and digital buses, and analog switches. For APE operation programming and controlling a 16-bit digital word is used. These digital signals define all values of the coefficients in (1).

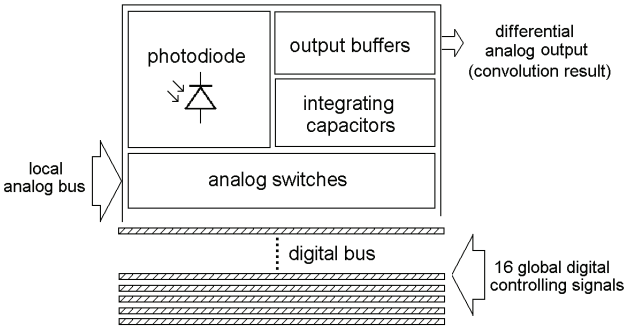

Fig.3. APE floorplan

Two separate capacitors are used for independent processing of two vision signals. The voltages on both capacitors are buffered and in the form of differential signals are routed outside the APE. It is important to explain that the differential vision signals are only required outside the light-sensitive-matrix, because inside the matrix the negative coefficients are realized by proper switching of signals between neighboring APEs. In the presented architecture only a single circuit for the differential signal calculation is needed for entire matrix, and therefore it can be easily implemented as an additional low-power subcircuit outside the matrix. An important, advantage of such an configuration is no mismatch between parameters of the circuit for vision signal processing, because all the signals are processed by the same single circuit.

The implemented APE circuit consists of 28 MOS transistors, which together with all the analog and digital controlling rails occupies 35 μm x 35 μm chip area. The layout has been designed with particular attention paid to minimizing capacitive coupling between various analog and digital signals. The control digital signals are not routed over elements such as transistors, capacitors and diodes. The APE area is shielded by the power supply and ground planes, which protects the APE circuitry from the incident light, while the photo-diode area is fully exposed to increase the photosensitivity.

Results of a prototype measurements

The microphotograph of a prototype integrated circuit is presented in Fig. 4. The developed measurement system, shown in Fig. 5, includes the following circuits: 4-channel AD converter, a dedicated module with a socket for the prototype vision chip and all the necessary supply circuits, and an evaluation FPGA Virtex4-SX35 board. The measurement system is controlled by a PC computer and a dedicated software responsible for generation of all the necessary signals and reading vision data from the chip. The software enables definition of all coefficients in the convolution kernel, and visualization of a recorded image. The test board is connected with a computer using USB interface. The image acquisition and visualization are performed in real time allowing recording pictures of moving objects. The examples of software windows for vision chip configuration, and image visualization are shown in Fig. 6, and Fig. 7 respectively.

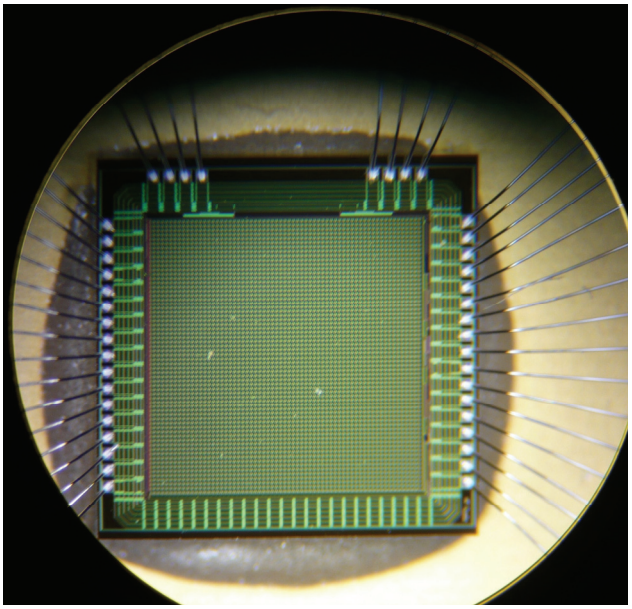

Fig.4. Prototype chip microfotograph

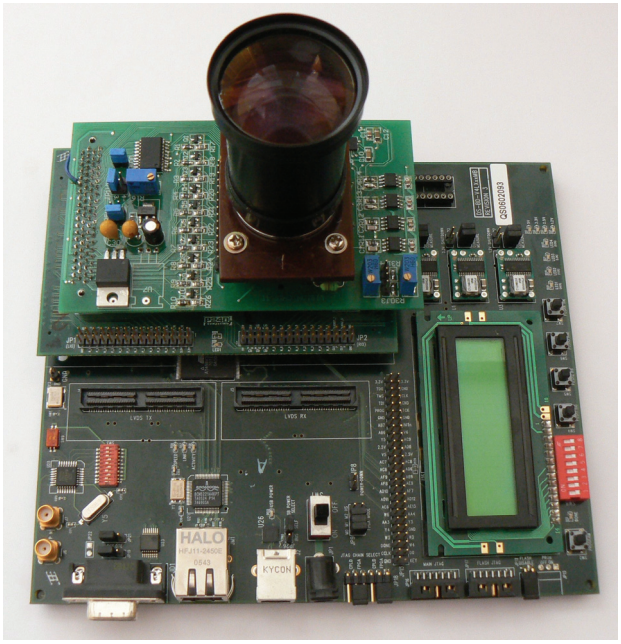

Fig.5. Measurement system

The presented vision chip can be configured to implement all typical convolution algorithms. The selected examples of image algorithms results are presented in Figs. 8 (b) – 9 (b). Fig. 8 (a) shows a raw image for the reference, whereas Fig. 8 (b) illustrates the left-bottom corner detection, Fig. 9 (a) the vertical edges detection, and Fig. 9 (b) all the edges detection (the laplasian). For the presented results, the achieved image processing accuracy is about 5-6 bit. The total processing error was evaluated for images presented in Fig. 8 (b), Fig. 9 (a) – (b). For these images, the achieved processing errors are equal to 1.8 %, 2.1 %, and 2.2 %, respectively. The error was defined as a root mean square (RMS) of difference between the perfect processing, using 16-bit resolution, and results achieved with the use of the presented vision chip. The results show that the accuracy offered by the developed analog APEs is typically sufficient for reliable image processing for low-resolution automats. The main parameters of the implemented vision chip are listed in Table 1.

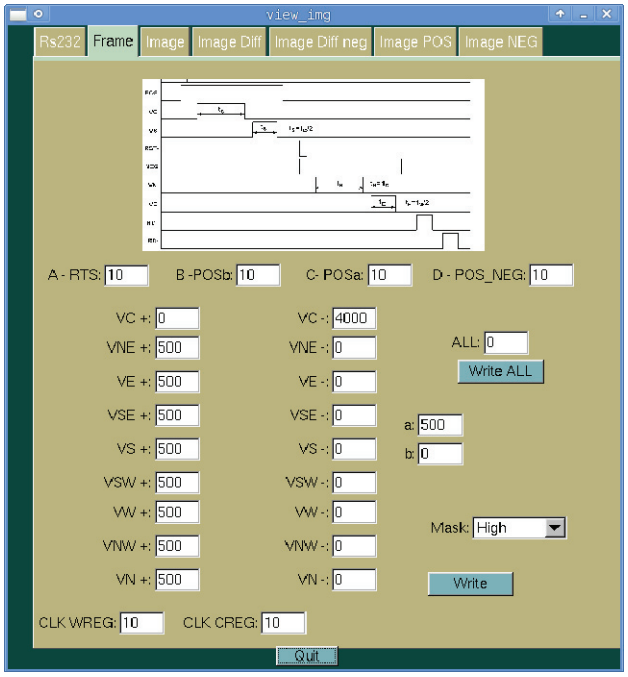

Fig.6. Vision chip configuration window

Fig.7. Window for recorded image visualization

Table 1. The main parameters of prototype circuit

Parameter	Value
Technology	0.35 μm AMS CMOS, 2P, 4M
Supply	3.3 V
Array size	64 × 64 pixels
APE dimensions	35 μm × 35 μm
Photodetector fill factor	23 %
APE density	877 cell/mm^2
Power per APE @ 100 fr/s	0.066 μW max
No. of transistors per APE	28
Implemented algorithms	Convolution with full 3 × 3 mask
Image filtering accuracy	About 2.5 %

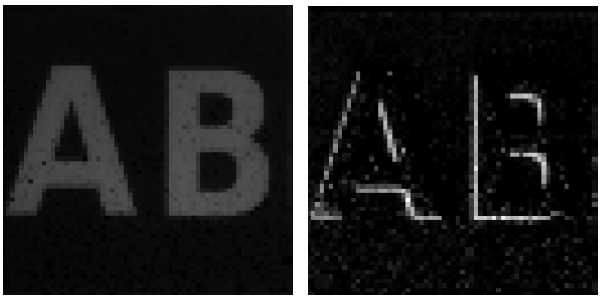

Fig.8. Results of image processing: (a) a raw image, (b) the left-bottom corner detection

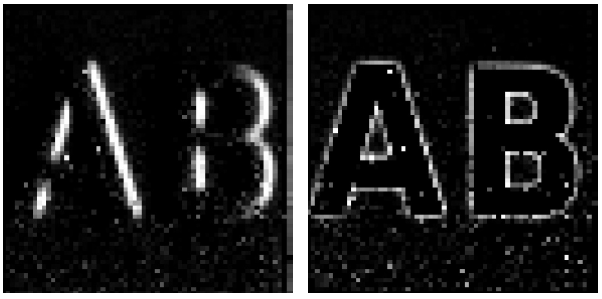

Fig.9. Results of image processing: (a) the vertical edges detection, (b) all the edges detection

Conclusions

The concept of a ultra-low power vision chip and its practical implementation using AMS CMOS 0.35 μm technology are presented and discussed. The prototype integrated circuit includes a photo-sensor matrix with analog early-vision processing elements. The designed processing elements combine extremely minimum circuitry (28 MOS transistors) and low power dissipation. Due to parallel signal processing a high-speed and ultra-low power operation can be achieved. The analog processors operate on the full 3x3 convolution kernel with positive and negative values of coefficients, and therefore all convolution algorithms can be implemented on the chip. The performed practical tests confirm a proper operation and full functionality of the fabricated prototype circuit. Despite a relatively low resolution (64x64 pixels) of the prototype, it has been possible to reliably process simple geometric images. The complete prototype vision chip consumes a few μW of power from 3.3 V supply voltage, which means that VGA-resolution variant of that vision chip would result in about 30 mW power consumption.

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