Postprint of: Lewicki A., Dead-Time Effect Compensation Based on Additional Phase Current Measurements, IEEE Transactions on Industrial Electronics, Vol. 62, Iss. 7 (2015), pp. 4078-4085, DOI: 10.1109/TIE.2015.2389756



# Dead-Time Effect Compensation Based on Additional Phase Current Measurements

Arkadiusz Lewicki

***Abstract*— This paper proposes a new method of dead-time effect compensation. The proposed solution is based on additional phase current measurements, realized by Analog to Digital (A/D) converters. These measurements are carried out at the time instants specified by a Pulse Width Modulation (PWM) strategy. This makes it possible to estimate inverter currents at the commutation instants and finally to estimate the voltage error caused by dead time. This voltage error is compensated during next switching period by modification of a reference voltage.**

**The proposed solution can be used to compensate the voltage error in a multilevel, multiphase Voltage Source Inverters (VSIs). The experimental researches were carried out on three-phase two-level and three-level Neutral Point Clamped (NPC) inverters supplying 55 kW and 160 kW motors, respectively. The results of the experimental investigations are presented in the paper.**

***Index Terms*— Dead-time effect, digital control of voltage source inverter, multilevel inverters, pulse width modulation**

## I. Introduction

PULSE Width Modulation (PWM) strategies for Voltage Source Inverters (VSIs) are based on the assumption that the inverter consists of ideal power-electronics switches. An infinitely short commutation time is assumed, and the voltage drops are assumed to be zero. Despite the continuous progress in power semiconductor technology, there are no power electronic switches that meet the above objectives. Because the turn-off time of a transistor is longer than the turn-on time, a dead-time must be set to prevent a short-circuit from being made by simultaneously switching on upper and lower transistors. The dead-time delays the activation of the next transistor until the previous one in the same inverter branch is fully deactivated. When transistors in one inverter branch are deactivated, the potential on the inverter terminal depends on the direction of current flow (Fig. 1). This phenomenon (called the dead-time effect), nonzero commutation times, and voltage drops on conducting transistors and diodes have a significant impact on the correctness of the inverter's output voltage. All voltage distortion sources of VSI and their influence on the inverter output voltage are summarized in [1].

Manuscript received April 10, 2014; revised July 22, 2014, September 10, 2014 and October 29, 2014; accepted December 8, 2014.



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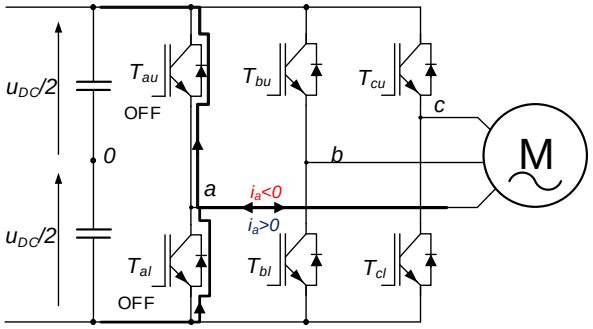


Fig. 1. Two-level three-phase VSI

Dead-time effect compensation strategies can be divided into two groups. The first group includes strategies in which gate signal sequences are modified [2]-[7]. These methods can be called pulse-based compensation strategies [3]. The gate pulse durations for inverter transistors are changed in order to counteract the dead-time effect [2, 5, 7] and to compensate the voltage drops on conducting transistors and diodes [4, 6]. It can be realized on basis of measured or detected phase current directions [2, 3, 8, 29]. In the inverters, where field oriented control is implemented, there exists a relation between the current polarities and the electrical rotor angle, which is already available for field orientation. The compensation algorithms can also be realized on basis of current vector position [5, 6].

The second group consists of compensation strategies in which the voltage error caused by dead-time is reduced by modification of a reference voltage. In these solutions a compensating voltage is added to the reference voltage [10, 11]. Because these compensation strategies utilize the average value of compensating voltage, they can be called average value compensation strategies or volt-second compensation methods [6, 27]. Due to their simplicity, they can be used in multiphase and multilevel VSI [12].

The compensating voltage should be equal to the voltage disturbance caused by inverter nonlinearities. It can be defined as the difference between the reference voltage vector and the voltage vector generated in the inverter:

$$\Delta \boldsymbol{u}_{o(comp)} = \boldsymbol{u}'_{o(ref)} - \boldsymbol{u}_o , \qquad (1)$$

where $\boldsymbol{u}'_{o(ref)}$ is a reference output voltage vector (meaning of

the symbol " ′ " is explained in section III) and $\boldsymbol{u}_o$ is an inverter output voltage vector.

Dead-time effect compensation strategies in which the reference voltage is modified make it possible to create a feedback for precise control of the inverter output voltage. The parameters of the compensating voltage, added to the reference voltage vector, can be tuned in order to reduce the dead-time effect [13]. The resulting effect of dead-time mainly manifests in an increased content of odd harmonics of inverter phase currents (fifth and seventh in three-phase inverters, third and seventh in five-phase inverters) [14, 15]. Fourier analysis of inverter phase currents makes it possible to prepare a compensation strategy, which will reduce selected current harmonics.

Proper compensation of inverter nonlinearities requires information about the voltage vector generated in the inverter. Because of its shape, the inverter output voltage cannot be measured using A/D (Analog to Digital) converters. The only way to identify the inverter output voltage is to estimate it using available currents and voltage measurement. The compensating voltage can be determined using estimators [10, 17, 18, 32] or adaptive strategies [7]. It can be estimated based on analysis of current slope [19, 28, 30] and can be determined by PI [20] or resonant controllers [21].

The compensating voltage can also be determined immediately in dependence on phase currents, DC-link voltage, and PWM frequency [10, 22]. The dead-time effect will be compensated properly if the phase currents and DC-link voltage are known at the instants of active and zero voltage vector activation. Because of multiple changes of current direction caused by active voltage vectors and the zero current clamping phenomenon, accurate determination of the phase current polarity is very challenging. The direction of phase current can be determined using additional sensors [8, 23, 24, 31], estimated from the electrical angle [9, 25] or obtained using inverter load model [26].

In most solutions the phase currents are measured at the beginning of each pulse period. The compensation strategies, realized during the (*n*)-th pulse period, are based on information about the phase currents measured at the beginning of the same (*n*)-th pulse period. If the phase current is close to zero, its direction may change during the pulse period. Detection of current polarity, when the phase current is close to zero, is one of the biggest challenges in dead-time effect compensation strategies. In order to prevent undesired current distortions caused by incorrect determination of current polarity some restrictions on compensation methods should be defined. The compensation may be ignored when the phase current is close to zero and its polarity can not be determined correctly [9, 10].

In this paper a new method of inverter output voltage identification is proposed. The solution utilizes information about phase currents and DC-link voltages. The values of currents and voltages are repeatedly measured at the beginning of the pulse period and at the time instants dependent on the switching sequences. The proposed solution makes it possible to identify phase currents and DC-link voltages at the commutation instants and allows the voltage error due to dead-time and voltage drops to be determined. This solution has been used for dead-time effect compensation in two- and three-level NPC converters supplying 55 kW and 160 kW asynchronous motors. The results of the experimental investigation are presented in the paper.

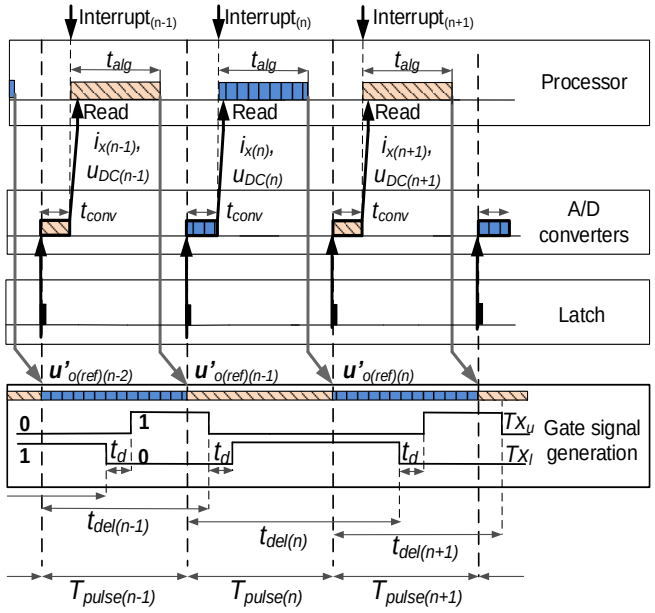


Fig. 2. Timing in the microprocessor control system for the VSI.

The paper is organized as follows: in section II a structure of classic digital control system for Voltage Source Inverters is described. In section III the modification of this structure is proposed and utilized method of dead-time effect compensation is presented. The estimation method of inverter output voltage, based on additional measurements of phase currents and DC-link voltage, is proposed in section IV. The results of experimental investigation are presented in the section V. In the section VI the limitations of proposed method are discussed.

## II. Digital Control of a Voltage Source Inverter

Power electronic converters are constructed as digitally controlled units. The values of inverter phase currents: $i_{x(n)}$ and DC-link voltages: $u_{DC(n)}$ (Fig. 2) are measured using current and voltage transducers and A/D converters, where index (*n*) denotes actual sample and "*x*" denotes an inverter phase (*x=a, b or c*). These measurements are carried out at the beginning of every pulse period (Fig. 2).

When the inverter output voltage is generated, the upper $T_{xu}$ and lower $T_{xl}$ transistors are switched alternately (Fig. 2), where "1" indicates switched-on and "0" defines switched-off transistors. A dead-time $t_d$ must be set to prevent a short-circuit from being made by simultaneously switching on upper and lower transistors.

During any of the pulse periods a control algorithm, PWM strategy and dead-time effect compensation strategy are realized in the microprocessor with the computation time $t_{alg}$ (Fig. 2). These algorithms utilize the information about

measured phase currents and DC-link voltages. The measurement frequency and the frequency of control algorithm computation are usually the same.

The values of inverter currents and voltages, which are used to determine the amplitude and position of the (*n*)-th reference voltage vector ($\boldsymbol{u}'_{o(ref)(n)}$), are measured at the beginning of the (*n*)-th pulse period (Fig. 2). At the same time the generation of the previous voltage vector ($\boldsymbol{u}_{o(n-1)}$) begins. The generation of the voltage vector ($\boldsymbol{u}_{o(n)}$) is delayed by a time equal to the pulse period ($T_{pulse}$). This time includes the computation time of the control algorithm ($t_{alg}$) and the conversion time ($t_{conv}$) of the A/D converters (Fig. 2). If the generation of the output voltage vector requires several commutations, the time ($t_{del}$) between current and voltage measurement and a commutation will be in the range of one to two pulse periods (Fig. 2):

$$T_{pulse(n-1)} \le t_{del(n-1)} \le T_{pulse(n-1)} + T_{pulse(n)}, \qquad (2)$$

where $T_{pulse(n)}$ – actual pulse period, $t_{del(n-1)}$ – delay between (*n-1*)-th measurements and the commutation in the (*n*)-th pulse period.

The delay ($t_{del}$) affects the correctness of dead-time effect compensation especially in the case when the phase current reaches zero. The changes of phase current direction between measurement and commutation result in faulty operation of the dead-time effect compensation strategy.

## III. Compensation of Dead-Time Effect in Voltage Source Inverters

In the proposed solution the voltage disturbances of VSI are compensated by modification of a reference voltage vector. The voltage disturbance vector can be determined for the (*n-1*)-th pulse period by comparing a reference voltage vector with the inverter output voltage.

$$\Delta\boldsymbol{u}_{o(comp)(n-1)} = \boldsymbol{u}'_{o(ref)(n-1)} - \boldsymbol{u}_{o(n-1)}, \qquad (3)$$

where $\Delta\boldsymbol{u}_{(comp)(n-1)}$ is the voltage disturbance vector, $\boldsymbol{u}'_{o(ref)(n-1)}$ is the reference voltage vector, and $\boldsymbol{u}_{o(n-1)}$ is the generated (or estimated) inverter output voltage, all determined for the (*n–1*)-th pulse period.

The determined voltage disturbance vector can be used as a compensating voltage in the next (*n*)-th pulse period:

$$\boldsymbol{u}'_{o(ref)(n)} = \boldsymbol{u}_{o(ref)(n)} + \Delta\boldsymbol{u}_{o(comp)(n-1)}, \qquad (4)$$

where $\boldsymbol{u}'_{o(ref)(n)}$ is the new reference voltage vector and $\boldsymbol{u}_{o(ref)(n)}$ is the reference voltage vector determined by the VSI control system for the (*n*)-th pulse period.

The reference voltage vector $\boldsymbol{u}'_{o(ref)(n-1)}$ is determined by a microprocessor during the (*n–1*)-th pulse period. This voltage vector will be generated in the inverter during the next (*n*)-th period (Fig. 2).

The obtained output voltage $\boldsymbol{u}_{o(n-1)}$ can be estimated if the activation times of the transistors and directions of phase currents are known for the whole pulse period. The directions of phase currents can be determined using additional sensors, but usually—in these solutions—an additional separation between sensors and microprocessor circuit is required. The values of phase current for the commutation instant can also be determined with additional measurements at selected time instants. These measurements can be realized using standard inverter sensors.

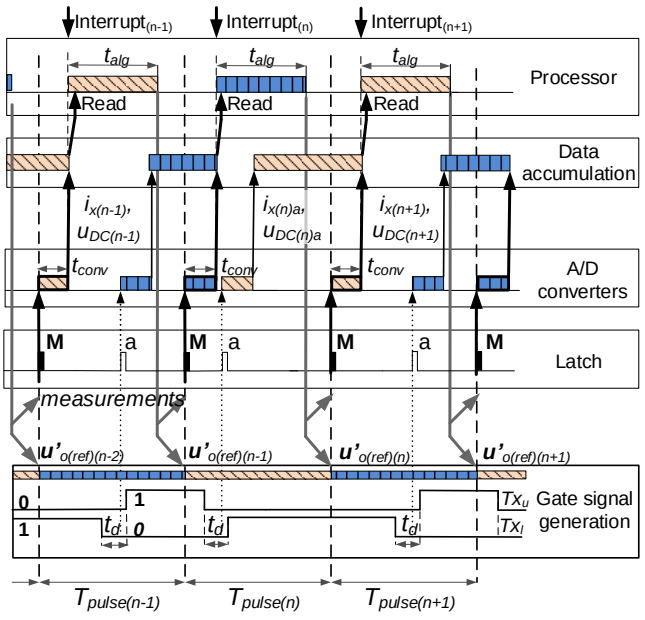


Fig. 3. Proposed timing for microprocessor control system with additional measurements using A/D converters: "M" - main measurements, "a" – additional measurements (during dead-time)

The maximum frequency of transistor switching is in the range of several hertz to several kilohertz. Currently produced microprocessors can compute the position and amplitude of inverter output voltage during several microseconds. The phase currents and DC-link voltages at the beginning of every pulse period are measured using A/D converters (Fig. 2). The measurement frequency depends on the processor speed. In a large part of the pulse period the A/D converters remain deactivated. It is possible to realize a few additional measurements using A/D converters when the inverter output voltage is generated. In the proposed solution additional measurements of phase currents are realized at the time instants determined by the switching sequences of the inverter transistors (Fig. 3). Simultaneous latch of all A/D converter channels gives additional information about DC-link voltage changes during a pulse period.

Analysis of switching sequences, designated in PWM algorithms, makes it possible to specify the commutation instants for any inverter branch. It also makes it possible to determine the instants when dead-time will be introduced to these sequences. Additional measurements of phase currents: $i_{x(n-1)a}$, $i_{x(n)a}$ (Fig. 3) and (optionally) DC-link voltages: $u_{DC(n-1)a}$, $u_{DC(n)a}$ can be realized during the dead-times, when inverter transistors remain deactivated. The measurement instants are synchronized with commutation in this inverter phase, where the current is close to zero. This makes it possible to detect the

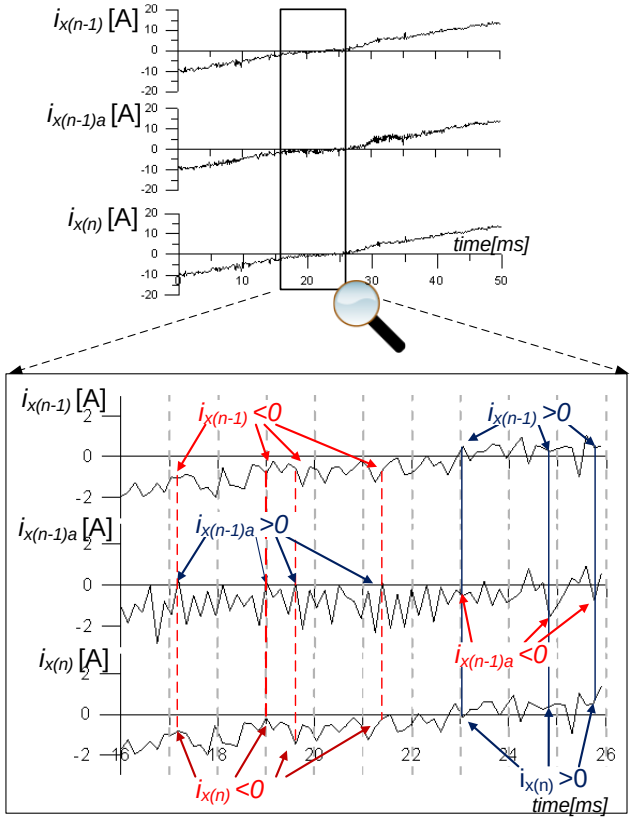


Fig. 4. The "*x*" phase current of the two-level VSI measured using A/D converter at the beginning of (*n–1*)-th and (*n*)-th pulse periods ($i_{x(n-1)}$, $i_{x(n)}$) and during the dead-time ($i_{x(n-1)a}$). Results of experimental investigations

phase current direction (and value) during the dead-time (Fig. 4).

The experimental results for the two-level VSI, supplying 55kW unloaded induction machine, with additional phase current measurements are presented in Figure 4. The values of inverter phase current were measured using an A/D converter at the beginning of the (*n–1*)-th and (*n*)-th switching periods ($i_{x(n-1)}$ and $i_{x(n)}$ respectively). The $i_{x(n-1)}$ is delayed with respect to $i_{x(n)}$ by one pulse period. $i_{x(n-1)a}$ is a current in the same inverter phase, but measured 0.5µs before the end of a dead-time. Additional phase current measurements make it possible to detect the changes of phase current directions caused by active voltage vectors (Fig. 4). These changes are the main cause of improper dead-time effect compensation.

## IV. Estimation of Output Voltage Vector of Voltage Source Inverter

Estimation of the output voltage vector requires information about the phase current at the commutation instant, the duration of active and zero voltage vectors and DC-link voltages. The DC-link voltages and phase currents are measured at selected time instants. Assuming that they change linearly between measurements and the results of one additional measurement are available, the phase currents and

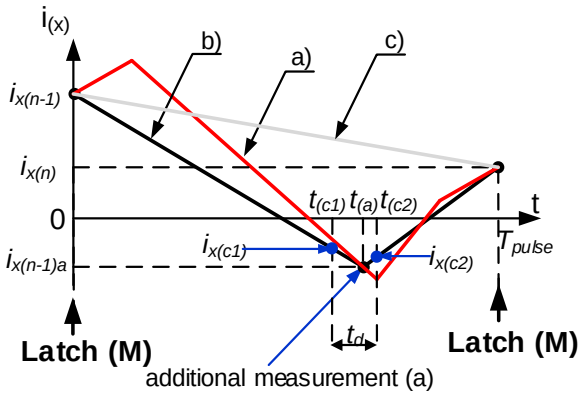


Fig. 5. The real a) and reconstructed b) c) waveforms of an inverter phase current. The reconstruction is based b) and not based c) on additional measurement of a phase current. The measurement instants: main (**M**) and additional (a).

DC-link voltages at the beginning ($_{c1}$) and at the end ($_{c2}$) of dead-time $t_d$ (Fig. 5) can be calculated as:

$$
\begin{aligned}
u_{DC(c1)} &= \left( \frac{u_{DC(n-1)a} - u_{DC(n-1)}}{t_{(a)}} \right) \cdot t_{(c1)} + u_{DC(n-1)}, \\
i_{x(c1)} &= \left( \frac{i_{x(n-1)a} - i_{x(n-1)}}{t_{(a)}} \right) \cdot t_{(c1)} + i_{x(n-1)}, \\
u_{DC(c2)} &= \\
&\left( \frac{u_{DC(n)} - u_{DC(n-1)a}}{T_{pulse} - t_{(a)}} \right) \cdot \left( t_{(c2)} - t_{(a)} \right) + u_{DC(n-1)a}, \\
i_{x(c2)} &= \\
&\left( \frac{i_{x(n)} - i_{x(n-1)a}}{T_{pulse} - t_{(a)}} \right) \cdot \left( t_{(c2)} - t_{(a)} \right) + i_{x(n-1)a},
\end{aligned}
\tag{5}
$$

where $i_{x(c1)}$, $i_{x(c2)}$, $u_{DC(c1)}$, $u_{DC(c2)}$ are the phase currents and DC-link voltages reconstructed for the beginning ($t_{(c1)}$) and for the end ($t_{(c2)}$) of a dead time (Fig. 5), $i_{x(n-1)}$, $i_{x(n)}$, $u_{DC(n-1)}$, $u_{DC(n)}$ are the phase currents and DC-link voltages measured at the beginning of (*n-1*)-th and (*n*)-th pulse periods, respectively (Fig. 3, 5), $i_{x(n-1)a}$, $u_{DC(n-1)a}$, are the phase current and DC-link voltage measured during the dead-time, $t_{(a)}$ is the instant of additional measurement.

In the same manner the DC-link voltages and phase current for any commutation instants can be determined.

The additional measurements cannot be done if the duration of zero voltage vectors is less than the conversion time of A/D converters. In this case the reconstruction of a phase current and DC-link voltages can be realized with reduced accuracy. The phase currents and DC-link voltages can be estimated from (Fig. 5c):

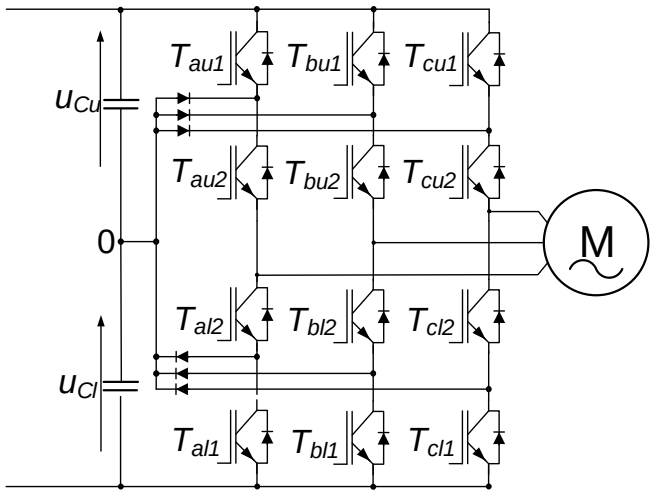


Fig. 6. Three-level three-phase NPC inverter

$$
\begin{aligned}
u_{DC(c1)} &= \left( \frac{u_{DC(n)} - u_{DC(n-1)}}{T_{pulse}} \right) \cdot t_{(c1)} + u_{DC(n-1)}, \\
i_{x(c1)} &= \left( \frac{i_{x(n)} - i_{x(n-1)}}{T_{pulse}} \right) \cdot t_{(c1)} + i_{x(n-1)}, \\
u_{DC(c2)} &= \left( \frac{u_{DC(n)} - u_{DC(n-1)}}{T_{pulse}} \right) \cdot t_{(c2)} + u_{DC(n-1)}, \\
i_{x(c2)} &= \left( \frac{i_{x(n)} - i_{x(n-1)}}{T_{pulse}} \right) \cdot t_{(c2)} + i_{x(n-1)},
\end{aligned}
\tag{6}
$$

where the indexes (*n*) and (*n–1*) denote the main measurements realized at the beginning of (*n*) and (*n–1*) pulse periods, respectively.

The phase current direction, reconstructed for the beginning of a dead-time ($t_{(c1)}$ / Fig. 5), can be used in dead-time effect compensation algorithm. The phase current polarity, determined for the end of the dead-time ($t_{(c2)}$), can be used to compensate the voltage drops. Because utilized dead-time effect compensation strategy (3)-(4) require information about inverter output voltage, it is necessary to calculate it. The voltage between the "x" terminal of a two-level inverter and the DC-link neutral point can be determined from (Fig. 1):

$$
u_{x0(i)} = \begin{cases} u_{DC(i)}/2 \Leftrightarrow \left( \left( T_{xu(i)} = 0 \wedge T_{xl(i)} = 0 \right) \wedge i_{x(i)} < 0 \right) \\ \qquad \vee \left( T_{xu(i)} = 1 \wedge T_{xl(i)} = 0 \right) \\ -u_{DC(i)}/2 \Leftrightarrow \left( \left( T_{xu(i)} = 0 \wedge T_{xl(i)} = 0 \right) \wedge i_{x(i)} > 0 \right) \\ \qquad \vee \left( T_{xu(i)} = 0 \wedge T_{xl(i)} = 1 \right) \end{cases}, \tag{7}
$$

where $u_{DC(i)}$ and $i_{x(i)}$ are the DC-link voltage and phase "*x*" current during generation of the (*i*)-th zero or active voltage vector in the VSI, respectively or during dead-time; "*1*" denotes that the transistor is switched on and "*0*" that it remains switched off .

The voltage between the "*x*" terminal of the three-level NPC inverter (Fig. 6) and the DC-link neutral point can be calculated using (8):

$$
\begin{aligned}
&u_{(x0)i} = u_{(Cu)i} \Leftrightarrow \\
&\begin{cases} \left( \begin{matrix} Tx_{(u1)i} = 1 \wedge Tx_{(u2)i} = 1 \wedge \\ Tx_{(l2)i} = 0 \wedge Tx_{(l1)i} = 0 \end{matrix} \right) \\ \vee \left( \left( \begin{matrix} Tx_{(u1)i} = 0 \wedge Tx_{(u2)i} = 1 \wedge \\ Tx_{(l2)i} = 0 \wedge Tx_{(l1)i} = 0 \end{matrix} \right) \wedge i_{(x)i} < 0 \right), \end{cases} \\
&u_{(x0)i} = -u_{(Cl)i} \Leftrightarrow \\
&\begin{cases} \left( \begin{matrix} Tx_{(u1)i} = 0 \wedge Tx_{(u2)i} = 0 \wedge \\ Tx_{(l2)i} = 1 \wedge Tx_{(l1)i} = 1 \end{matrix} \right) \\ \vee \left( \left( \begin{matrix} Tx_{(u1)i} = 0 \wedge Tx_{(u2)i} = 0 \wedge \\ Tx_{(l2)i} = 1 \wedge Tx_{(l1)i} = 0 \end{matrix} \right) \wedge i_{(x)i} > 0 \right), \end{cases} \\
&u_{(x0)i} = 0 \Leftrightarrow \\
&\begin{cases} \left( \begin{matrix} Tx_{(u1)i} = 0 \wedge Tx_{(u2)i} = 1 \wedge \\ Tx_{(l2)i} = 1 \wedge Tx_{(l1)i} = 0 \end{matrix} \right) \vee \\ \left( \left( \begin{matrix} Tx_{(u1)i} = 0 \wedge Tx_{(u2)i} = 1 \wedge \\ Tx_{(l2)i} = 0 \wedge Tx_{(l1)i} = 0 \end{matrix} \right) \wedge i_{(x)i} > 0 \right) \vee \\ \left( \left( \begin{matrix} Tx_{(u1)i} = 0 \wedge Tx_{(u2)i} = 0 \wedge \\ Tx_{(l2)i} = 1 \wedge Tx_{(l1)i} = 0 \end{matrix} \right) \wedge i_{(x)i} < 0 \right). \end{cases}
\end{aligned}
\tag{8}
$$

The components of the active and zero voltage vectors can be determined by substituting (9):

$$
\begin{aligned}
u_{an} &= \frac{2 \cdot u_{a0} - u_{b0} - u_{c0}}{3}, \\
u_{bn} &= \frac{2 \cdot u_{b0} - u_{a0} - u_{c0}}{3}, \\
u_{cn} &= \frac{2 \cdot u_{c0} - u_{a0} - u_{b0}}{3},
\end{aligned}
\tag{9}
$$

into the Clarke transformation (10):

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} u_{an} \\ u_{bn} \\ u_{cn} \end{bmatrix}, \qquad (10)$$

where $u_\alpha$ and $u_\beta$ are the components of the active and zero voltage vectors used for generating the inverter output voltage.

The components of the voltage vector, generated in the inverter during the ($n$)-th pulse period, can be determined from (14):

$$u_{o\alpha(n-1)} = \frac{1}{T_{pulse(n-1)}} \sum_{i=1}^{k} \left( u_{\alpha(i)} \cdot t_i \right),$$
$$u_{o\beta(n-1)} = \frac{1}{T_{pulse(n-1)}} \sum_{i=1}^{k} \left( u_{\beta(i)} \cdot t_i \right), \qquad (11)$$

where $k$ is the quantity of active and zero voltage vectors used for generating the output voltage vector in VSI, $t_i$ are the activation times of these vectors, $u_{o\alpha(n-1)}$, $u_{o\beta(n-1)}$ are the components of output voltage vector $\mathbf{u}_{o(n-1)}$ (3). The activation times (including the dead-times introduced to the switching sequences) are determined in PWM algorithm.

Calculation of inverter output voltage is valid only for the actual sampling period. In many solutions of SV-PWM strategies the sequence of the active and zero voltage vectors is reversed every pulse period. If the sequence of four voltage vectors (two zero and two active vectors): $zero_1 \rightarrow active_1 \rightarrow active_2 \rightarrow zero_2$ during even pulse period is utilized, the reverse sequence of the same voltage vectors: $zero_2 \rightarrow active_2 \rightarrow active_1 \rightarrow zero_1$ will be activated during next, odd pulse periods. The compensation algorithm, realized in microprocessor during ($n$)-th (even) pulse period $T_{pulse(n)}$ (Fig. 3), utilizes phase currents measured during previous (odd) pulse period ($T_{pulse(n-1)}$). Compensation of inverter nonlinearities bases on modification of a reference voltage. This voltage vector will be generated during the next (odd) pulse period $T_{pulse(n+1)}$ (Fig. 3). The voltage disturbance, restored for the switching sequence of odd pulse period, will be compensated during activation of the same switching sequence in the next odd pulse period. It can be assumed that the dead-time effect is compensated without any delay if the inverter voltage and current vectors remain in their sectors during three pulse periods (if the polarities of phase current and voltages remain the same). Otherwise, the voltage disturbances will be compensated with delay in relation to their occurrence.

Proposed solution makes it possible to identify the inverter phase currents at the commutation instant. Since the phase current directions are known for any active or zero voltage vector, it is possible to estimate and to compensate the voltage drops on conducting transistors and diodes. It is also possible to combine the proposed solution with any other compensation algorithm. In this case the proposed strategy will correct the disturbances caused by other compensation algorithms.

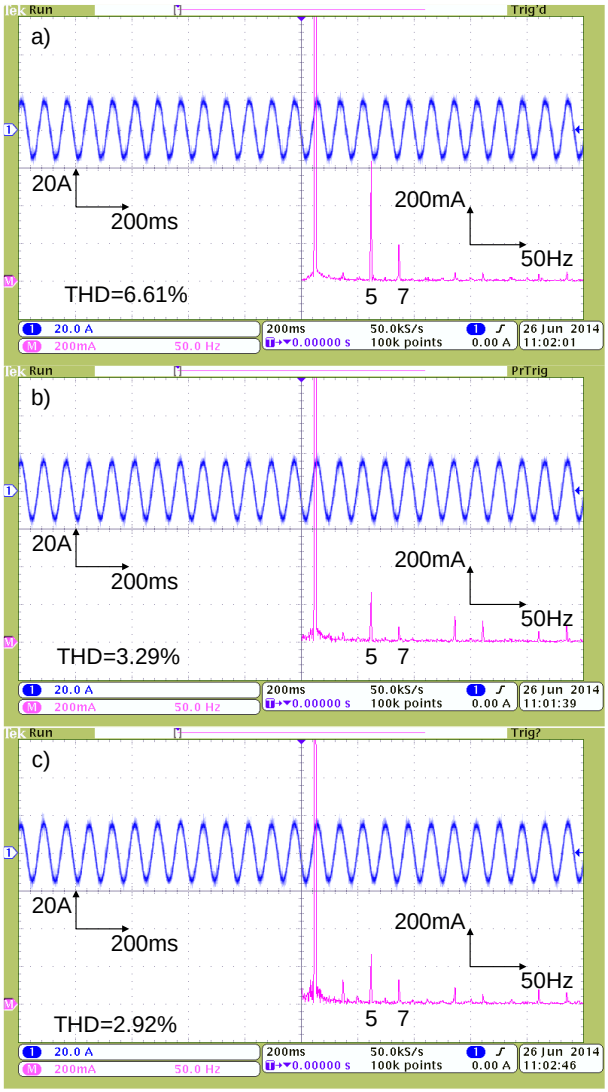


Fig. 7. The harmonics and phase current waveform of a two-level VSI without a) and with compensation of dead-time effect using classic b) and proposed compensation method c). The frequency of output voltage vector: $f$=12.5Hz. Indicated: 5-th and 7-th harmonics of a phase current

## V. Results of Experimental Investigations

The experimental research was carried out on three-phase two-level ($u_{DC}$=690V) (Figs. 4, 7, 8, 9, 11) and three-phase three-level NPC ($u_{DC}$=560V) inverters (Figs. 10) supplying no-load 55 kW and 160 kW asynchronous motors respectively. The other parameters (for both inverters): dead-time $t_d$=2.5$\mu$s, pulse period $T_{pulse}$=150$\mu$s, switching frequency $f_{sw}$=3.33kHz. In both inverters two-phase currents and a DC-link voltage were measured.

The microprocessor system contains: a floating-point DSP processor (the computation of AC motor control strategy and SV-PWM algorithm), FPGA (control of A/D converter, data acquisition and buffering, generation of transistor gate signals) and 8-channel, 14-bit A/D converter with simultaneous sampling of all channels and conversion time $t_{conv}$=3.7$\mu$s.

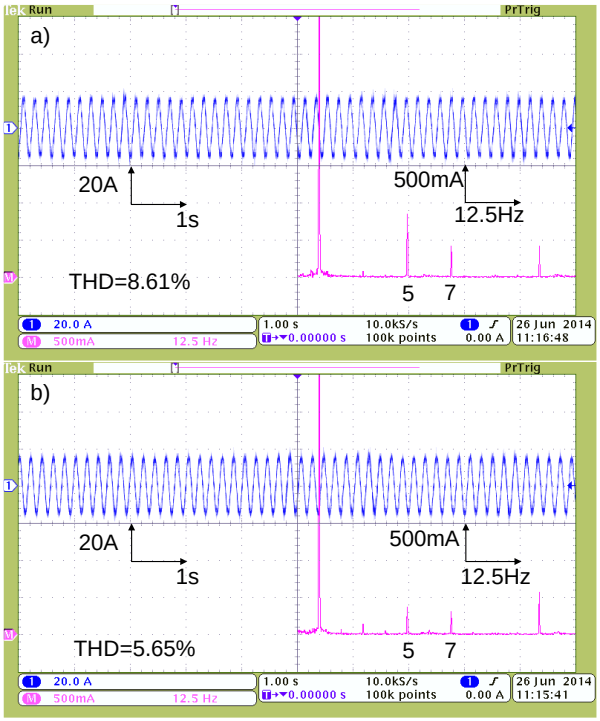


Fig. 8. The harmonics and phase current waveform of a two-level VSI with compensation of dead-time effect using classic (a) and proposed compensation method (b). The frequency of output voltage vector: f=5Hz. Indicated: 5-th and 7-th harmonics of a phase current.

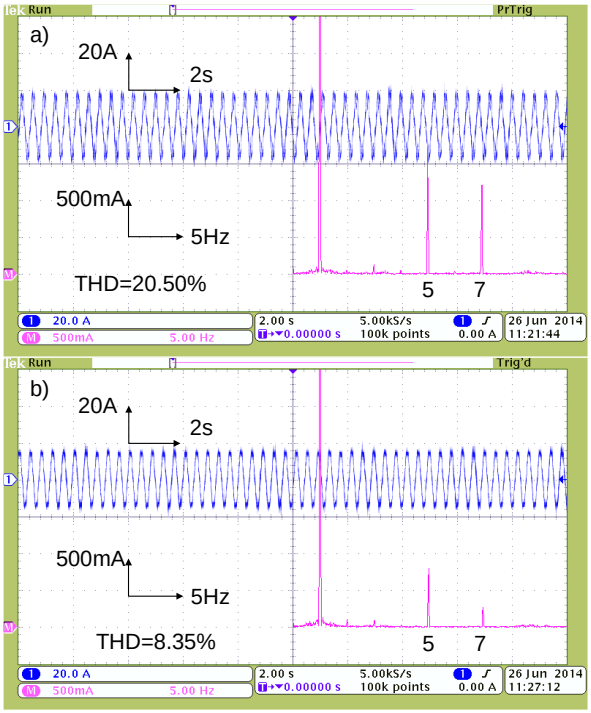


Fig.9. The harmonics and phase current waveform of a two-level VSI with compensation of dead-time effect using classic (a) and proposed compensation method (b). The frequency of output voltage vector: f=2.5Hz. Indicated: 5-th and 7-th harmonics of a phase current.

The phase current waveforms and THD (up to 40 harmonics) of the two-level inverter in Figures 7, 8, 9 are presented. The dead-time effect was not compensated (Fig. 7a) and was compensated using classic, pulse based compensation strategy (Fig. 7b, Fig. 8a, Fig. 9a) and proposed (Fig. 7c, Fig. 8b, Fig. 9b) method. Utilized classic, pulse-based compensation strategy bases on information of phase current directions measured at the beginning of each pulse period.

In comparison with classic compensation method the proposed solution gives similar effects for higher frequencies of output voltage (Fig. 7b, 7c). During generation of lower frequency output voltages the amplitudes of 5-th and 7-th current harmonics are lower by about 50% (Fig. 8a, 8b; Fig. 9a, 9b) when proposed solution is utilized. This is caused by extension of the period, when phase currents are close to zero and their directions can be changed during a pulse period. Additional current measurements allow detecting these changes and improving the compensation accuracy.

Proposed strategy makes it possible to compensate the dead-time effect in multilevel VSI. The phase current waveform and THD (up to 40 harmonics) of a three-level NPC inverter without compensation of the dead-time effect is shown in Figure 10a. Figure 10b shows the phase current waveform and harmonics of the NPC inverter where the dead-time effect has been compensated.

## VI. Limitations of the Proposed Solution

In the proposed solution some constraints related to the properties of digital controller have to be taken into account. The conversion time ($t_{conv}$) of the A/D converters is not equal to zero. Because the measurements realized at the beginning of any switching period have the highest priority, there is no possibility of further measurements at any time instant. Additional measurements can be realized not earlier than the time ($t_{conv}$) from the beginning of the pulse period and no later than ($T_{pulse} - t_{conv}$) before its end.

The second constraint is related to the architecture of the microprocessor system. If the simultaneous latch of two phase currents and DC-link voltage is required, A/D converter with at least 3 sample and hold channel is needed. It is also necessary to ensure a memory area for storing additional measurement results.

The next constraint relates to the high frequency (HF) current oscillations after commutation (Fig. 11). These oscillations may have an influence on the accuracy of current measurement during dead time, however the current polarity can be determined correctly. The problem of high frequency current oscillations can be reduced by appropriately selected low-pass analog filters in the measurement system.

The last constraint of the proposed solution relates to the measurement accuracy. The information about the current signs is not sufficient to compensate the voltage disturbances caused by parasitic capacitances or zero current clamping phenomenon. When the IGBT is switched-off the dv/dt depends on the current value, especially when the phase current is close to zero. Compensation of these phenomena requires precise information about the phase current value during commutation. Limited accuracy of current measurements restrict the applicability of the proposed method only to compensate the dead-time effect and voltage drops on

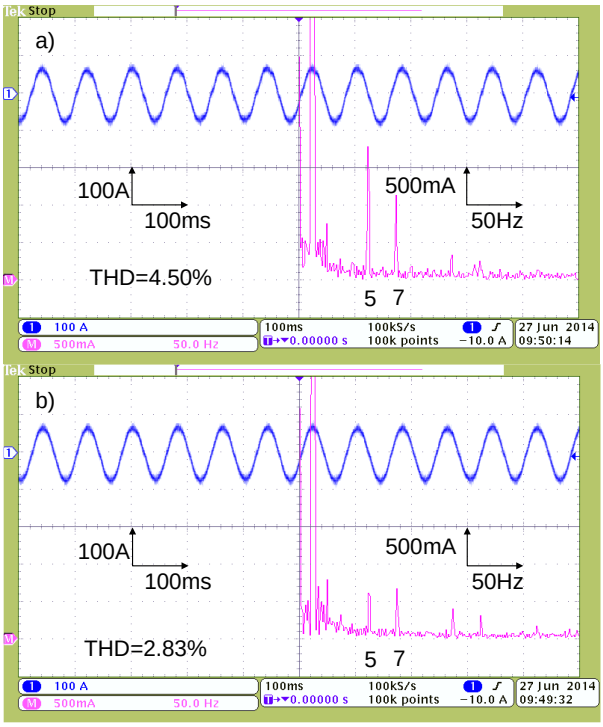


Fig. 10. The harmonics and phase current waveform of three-level NPC Voltage Source Inverter without a) and with compensation of dead-time effect b). The frequency of output voltage vector: $f$=12.5Hz. Indicated: 5-th and 7-th harmonics of a phase current

conducting transistors and diodes. This is the cause for inaccurate compensation of inverter nonlinearities (Fig. 7c, Fig. 8b, Fig. 9b). Additionally, generating of a low frequency output voltage increases the time period when the phase current is close to zero. In this case the parasitical capacitances have a greater impact on the inverter output voltage and the current harmonics (Fig. 8b, Fig. 9b).

## VII. Conclusion

This paper proposes a new method of inverter nonlinearities compensation. The proposed solution utilizes additional measurements of inverter phase currents and DC-link voltages. Additional measurements were realized at the time instants dependent on switching sequences. This made it possible to restore the phase currents and DC-link voltages for any instant of a switching period. Because the DC-link voltage does not vary greatly during a switching period, it is possible to utilize only current measurements in proposed algorithm. This will reduce the computation amount realized in microprocessor.

In proposed solution the additional measurements were utilized to estimate the output voltage error. Restored output voltage vector has been used for dead-time effect compensation in two-level and three-level NPC inverters. It can also be utilized to compensate for nonlinearities in multi-phase and multi-level VSIs.

The additional measurements were carried out 0.5µs before the end of a dead-time. Due to the utilized low-pass analog filters (in the measurement system) and relatively small

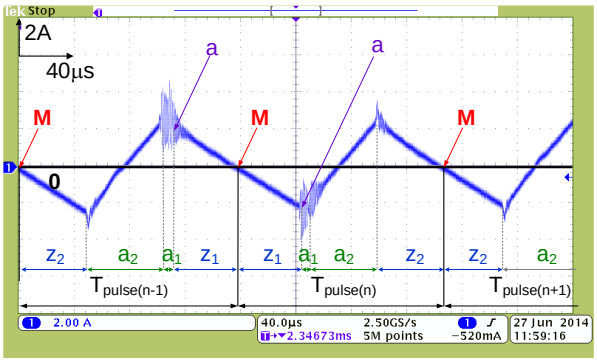


Fig. 11. Detection of current polarity when the phase current is close to zero: $z_1$, $z_2$, $a_1$, $a_2$ – zero ($z_1$, $z_2$) and active ($a_1$, $a_2$) voltage vector, M – main measurement of a phase current, a – additional measurement of a phase current

amplitude of the HF current oscillations after commutation (Fig. 11) the changes of this time instant had a negligible effect on the accuracy of dead-time compensation and current harmonics. It cannot be excluded, that the change of the time instant of additional measurements will give better results in the case of other low-pass filter parameters. Optimal choice of this time instant requires further investigation.

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