

# Resonant DC link inverters for AC motor drive systems – critical evaluation

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**Abstract.** In this survey paper, resonant and quasiresonant DC link inverters are reexamined for AC motor drive applications. Critical evaluation of representative topologies is based on simulation and waveform analysis to characterize current/voltage stress of components, control timing constraints and feasibility. A special concern over inverter common-mode voltage and voltage gradient  $du/dt$  limitation capacity is discussed for motor bearing and winding insulation safety. Experimental records of the laboratory developed parallel quasiresonant DC link inverter feeding induction motor confirm results of analysis. Comparative tables and simulation results demonstrate characteristic features of various schemes.

**Key words:** soft-switching, resonant DC link inverter, quasiresonant DC link inverter, common-mode voltages, voltage gradient, zero voltage switching.

## 1. Introduction

Soft switching techniques and circuits have been from the beginning integrated state-of-art of power electronics achievements [1–3]. Soft switching art is particularly demanded with implementation of wideband SiC and GaN power semiconductor devices for high frequency operation to reduce the switching loss and electromagnetic interference (EMI) emission [4]. In AC motor drive systems reliability investigations have pointed to common mode voltages and high  $du/dt$  generated by hard switching inverters as the cause of bearing damage and premature winding insulation faults. One of the solution to limit these problems is the concept of the auxiliary resonant commutated pole inverter (ARCPI) [5]. Recent achievements in control of current in resonant branch and design of resonant tank components [6–8] indicate a potential of efficiency improvement for this technique. However, the ARCPI features complexity with auxiliary resonant pole switches, diodes, inductors or coupled inductors, that are associated with each inverter phase leg.

The concept of resonant DC link inverter (RDCLI) with single resonant or quasi-resonant circuits inserted between the DC voltage source and the inverter is presented in Fig. 1. As a result of the resonant process, the inverter input voltage  $u_F$  is periodically and incessantly reduced to zero, creating zero voltage switching (ZVS) conditions for all inverter transistors. Alternatively, in quasiresonant circuits the resonant process is activated once per commutation of inverter switches. Since early RDCLI presentations in the late 1980s [9, 10] – various topologies have been intensively developed and experimentally tested, in order to respect objectives for AC motor drive systems. These are high efficiency and power density of converter fed drives. Recently, instead of using common mode chokes, transformers

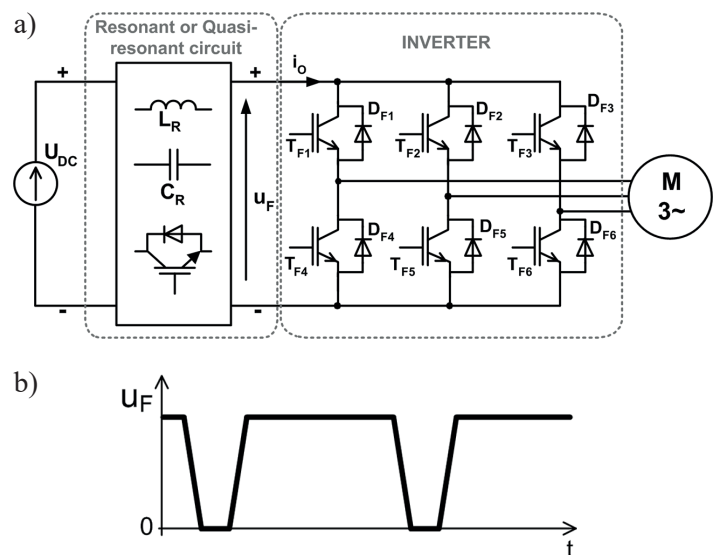


Fig. 1. Conception of the resonant DC link inverter: a) scheme, b)  $u_F$  voltage waveforms

and  $du/dt$  filters in hard switching converter – a motor friendly quasi-RDCLI has been proposed [11]. However, some previous comparative measurement of bearing currents and shaft voltages for hard- and soft-switching inverter excitation [12, 13] have not indicated clear superiority of inverters with resonant or quasi-resonant DC link. Moreover, they have not achieved better conversion efficiency. Still recent research results based on the SiC MOSFET modules demonstrate, that increasing switching frequency to hundreds of kHz brings out new quality in power efficiency & density of soft-switched inverters [14]. Therefore, the aim of this paper is a reexamination of selected indexes of performance of typical RDCLI/QRDCLI topologies addressed for AC motor drive systems. Comparative evaluation is based on simulation and analysis of power converter schemes in Saber program. At first, selected representative resonant or

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quasi-resonant DC link circuits are described by principle of operation. Then, simulation and experimental results are gathered in form of comparative tables and diagrams to demonstrate advantages and limitations of converter topologies.

## 2. Investigated topologies

**2.1. Basic resonant DC link inverter (BRDCLI).** The BRDCLI presented in Fig. 2a) consists of six switches and additional resonant inductor  $L_R$  constituting with resonant capacitor  $C_R$  a parallel resonant network [9]. Inverter input voltage  $u_F$  has a pulsating character that it is periodically reduced to zero during a period  $t_F$  providing a soft-switching of inverter transistors. When the resonant process occurs continuously and the load current  $I_O$  (Fig. 2b) is constant, then periods  $t_S$  and  $t_F$  (Fig. 2c) are also constant. The resonant inductor  $L_R$  is connected in series in the main DC voltage bus. Thus, the resonant inductor current  $i_{LR}$  is a sum of the load current  $I_O$  and the component of the resonant process between  $L_R$  and  $C_R$ . As a result, the maximum value of  $i_{LR}$  may be a few times higher than  $I_O$ .

The total energy accumulated in the resonant inductor  $L_R$  depends on the period  $t_F$  duration, when all inverter transistors are turned-on. When the period  $t_F$  ends, inverter transistors  $T_{F1} \div T_{F6}$  are switched to a new state (transistor  $T_F$  of an equivalent circuit in Fig. 2b is turned-off) and then energy is transferred from  $L_R$  to  $C_R$  causing increase of  $u_F$  voltage. The

maximum value of  $u_F$  strongly depends on  $I_O$  and at no-load conditions it may reach twice supply voltage  $U_{DC}$ . If the load transits from motor mode to a generation mode, the  $u_F$  voltage may be higher more than three times of  $U_{DC}$  value [15]. Therefore the BRDCLI may suffer from problematic control of  $u_F$  voltage maximum value as well as an increased current and voltage stress of inverter switches.

**2.2. Active clamped resonant DC-link inverter (ACRDCLI).** One of the way to improve BRDCLI features is an active – clamping of  $u_F$  voltage, as it is realized in the ACRDCLI [10]. It contains additional capacitor  $C_C$  and transistor  $T_1$  with parallel diode  $D_1$  (Fig. 3). At steady state, the mean value of inverter input voltage  $u_F = K \cdot U_{DC}$ , where  $K$  is a clamping factor. In practical applications,  $K \leq 1.3$  [10].

The resonant process occurs continuously with nearly constant duration of operational periods. If transistor  $T_1$  is not turned-on before current  $i_{LR}$  changes the direction in the period  $\langle t_1, t_2 \rangle$  (Fig. 3c), undesirable oscillations of  $u_F$  voltage will be initialized as a results of the resonance between  $L_R$  and  $C_R$ . The proposed ACRDCLI is generally dedicated to operation with sigma delta modulators, where moments of inverter transistors switching are correlated with  $t_4$ . The continuous  $i_{LR}$  current is a sum of the load current  $I_O$  and the component resulting from the resonant process. It means that the inductor  $L_R$  quality must be high in order to reduce the total energy losses [16]. A capacity of clamping capacitor  $C_C$  should be high enough

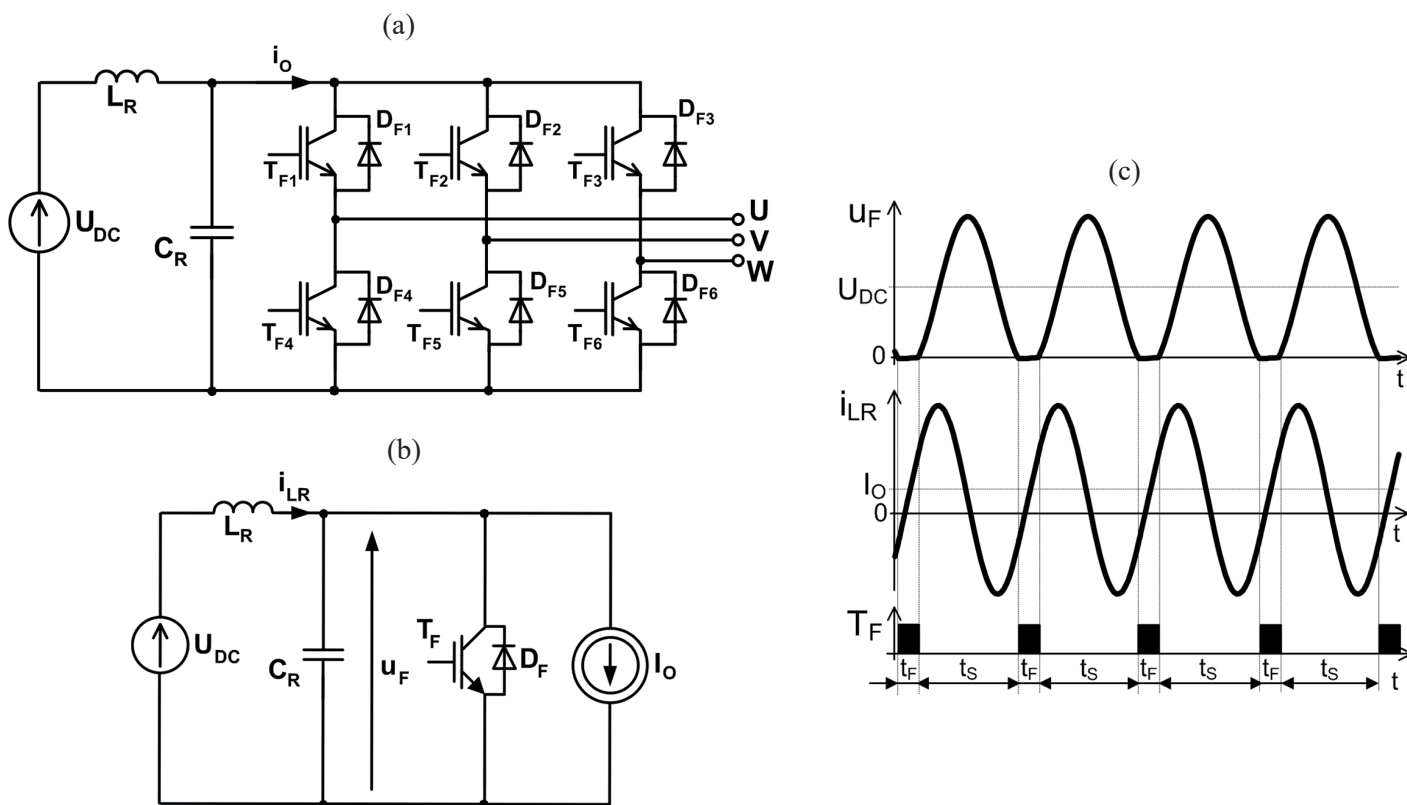


Fig. 2. a) BRDCLI scheme [9], b) equivalent circuit, c) typical transient waveforms

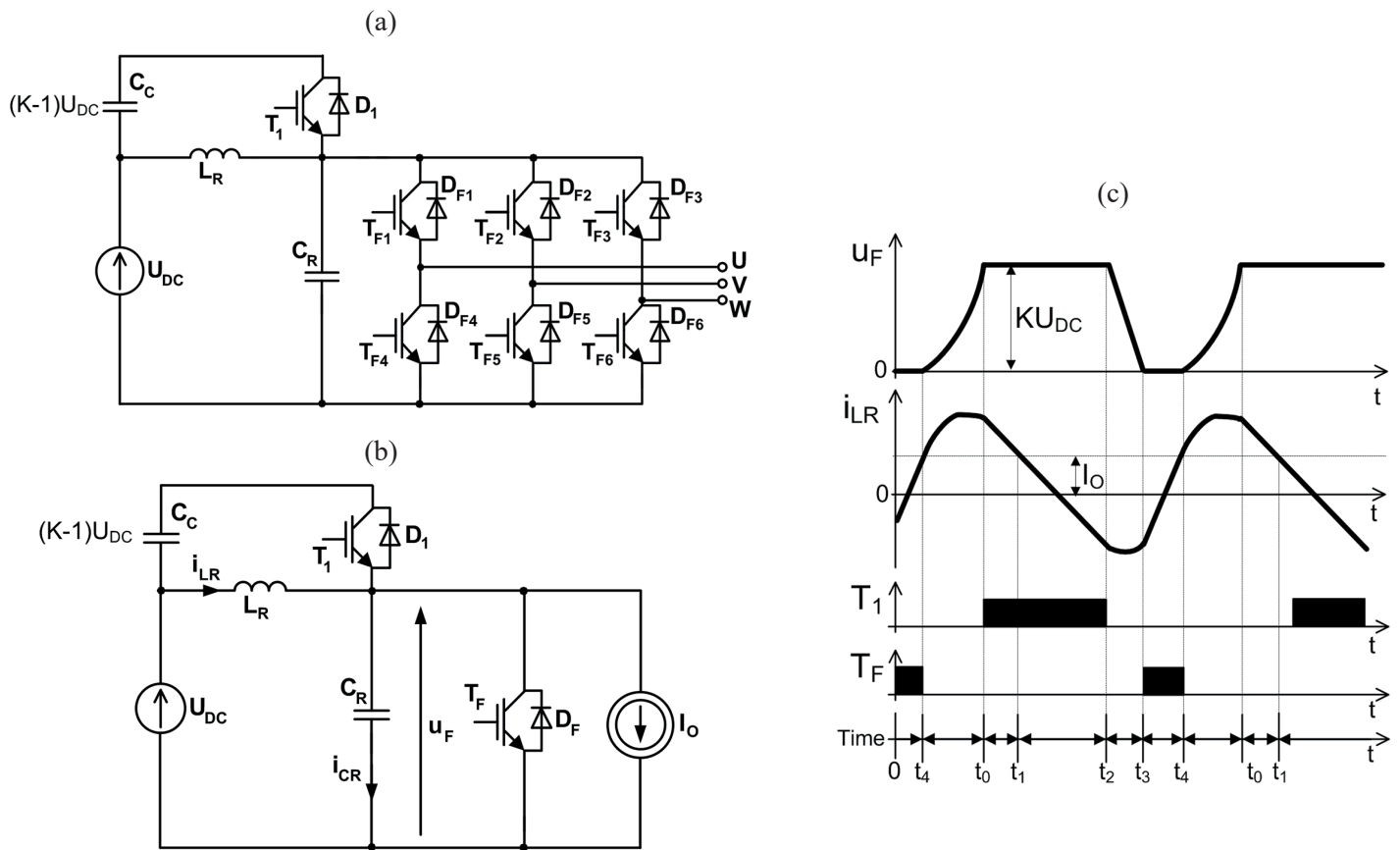


Fig. 3. a) ACRDCLI scheme [10], b) equivalent circuit, c) transient waveforms at positive load current  $I_O > 0$

(up to single mF) to ensure voltage stability. However, some problems with stability of  $C_C$  voltage may appear. Therefore, it is required to use an additional voltage regulator or modify the control algorithm. If the capacitor  $C_C$  is fully discharged, a proper operation is not possible. The capacitor  $C_C$  must be precharged before the ACRDCLI starts to operate [17]. Moreover, the ACRDCLI is sensitive to the clamp factor  $K$  changes. If inverter operates with a constant duration of period  $\langle t_0, t_2 \rangle$ , increase of the factor  $K$  by several percent results in disproportionate extension of  $u_F$  zero voltage state period (e.g. results from simulation test: duration of period  $\langle t_3, t_4 \rangle = 3 \mu s$  for  $K = 1.20$  and respectively, if  $K = 1.25$  the length of period  $\langle t_3, t_4 \rangle$  increases to  $4.1 \mu s$ ).

The total energy stored in magnetic field of the inductor  $L_R$  can be controlled by the length of period  $\langle t_3, t_4 \rangle$ , when inverter is short-circuited by turned-on transistors  $T_{F1} \div T_{F6}$ . Energy stored during this time interval has to be sufficient to ensure rebuilding of the  $u_F$  voltage during period  $\langle t_4, t_0 \rangle$  and allow to realize soft-switching conditions for the next switching cycle. During  $u_F$  zero voltage stage, current  $i_{LR}$  increases linearly until the moment  $t_4$ , when inverter transistors are switched to a new state. Maximum length of period  $\langle t_3, t_4 \rangle$  is limited by the maximum value of  $i_{LR}$  current, that does not allow to form a variable zero voltage duration. Control of the rate of change of input inverter voltage  $du_F/dt$  is limited to resonant circuit dimensioning.

**2.3. Active clamped quasi resonant DC-link inverter (ACQRDCLI).** In [18] and [19] a single resonant capacitor was replaced by six resonant capacitors  $C_R$  connected parallel to inverter transistors  $T_{F1} \div T_{F6}$  (Fig. 4). This topology inherits features of basic ACRDCLI, but the most significant modification refers to the control algorithm. Modulation scheme ensures execution of space vector pulse width modulation (SVPWM) vectors sequence: zero – active – active – zero during a single resonant cycle. The auxiliary transistor  $T_1$  is switched once for a modulation period and the resonance reduction of  $u_F$  voltage to zero is used to switch inverter transistors from zero voltage vector to an active vector. During the  $u_F$  zero voltage state,

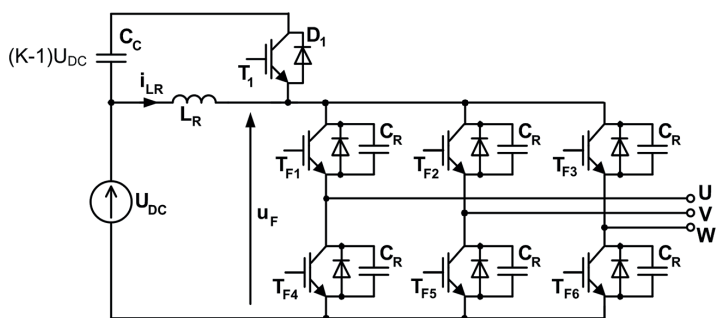


Fig. 4. ACRDCLI modification [18, 19]

the inverter is short-circuited by turned-on transistors of one selected inverter leg. It allows to store enough energy in  $L_R$  to perform resonant process for the next switching cycle.

Maximum energy efficiency of tested 30 kW inverter was 98.2%. However, correct execution of modulation scheme requires assumed direction of inverter output phase currents for each of particular voltage space vector sectors. For this reason, the proposed inverter was adapted to operate as a grid-connected inverter for the power factor angle between  $\pm\pi/6$ .

Another approach is presented in [20], where resonant circuit is formed by capacitor  $C_R$ , diode  $D_1$ , transistor  $T_1$  and coupled inductors  $L_{R1}$  and  $L_{R2}$  (Fig. 5a, b). Realization of a resonant cycle requires the flow of constant currents  $i_{LR1}$  and  $i_{LR2}$  in each of inductor between two resonant cycles (Fig. 5c). Sum of  $i_{LR1}$  and  $i_{LR2}$  current absolute values in period  $\langle 0, t_0 \rangle$  and for the time  $t > t_5$  have to be  $3-4 I_O$ . After turn-on of the transistor  $T_1$  at the moment  $t_3$ , current  $i_{LR1}$  should be high enough at the moment  $t_4$  to ensure rebuilding of  $u_F$  voltage to the  $U_{DC}$  value

and further discharge of the resonant capacitor  $C_R$  during next resonant cycle. However, this requirement limits the possibility of control  $du_F/dt$  when the load current  $I_O$  changes. The minimal length of  $u_F$  zero voltage period  $\langle t_1, t_4 \rangle$  is determined by the falling time of  $i_{LR2}$  current at the period  $\langle t_1, t_2 \rangle$  and the  $i_{LR1}$  current rise time during period  $\langle t_3, t_4 \rangle$ . The period  $\langle t_2, t_3 \rangle$  ends, when transistor  $T_1$  is turned – on at the moment  $t_3$  and this stage may be maintained for any time period. It allows to form variable zero voltage  $u_F$  duration stage. At the period  $\langle t_2, t_3 \rangle$ :  $i_{LR1}$  and  $i_{LR2}$  currents are reduced to zero increasing inverter efficiency. Due to the parasitic leakage inductances of  $L_{R1}$  winding, a high overvoltage may be induced at the transistor  $T_1$  turn-off. Additional snubber circuits or specially designed inductors with reduced leakage inductances have to be used.

**2.4. Passive clamped quasi resonant DC-link inverter (PCQRDCLI).** Clamping of  $u_F$  voltage may be realized by

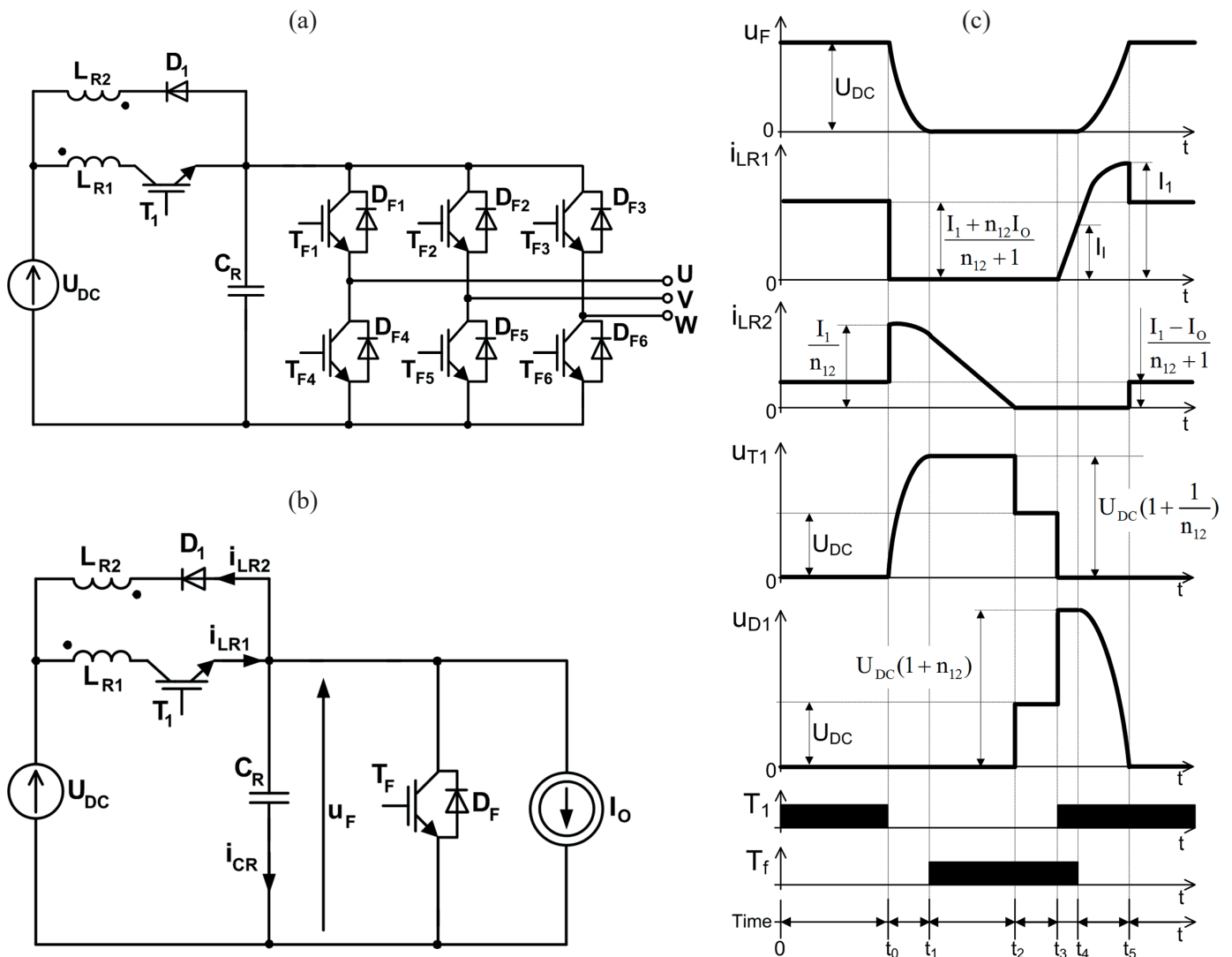


Fig. 5. ACQRDCLI with two coupled inductors [20]: a) scheme, b) equivalent circuit, c) transient waveforms at positive load current  $I_O > 0$ ,  $n_{12}$  – turns ratio  $L_{R1}:L_{R2}$

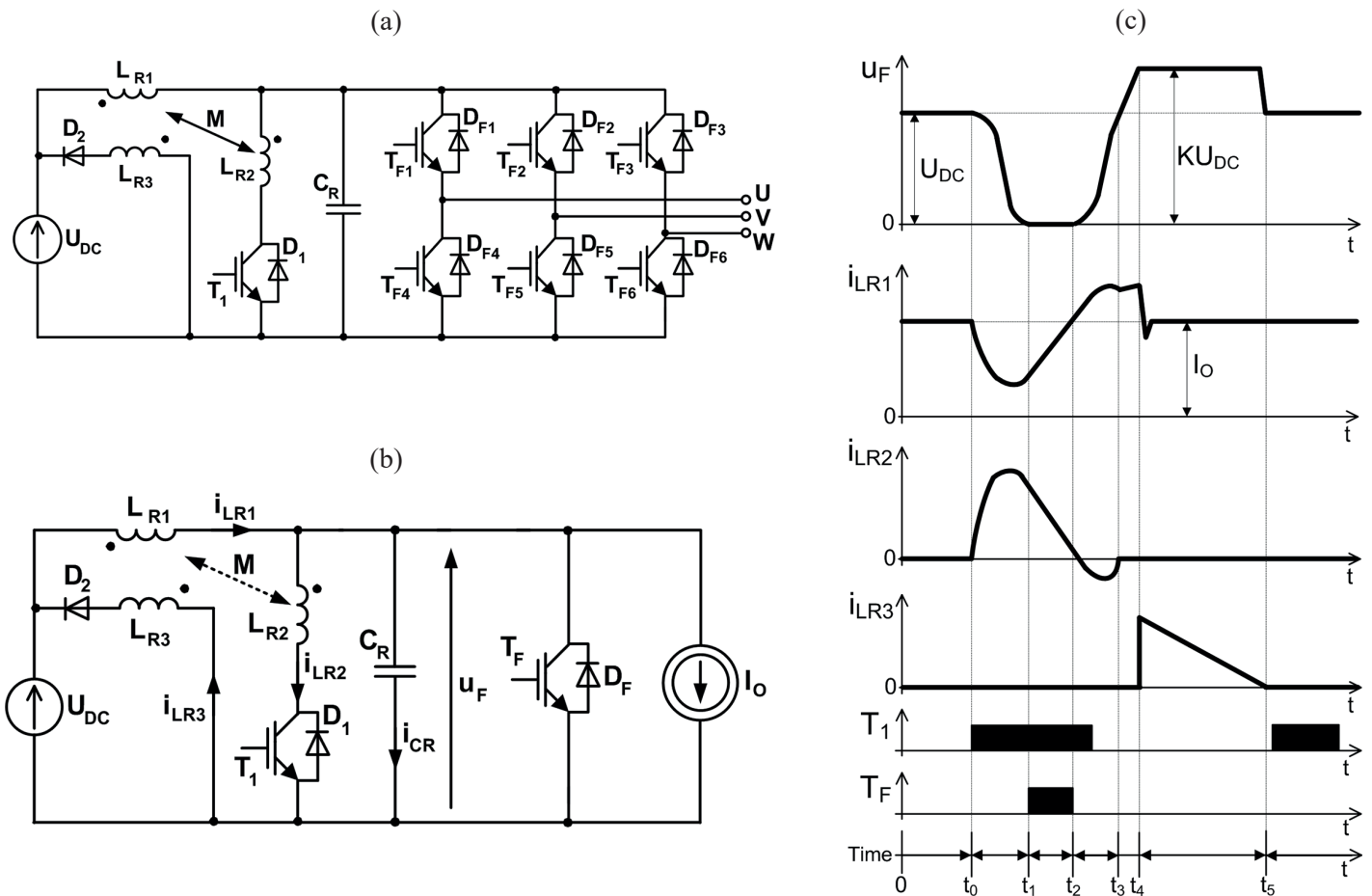


Fig. 6. PCQRDCLI [21, 22]: a) scheme, b) equivalent circuit, c) transient waveforms at positive load current  $I_O > 0$

using the PCQRDCLI [21]. The auxiliary transistor  $T_1$  is connected in series with the winding  $L_{R2}$  of the resonant inductor, which is composed of three coupled windings  $L_{R1}$ ,  $L_{R2}$  and  $L_{R3}$ . Additionally, windings  $L_{R1}$  and  $L_{R3}$  form a passive clamp transformer. The diode  $D_1$  is a parallel diode of transistor  $T_1$ , while a diode  $D_2$  connects windings  $L_{R3}$  with the voltage source  $U_{DC}$  (Fig. 6a, b). When  $u_F$  voltage reach value  $K \cdot U_{DC}$  at the moment  $t_4$  (Fig. 6c), diode  $D_2$  starts to conduct until moment  $t_5$ , enabling to return energy stored in inductor to the voltage source  $U_{DC}$ , what is an advantage over the active clamping method. Thus, the maximum value of  $u_F$  voltage is limited to  $K \cdot U_{DC}$ , but the maximum voltage stress for a single element is higher than  $K \cdot U_{DC}$  and for diode  $D_2$  it equals to  $U_{D2(max)} = K \cdot U_{DC} / (K-1)$ . For the time  $t > t_5$ ,  $u_F$  voltage is assumed to be constant, but as a result of resonance between  $L_{R1}$  and  $C_R$ ,  $u_F$  voltage oscillations were observed in [21]. The topology complexity level is high as a result of the inductor composed of three coupled windings. The correct inverter operation requires that  $L_{R1} > L_{R2}$ . Furthermore, windings are not loaded symmetrically – at the steady state between two resonant cycles, winding  $L_{R1}$  conducts the load current  $I_O$ , what generates additional losses, while windings  $L_{R2}$  and  $L_{R3}$  are only used during the resonant cycle. The clamp factor  $K$  is determined by the turns ratio between windings  $L_{R3}$  and  $L_{R1}$ .

Quality of the inductor should be high and this component design procedure is described in [22]. Control of  $du_F/dt$  value for rising and falling voltage slopes and duration of the  $u_F$  zero voltage period  $<t_1, t_2>$  is not possible. These values are determined by design of resonant circuit parameters and a value and flow direction of the load current  $I_O$ .

PCQRDCLI [12] still contains three inductances, but the inductor  $L_{R2}$  is not coupled with others windings (Fig. 7). Modification of resonant circuit structure is done by adding an auxiliary transistor  $T_2$  and diode  $D_2$ . Control of  $du_F/dt$  derivatives for the rising voltage slope is possible by the duration control

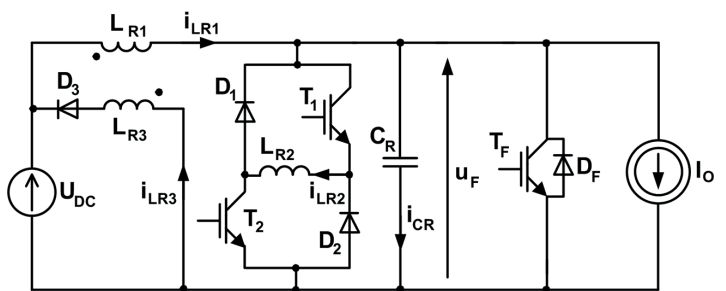


Fig. 7. Modification of the PCQRDCLI Link Inverter [12]

of  $u_F$  zero voltage period. The length of this period is determined by the turn-off moment of transistors pair  $T_1/T_2$ , what allows to control the resonant capacitor  $C_R$  charging current. Maximum length of the  $u_F$  zero voltage period is determined by the maximum permissible value of a  $L_{R1}$  winding current. Hence, the resonant  $u_F$  zero voltage state cannot be formed as variable duration inverter zero voltage vector.

**2.5. Parallel quasi resonant DC-link inverter (PQRDCLI).**

The PQRDCLIs use a transistor switch in series with the DC voltage bus, as in [23] (Fig. 8a). The resonant tank is formed by a resonant inductor  $L_R$ , resonant capacitor  $C_R$  and parallel snubber capacitors  $C_S$ . Snubber capacitors  $C_S$  may be replaced by an equivalent capacitor  $C_F = 3 \cdot C_S$  (Fig. 8b). Resonant capacitor  $C_R$  should be a few times higher than  $C_F$ . Correct realization of resonant cycle requires precise transistors switching moments to ensure ZVS for all inverter transistors. When the control algorithm with constant periods is implemented, the maximum of resonant inductor current  $i_{LR}$  is 2–3  $I_O$ . The current flow through resonant inductor  $L_R$  takes place only during the resonant cycle (Fig. 8c). At a steady state, between two resonant cycles,  $i_{LR} = 0$ . Using the appropriate control algorithm, inverter operation is performed with a zero mean value of  $i_{LR}$  current. The  $u_F$  zero voltage state cannot be variable due to inability to stop resonant cycle at the moment  $t_3$  (Fig. 8c). During period  $\langle t_0, t_1 \rangle$  sufficient energy to discharge  $u_F$  voltage do

zero has to be stored in a resonant tank. The  $du_F/dt$  derivative of the falling slope depends on  $i_{LR}$  value at the moment  $t_1$ .

When inverter transistors change state at the moment  $t_4$ , the value of load current  $I_O$  at the moment  $t_6$  may be much higher than at the moment  $t_0$  (eg. when the inverter state changes from zero to active vectors), then energy stored during period  $\langle t_0, t_1 \rangle$  may be insufficient to rebuild  $u_F$  voltage at the period  $\langle t_4, t_6 \rangle$ . Moreover, the  $du_F/dt$  control for the rising slope requires precise  $i_{LR}$  current estimation at the moment  $t_4$ . It means, that the full control of  $du_F/dt$  slopes is limited.

Modification of [23] as proposed in [11] by full separation of the DC voltage source allows reduction of a common-mode voltage amplitudes. Due to application of the second switch  $T_4/D_4$  in series with the DC power flow, the variable duration  $u_F$  zero voltage state is formed (Fig. 9). The zero voltage period ends when transistor  $T_F$  is turned-off at the time  $t = t_5$ . Before  $T_F$  is turned-off at the moment  $t_5$ , transistor  $T_3$  is switched-on at the moment  $t_4$ , what allows the resonant transfer of energy for rebuilding of  $u_F$  voltage during period  $\langle t_5, t_6 \rangle$ . During the period  $\langle t_3, t_4 \rangle$  total energy for  $u_F$  voltage rebuilding is stored in capacitor  $C_R$ . Maximum voltage stress of the transistor  $T_3$  equals to the maximum voltage of the resonant capacitor  $C_R$ .

The PQRDCLI [24] is an extension of [25] enabling full control of  $U_{C1}/U_{C2}$  voltage balance with variable duration  $u_F$  zero voltage state. Additional series switch  $T_4/D_4$  with auxiliary transistor  $T_3$  and parallel diode  $D_3$  are used (Fig. 10a).

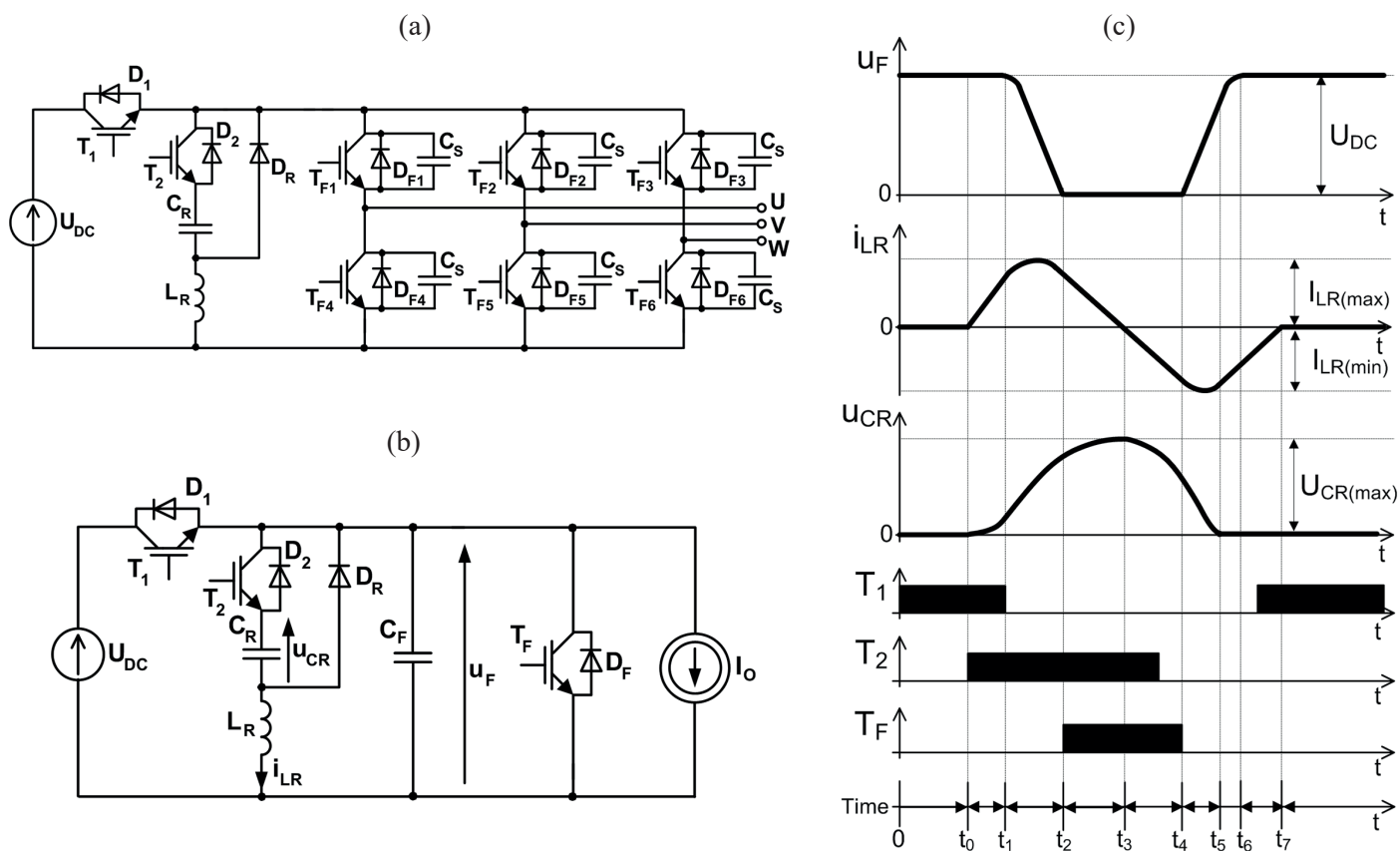


Fig. 8. PQRDCLI [23]: a) scheme, b) equivalent circuit, c) transient waveforms at positive load current  $I_O > 0$

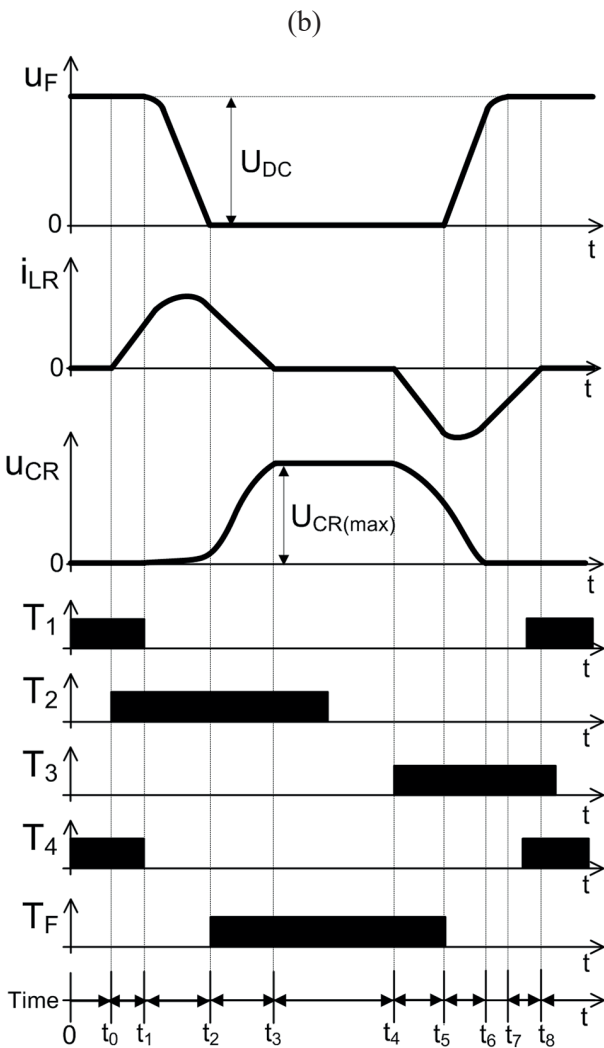
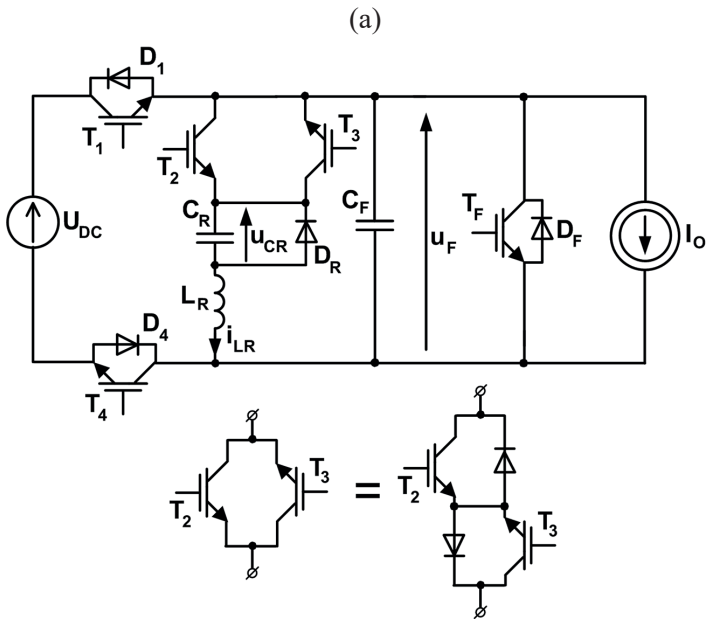


Fig. 9. PQRDCLI [11] with separation of DC voltage source: a) equivalent circuit scheme, b) transient waveforms at positive load current  $I_o > 0$

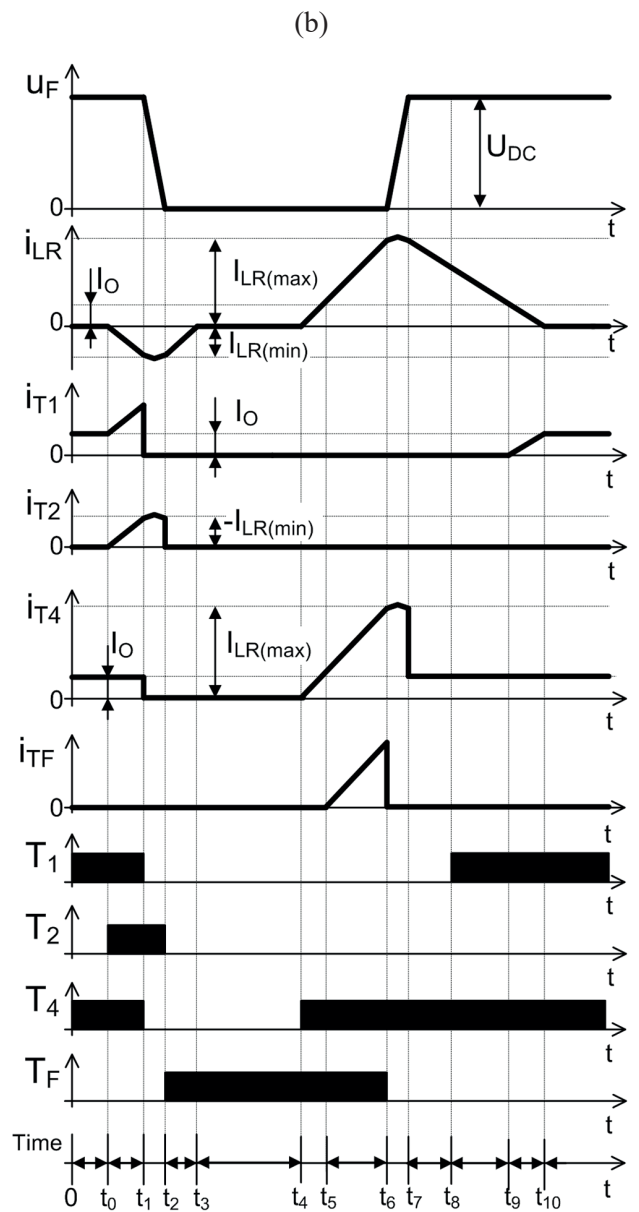
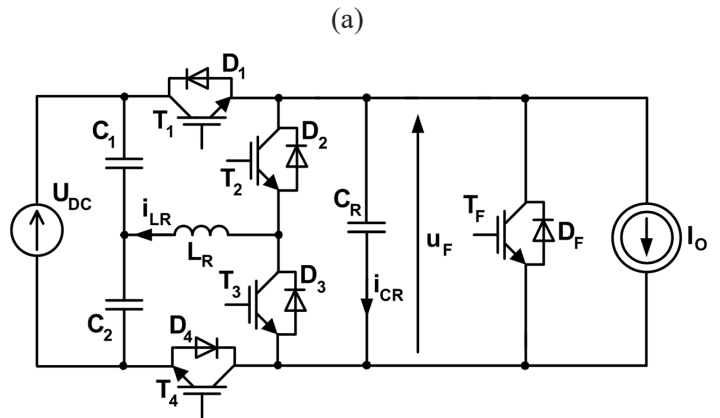


Fig. 10. PQRDCLI [24]: a) equivalent circuit, b) transient waveforms at positive load current  $I_o > 0$  for selected pair of transistors  $T_1/T_2$

A resonant cycle is performed by switching of transistor pairs  $T_1/T_2$  or  $T_3/T_4$ . The choice of switched transistor pairs depends on the actual measured values  $U_{C1}/U_{C2}$  and estimated charges flow for capacitors  $C_1$  and  $C_2$ . During  $u_F$  zero voltage state, the period  $\langle t_3, t_4 \rangle$  can be variable, allowing to form the zero voltage vector. This state ends when inverter transistors are switched to the new active state of inverter at the moment  $t_6$ . Transistor  $T_1$  or  $T_4$  is earlier turned-on at the moment  $t_5$  to store energy in the inductor  $L_R$ , for rebuilding the voltage  $u_F$  to the voltage-source value  $U_{DC}$ . During the period  $\langle t_3, t_4 \rangle$ , energy is stored in capacitors  $C_1/C_2$  and the inductor current  $i_{LR}$  equals to zero, what does not increase the energy losses. When inverter transistors are switched between two active states, transistor  $T_4$  remains turned-on and  $T_3$  is turned-off during a full resonant cycle, if a pair  $T_1/T_2$  is switched. Similarly, if  $T_3/T_4$  is switched,  $T_1$  remains turned-on and  $T_2$  is switched-off. When inverter transistors are switched from an inverter active state to a zero vector, transistors  $T_1/T_4$  are synchronously turned-off at ZVS conditions at the moment  $t_1$ . Return to the inverter active vector requires switching-on of transistor  $T_1$  or  $T_4$  under ZCS conditions at the moment  $t_4$  and the choice of the switched transistor depends on the  $U_{C1}/U_{C2}$  voltages balance requirements.

The  $i_{LR}$  current flows through the resonant inductor only in resonant cycle. Its mathematical description enables to estimate  $i_{LR}$  value in characteristic moments of the resonant cycle [26] improving timing precision, power efficiency and implementation of various control methods [26, 27].

### 3. Simulation and experimental results

Presented topologies were compared by simulation tests carried out by the Saber circuit simulator. Resonant circuit parameters, supply voltage and load current were used as in the original authors' papers to preserve their operation in predefined power ranges (Table 1). To realize resonant or quasi-resonant cycles at steady-state rated conditions – constant control timing were off-line calculated. In equivalent simulation circuits the inverter transistors were replaced by one transistor  $T_F$  and the load current  $I_O$  was modeled by a DC current source.

At first, for topologies with limited inherent control of  $du_F/dt$  slope their sensitivity to load current  $I_O$  changes was tested by simulation. In Fig. 11 per unit quantity of  $du_F/dt$  is

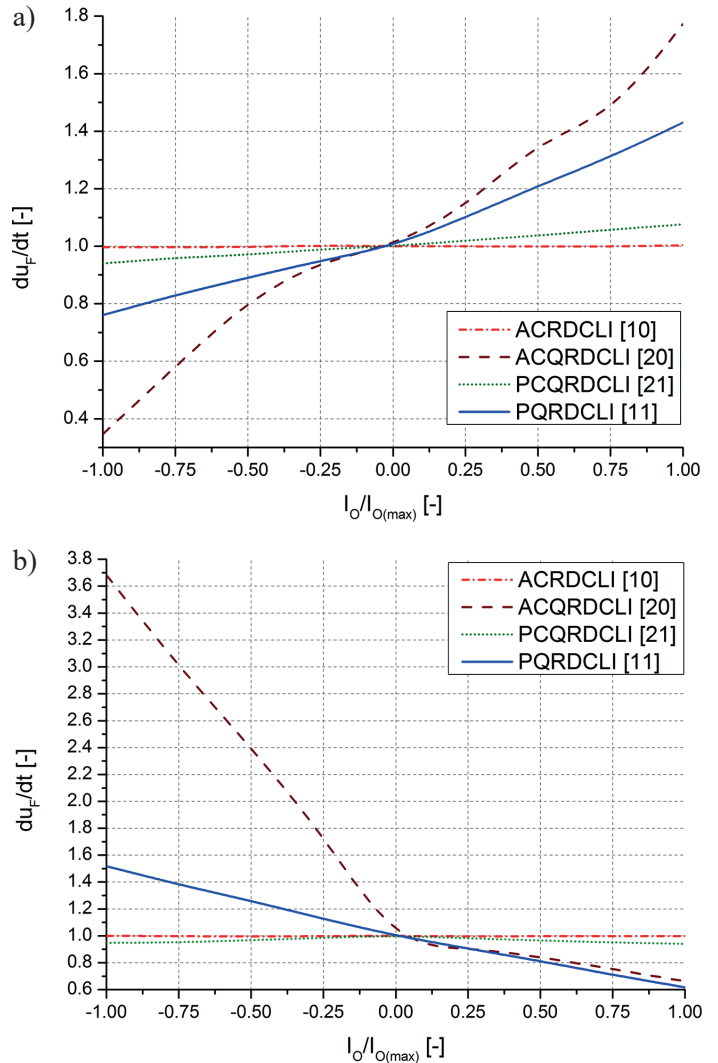


Fig. 11. Dependency of  $du_F/dt$  versus load current  $I_O$  referred to the  $du_F/dt$  for  $I_O = 0$ : a) falling slope, b) rising slope

referred to its base value obtained at zero load current, while per unit  $I_O/I_{O(max)}$  is referred to the maximal predefined load current  $I_{O(max)}$  of each tested inverter. For ACRDCLI [10], slope change  $du_F/dt$  is nearly constant and independent of load current. Similarly for the PCQRDCLI [21] – range of  $du_F/dt$

Table 1  
Parameters of tested topologies

ACRDCLI [10]	ACQRDCLI [20]	PCQRDCLI [21]	PQRDCLI [11]	PQRDCLI [24]
$L_R = 20.45 \mu\text{H}$ $C_R = 234 \text{ nF}$ $C_C = 2.2 \text{ nF}$ $K = 1.2$	$L_{R1} = 17 \mu\text{H}$ $k = 0.98$ $n_{12} = 2$ $C_R = 47 \text{ nF}$	$L_{R1} = 28.89 \mu\text{H}$ $L_{R2} = 11.8 \mu\text{H}$ $k = 0.9$ $n_{13} = 0.2$ $C_R = 50 \text{ nF}$ $K = 1.2$	$L_R = 30 \mu\text{H}$ $C_R = 470 \text{ nF}$ $C_F = 141 \text{ nF}$	$L_R = 10 \mu\text{H}$ $C_R = 220 \text{ nF}$ $C_1 = 4.7\text{mF}$ $C_2 = 4.7\text{mF}$
$P_N = 6.8 \text{ kW}$	$P_N = 3.5 \text{ kW}$	$P_N = 16 \text{ kW}$	$P_N = 8.8 \text{ kW}$	$P_N = 2.5 \text{ kW}$



changes for rising and falling slopes does not exceed 10%. For PQRDCLI [11]  $du_F/dt$  changes exceed 50%, but the highest sensitivity of  $du_F/dt$  is noted for ACQRDCLI [20] topology operating with the generator mode load. In PQRDCLI presented in [24], derivative  $du_F/dt$  is controlled independently for falling and rising  $u_F$  voltage slopes and can be regulated constant regardless of value and direction of load current  $I_O$  (Fig. 12).

Selected results of compared topologies:  $du_F/dt$  at no load,  $t_F$  – zero voltage  $u_F$  period, maximal inductor current  $I_{LR(max)}$  and maximal voltage stress of resonant circuit components  $U_{(max)}$  are presented in Table 2. For ACRDCLI [10] inverter input voltage  $u_F$  at a steady state is higher than supply voltage  $U_{DC}$ , what enables to reduce a negative influence of  $u_F$  zero voltage intervals on the inverter output voltage [28]. Maximal voltage stress of resonant circuit components was obtained for the PCQRDCLI [21], where the maximal voltage across the diode reached  $6 \cdot U_{DC}$ .

Model of resonant circuit with complete two-level bridge inverter used for simulation of the common-mode voltage  $u_{N-PE}$  and the input inverter voltage  $u_F$  is depicted in Fig. 13. The star connected capacitors  $C_d$  ( $3 \times 10$  nF) provided the common mode voltage  $u_{N-PE}$  between inverter output phases and the ground potential. The bus capacitances  $C_{PE} = 75$  nF and the

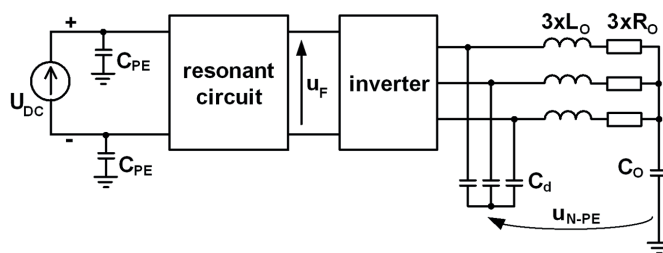


Fig.13. Simulation circuit for  $u_{N-PE}$  and  $u_F$  waveforms

ground capacitance  $C_O = 2.250$  nF were based on laboratory measurement of AC motor drive system. The DC source voltage  $U_{DC} = 230$  V.

Simulation results indicate significant reduction of common mode voltage  $u_{N-PE}$  levels of the PQRDCLI [11]. At active vector sequences of two-level inverter  $u_{N-PE} = \pm U_{DC}/6$ . At zero vector state,  $u_{N-PE}$  is reduced to zero (Fig. 14b) due to isolation of the source voltage from DC link bus. For other topologies, each resonant reduction of the  $u_F$  to zero state triggers the  $u_{N-PE}$  to  $-U_{DC}/2$ . When in PDM/PWM operation the singular zero vector state ‘000’ is applied, then the upper  $u_{N-PE}$  level amounting  $U_{DC}/2$  is eliminated (Fig. 14a). In the ACRDCLI [10], switching frequency of the input inverter voltage  $u_F$  is maximal, equal to the resonant DC-link circuit operation. In quasiresonant schemes switching frequency of the input inverter voltage  $u_F$  is decreased and synchronized to the switching frequency of inverter states. In [29] a shifted space vector pulse width modulation method was proposed to reduce necessary inverter state changes to only one for the pulse width modulation period.

In the laboratory setup of PQRDCLI [24] with induction motor load (Fig. 15) selected current and voltage waveforms were recorded to verify simulation results. Turn on of series DC link transistors:  $T_1$  and  $T_4$  enabled a comparison with conventional hard switched two-level inverter operation. In Fig. 16 are depicted ground leakage current  $i_{PE}$  and common-mode inverter voltage  $u_{N-PE}$  waveforms. It is evident of the  $i_{PE}$  spikes attenuation in quasi resonant switching. The  $u_{N-PE}$  amplitudes corresponding to soft-switching are consistent with Table 3 range, except that in hard switching mode the zero state ‘111’ is used increasing the  $u_{N-PE}$  amplitude ( $+U_{DC}/2$ ,  $U_{DC} = 230$  V).

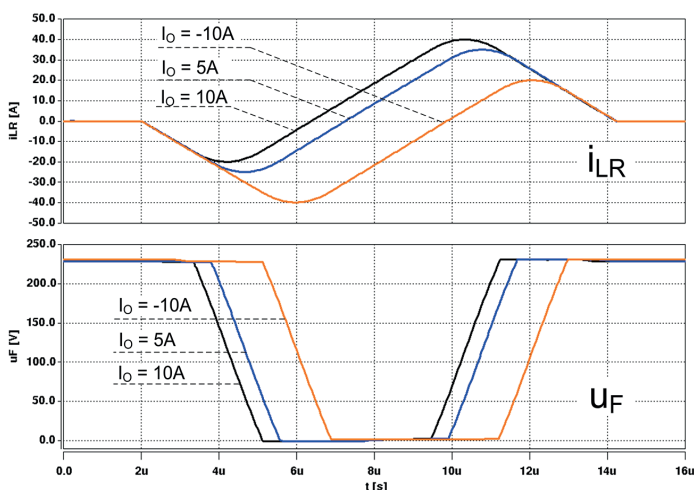


Fig. 12. Voltage  $u_F$  and current  $i_{LR}$  of the PQRDCLI [24] for various loading condition

Table 2  
Simulation results of tested topologies

Topology		ACRDCLI [10]	ACQRDCLI [20]	PCQRDCLI [21]	PQRDCLI [11]	PQRDCLI [24]	Unit
Parameter	falling	-140	-400	-500	-310	-130	V/ $\mu$ s
	rising	90	870	320	330	130	V/ $\mu$ s
$t_F$ [ $\mu$ s]		2.60	8.16	0.48	7.50	4.25	$\mu$ s
$I_{LR(max)}/I_O$		2.0	2.8	3.60	3.25	2.75	–
$U_{(max)}/U_{DC}$		1.2	3.0	6.0	1.0	1.0	–

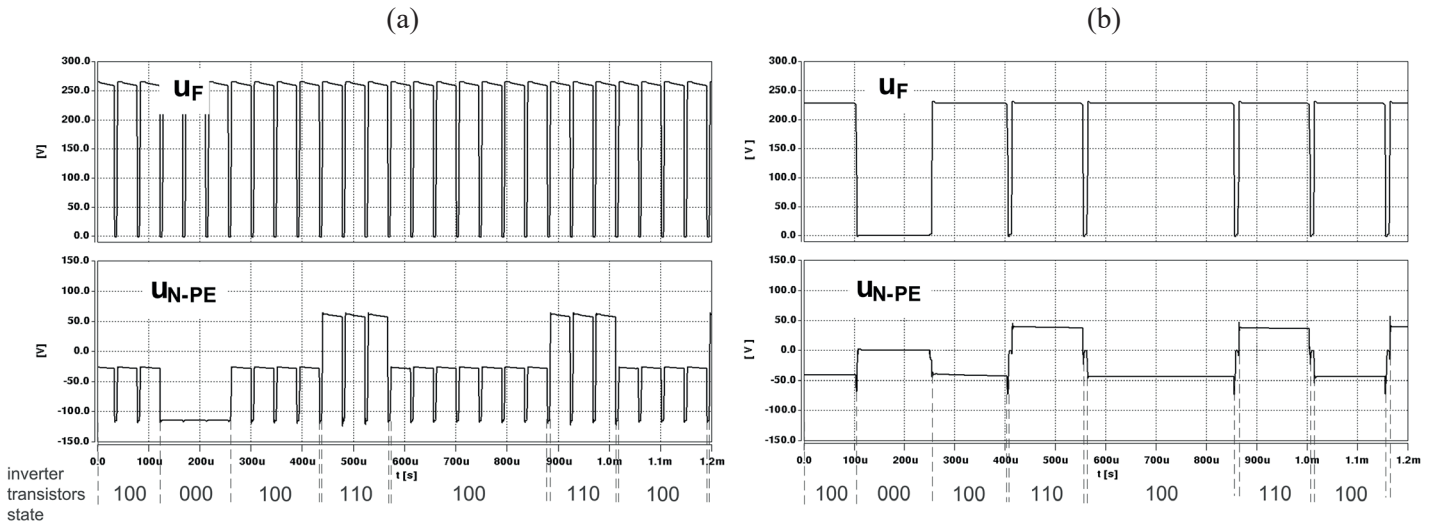


Fig. 14. Input inverter  $u_F$  and common-mode  $u_{N-PE}$  voltage waveforms ( $U_{DC} = 230\text{ V}$ ): a) ACRDCLI [10], b) PQRDCLI [11].

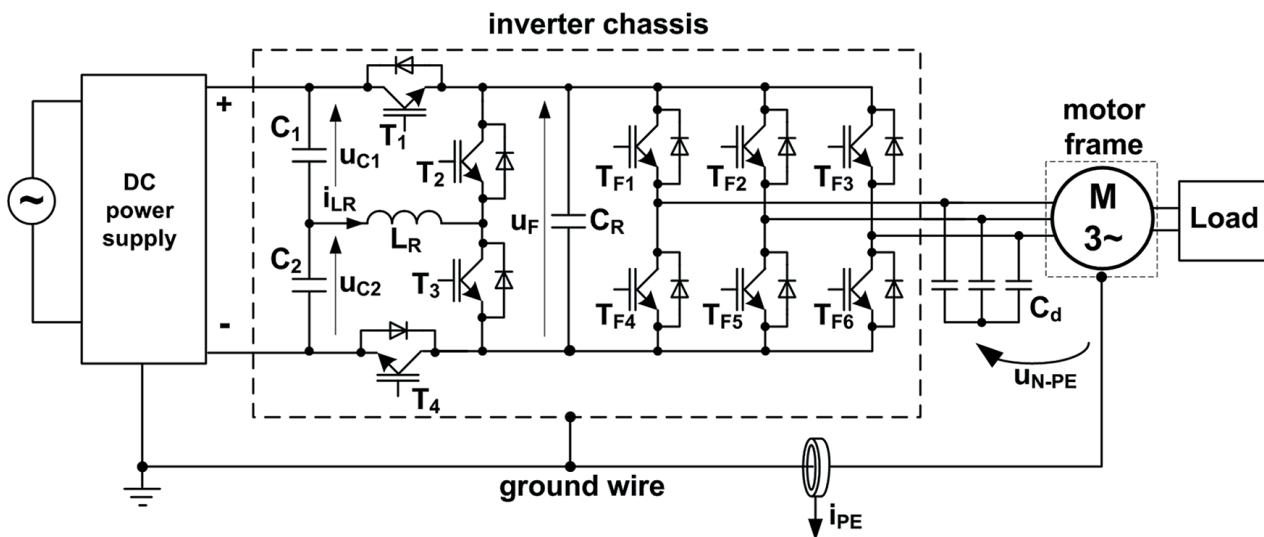


Fig. 15. Laboratory setup for experimental tests

Table 3  
Main features of compared topologies

Topology	Hard switching	ACRDCLI [10]	ACQRDCLI [20]	PCQRDCLI [21]	PQRDCLI [23]	PQRDCLI [11]	PQRDCLI [24]
Number of resonant circuit transistors	0	1	1	1	2	4	4
Commutation	Hard switching	ZVS	ZVS/ZCS	ZVS/ZCS	ZVS/ZCS	ZVS/ZCS	ZVS/ZCS
Voltage control	PDM/PWM	PDM	PDM/PWM	PDM/PWM	PDM/PWM	PDM/PWM	PDM/PWM
Energy stored in a resonant tank	–	Yes	Yes	No	No	Yes <sup>*)</sup>	No
Inverter input voltage $u_F/U_{DC}$	1	K	1	1	1	1	1
Variable duration of zero voltage $u_F$	No	No	Yes	No	No	Yes	Yes
Control of $du_F/dt$	No	Yes	Limit	Yes	Limit	Limit	Yes
Common mode voltage $u_{N-PE}/U_{DC}$	min	-1/2	-1/2	-1/2	-1/2	-1/6	-1/2
	max <sup>**)</sup>	1/6	(4K-3)/6	1/6	(4K-3)/6	1/6	1/6

<sup>\*)</sup> during forming the zero voltage vector, <sup>\*\*) when the singular zero vector '000' is applied.</sup>

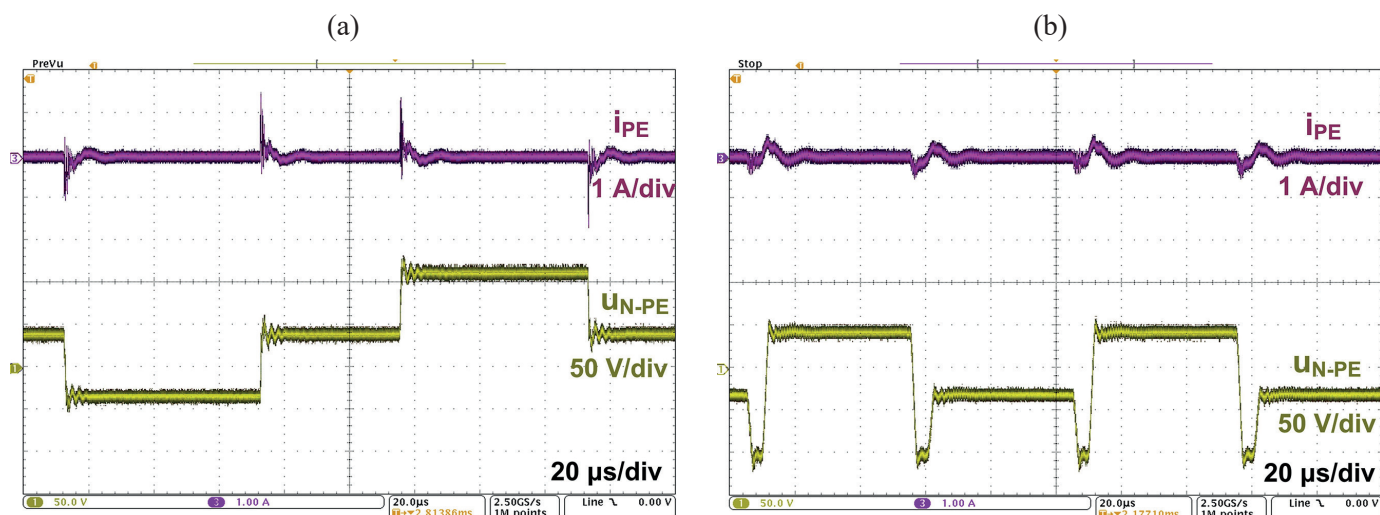


Fig. 16. Experimental waveforms of CM voltage  $u_{N-PE}$  and ground leakage current  $i_{PE}$ : a) hard switching, b) PQRDCLI [24] operation

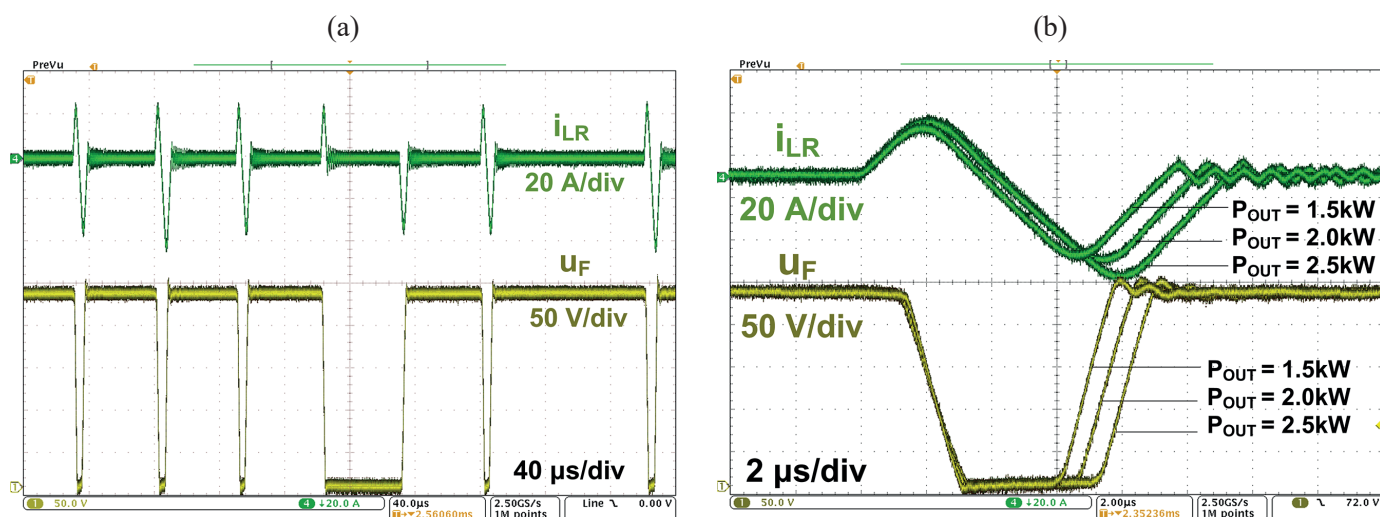


Fig. 17. Voltage  $u_F$  and current  $i_{LR}$  at PQRDCLI [24] operation: a) variable duration of zero vector, b) stabilization of  $du_F/dt$  independent of load

Variable duration of zero state is proved in Fig. 17a with inductor current  $i_{LR}$  and input voltage  $u_F$  transients at resonant zero notches of inverter commutation and prolonged zero vector state. In Fig. 17b is presented ability of  $du_F/dt$  stabilization, that is independent of loading conditions.

#### 4. Conclusions

Survey of representative resonant and quasiresonant DC link circuits has demonstrated features of compared topologies (Table 3). All investigated circuits ensure ZVS/ZCS commutation conditions of inverter switches, that are particularly desired for high frequency switching and power density indexes of AC motor drives.

Resonant zero notches of DC link voltage during inverter operation attenuate high voltage gradients of all inverter pulse

voltages. Thus, harmful EMI effects including ground leakage currents are limited at the excitation source without need of auxiliary voltage gradient filters. Stabilization of voltage gradient in function of load current is assured by the PQRDCLI [24] and [25]. In other cases, only PCQRDCLI [21] and ACRDCLI [10] topologies indicated its low sensitivity to load changing conditions. However in most configurations, zero notches of DC link voltage  $u_F$  increase common mode high frequency voltage amplitudes  $u_{N-PE}$  that may cause an increase of the electrical discharge machining (EDM) bearing currents in AC motor drive systems.

Significant attenuation of  $u_{N-PE}$  has been achieved in the PQRDCLI [11] at the cost of two transistor switches connected in series in the main the DC link power flow and isolating voltage source from DC link bus. Instead of insulating transistor switches, ACRDCLI topologies possessing series inductor in DC supply line offer boost of inverter voltage, which is advanta-

geous in full voltage exploitation for AC motor control. In view of above features and recent progress of field-programmable gate arrays enabling precise timing control of resonant circuit modes, resonant and quasiresonant DC link inverters seem to be a promising alternative to hard switching operation of conventional inverters in high switching frequency applications.

## REFERENCES

- [1] M.D. Bellar, T.S. Wu, A. Tchamdjou, J. Mahdavi, and M. Ehsani, "A review of soft-switched DC-AC converters," *IEEE Trans. Ind. Appl.*, 34 (4), 847–860 (1998).
- [2] B.K. Bose, "Need a Switch?," *IEEE Ind. Electron. Mag.*, 1 (4), 30–39 (2007).
- [3] S.J.V. Bright, S. Ramkumar, and H. Anand, "Positive output elementary Luo converter for fixed-frequency ZVS operation," *Bull. Pol. Ac.: Tech.*, 65 (2), 255–262 (2017).
- [4] A. Chub, J. Rabkowski, A. Blinov, and D. Vinnikov, "Study on power losses of the full soft-switching current-fed DC/DC converter with Si and GaN devices," in *IECON 2015 – 41st Annual Conference of the IEEE Industrial Electronics Society*, 13–18 (2015).
- [5] R.W.D. Doncker and J.P. Lyons, "The auxiliary resonant commutated pole converter," in *Conference Record of the 1990 IEEE Industry Applications Society Annual Meeting*, 1228–1235 (1990).
- [6] W. Yu, J.S. Lai, and S.Y. Park, "An Improved Zero-Voltage-Switching Inverter Using Two Coupled Magnetics In One Resonant Pole," in *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, 401–406 (2009).
- [7] S. Karyś, "Three-phase soft-switching inverter with coupled inductors, experimental results," *Bull. Pol. Ac.: Tech.*, 59 (4), 535–539 (2011).
- [8] S. Karyś, "Advanced control and design methods of the auxiliary resonant commutated pole inverter," *Bull. Pol. Ac.: Tech.*, 63 (2), 489–494 (2015).
- [9] D.M. Divan, "The resonant DC link converter—a new concept in static power conversion," *IEEE Trans. Ind. Appl.*, 25 (2), 317–325 (1989).
- [10] D.M. Divan and G. Skibinski, "Zero-switching-loss inverters for high-power applications," *IEEE Trans. Ind. Appl.*, 25 (4), 634–643 (1989).
- [11] J. Kedariseti and P. Mutschler, "A Motor-Friendly Quasi-Resonant DC-Link Inverter With Lossless Variable Zero-Voltage Duration," *IEEE Trans. Power Electron.*, 27 (5), 2613–2622 (2012).
- [12] S. Chen and T.A. Lipo, "Bearing currents and shaft voltages of an induction motor under hard- and soft-switching inverter excitation," *IEEE Trans. Ind. Appl.*, 34 (5), 1042–1048 (1998).
- [13] S. Bhattacharya, L. Resta, D.M. Divan, and D.W. Novotny, "Experimental comparison of motor bearing currents with PWM hard and soft-switched voltage-source inverters," *IEEE Trans. Power Electron.*, 14 (3), 552–562 (1999).
- [14] N. He, Y. Li, C. Du, C. Liu, C. Hu, and D. Xu, "SiC MOSFET zero-voltage-switching SVM controlled three-phase grid inverter," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 1–8 (2016).
- [15] T.W. Ching, "Soft-switching Converters for Electric Vehicle Propulsion," *J. Asian Electr. Veh.*, 5 (2), 1019–1026 (2007).
- [16] C. Du, W.G. Hurley, and D. Xu, "Design Methodology of Resonant Inductor in a ZVS Inverter," *IEEE J. Emerg. Sel. Top. Power Electron.*, 3 (4), 1142–1150 (2015).
- [17] Z. Hong, R. Duke, and S.D. Round, "A Resonant DC Link Inverter for an Electric Vehicle," *J. Electr. Electron. Eng. Aust.*, 21 (1), 65–71 (2001).
- [18] R. Li and D. Xu, "A Zero-Voltage Switching Three-Phase Inverter," *IEEE Trans. Power Electron.*, 29 (3), 1200–1210 (2014).
- [19] C. Du, D. Xu, N. He, and N. Zhu, "Modeling and Optimization of a Zero-Voltage Switching Inverter for High Efficiency and Miniaturization," *IEEE Trans. Power Electron.*, 32 (1), 150–163 (2017).
- [20] M.R. Amini and H. Farzanehfar, "Three-Phase Soft-Switching Inverter With Minimum Components," *IEEE Trans. Ind. Electron.*, 58 (6), 2258–2264 (2011).
- [21] S. Chen and T.A. Lipo, "A novel soft-switched PWM inverter for AC motor drives," *IEEE Trans. Power Electron.*, 11 (4), 653–659 (1996).
- [22] S. Chen, B.J.C. Filho, and T.A. Lipo, "Design and implementation of a passively clamped quasi resonant DC link inverter," in *Conference Record of the 1995 IEEE Industry Applications Conference, 1995. Thirtieth IAS Annual Meeting, IAS '95*, 2387–2392 (1995).
- [23] J.-W. Choi and S.-K. Sul, "Resonant link bidirectional power converter. I. Resonant circuit," *IEEE Trans. Power Electron.*, 10 (4), 479–484 (1995).
- [24] M. Turzyński, P.J. Chrzan, M. Kolincio, and S. Burkiewicz, "Quasi-resonant DC-link voltage inverter with enhanced zero-voltage switching control," in *2017 19th European Conference on Power Electronics and Applications (2017)*.
- [25] S. Mandrek and P.J. Chrzan, "Quasi-Resonant DC-Link Inverter With a Reduced Number of Active Elements," *IEEE Trans. Ind. Electron.*, 54 (4), 2088–2094 (2007).
- [26] M. Turzyński, P. Banach, P. Murawski, R. Pepliński, and P.J. Chrzan, "A predictive estimation based control strategy for a quasi-resonant dc-link inverter," *Bull. Pol. Ac.: Tech.*, 61 (4), 757–762 (2014).
- [27] S. Mandrek and P.J. Chrzan, "Control strategies of the quasi-resonant DC-link inverter," in *2008 13th International Power Electronics and Motion Control Conference*, 144–147 (2008).
- [28] S. Pan and J. Pan, "A Novel Zero-Voltage Switching Resonant Pole Inverter," in *2006 CES/IEEE 5th International Power Electronics and Motion Control Conference*, 1–5 (2006).
- [29] S. Pan, J. Pan, and Z. Tian, "A Shifted SVPWM Method to Control DC-Link Resonant Inverters and Its FPGA Realization," *IEEE Trans. Ind. Electron.*, 59 (9), 3383–3391 (2012).