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The structure and the Space Vector Modulation for a Medium Voltage Power-Electronic-Transformer based on two seven-level Cascade H-Bridge inverters

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Abstract: This paper presents the structure and the Space Vector Modulation (SVPWM) for Power Electronic Transformer (PET) based on two seven-level Cascade H-Bridge (CHB) inverters. The DC-links of CHB inverters are coupled with nine Dual-Active Bridge (DAB) converters with Medium Frequency (MF) transformers. The DC-link voltages are equalized with two methods –through the control of DAB voltages and through the modulation strategy applied to both CHB inverters. In the proposed SVPWM, the influence of vector sequences on predicted DC-link voltages is analysed and optimum vector sequence is selected in order to equalize them. Regardless of this, the proposed SVPWM strategy enables proper generation of output voltage vector also in the case of DC-link voltage imbalance - the calculation of the space-vector area takes into consideration the inequality of the DC-link voltages and its influence on the lengths and positions of active vectors. In order to simplify the modulation algorithm, the ML CHB inverter is considered as a set of three-level inverters connected in series. Each of them is controlled using the same SVPWM algorithm. The proposed modulation method reuses the H-Bridges with zero duty cycles determined in the initial stages of output voltage generation process. This enables optimal management of the DC-link voltage distribution. The experimental research was carried out on a 600 kW/ 3.3 kV PET. The results are presented in this paper.

1. Introduction

The Power Electronic Transformer (PET) is composed of a power electronic converter and a medium/high frequency isolation transformer [24]. The advantages of PET such as reduced weight / volume, flexibly power flow control, reactive power regulation, improved power quality and increased reliability make this solution widely used in place of classic transformers in modern power systems [1], [26], [51]. The structure of PET in high-power and medium-voltage (MV) applications is usually based on the modular multilevel (ML) converters due to the advantages of modular structure [2], [27]. In such PETs, the energy is usually transferred using Dual-Active H-Bridges (DABs) and medium/high frequency transformers [18], [20], [21], [22]. The active front converters used to construct the MV PETs witch are based on multilevel Voltage-Source Inverter topology are usually Modular Multilevel Converters (MMC) [49], [54] and Cascade H-Bridge converters (CHB) [19], [22], [52]. The research on PET control methods refers to the optimization of the work and control methods of the DABs [45] as well as fault-tolerant control [50]. The vast majority of papers show the methods for balancing the DC-link voltages [23], [25], [46], [47], [53], [54].

One of the most interesting PET structures are based on two active-front CHB inverters. This kind of inverter allows for increasing their output voltages by adding consecutive H-Bridges to inverter topology while the single H-Bridge is built of low blocking-voltage transistors. The introduction of additional levels to the CHB inverter structure allows to obtain voltage waveforms in a shape closer to sinusoid, with less harmonics content compared to two-level converters. The CHB inverters are utilised not only in PET applications [2], [26], [27]. They are commonly used in Static Synchronous Compensator (STATCOM) [3], [4], Energy Storage Systems [5], [6], [28], for the integration of Renewable Generation Systems [7], [8], [29] as well as in electric drive applications [30], [31].

In the ML inverters, regardless of their structure, it is necessary to balance the voltages on DC-link capacitors. The inverter output voltage significantly exceeds the blocking voltage of the transistors so the DC-link voltages should be maintained at the same level. Balancing the DC-link voltages is relatively difficult in CHB inverters. Even when the DC-link voltages are balanced they will not be constant because the legs of a cascaded H-bridge converter are single phase and are subject to power pulsations at twice the fundamental frequency [32]. The fluctuations of DC-link voltages make it difficult to develop Space Vector Pulse Width Modulation (SVPWM) strategies because the length and position of active vectors vary depending of the DC-link voltages [9], [10]. The additional difficulty is locating the reference voltage vector in non-regular hexagon with different size sub-triangles and variable section borders. The problem of correct generation of output voltages is particularly visible in SVPWM controlled inverters with a number of levels greater than three. This causes, that the most popular modulation strategies used in ML CHB inverters are carrier-based Sinusoidal Pulse Width Modulations (SPWMs) [7], [33], [34], [35] and non-carrier-based Selective-Harmonic-Elimination Pulse Width Modulations (SHE-PWMs) [11], [12], [36], [37].

The SPWM strategies for an *n*-level ML inverter utilize the sinusoidal reference waveform and '*n*-1' carriers shifted vertically (Level-Shifted PWM (LS-PWM)) [33],[34], [35] or horizontally (Phase-Shifted PWM (PS-PWM)) [7], [13], [29], [38]. The SHE-PWM strategy is based on staircase waveform generation. The conducting angles are chosen such that the total harmonic distortion of output voltage is minimum [12].

The DC-link voltage balancing strategies for CHB inverters generally relate to the modulation strategies. The

main advantage of PS-PWM is its ability to equalize the power distribution among the H-Bridges and consequently to balance their DC-link voltages. The DC-link voltages can be equalized by sharing the reference voltage between the H-Bridges [14] or by modifying their modulation indexes [39]. The same effect can be obtained in CHB inverters with LS-PWM, where the carrier signals rotate between the H-Bridges for every modulation cycle [40]. By managing the H-bridges which take part in the modulation, it is also possible to balance the DC-link voltages in the CHB inverter with SHE-PWM [11].

The SVPWM strategies for ML CHB converters usually utilize the three nearest space vectors defining the sector where the reference voltage vector is located [10]. The location of the reference voltage is usually considered for the area covering all obtainable active vectors. The fractional parts of normalized on-time durations [10] or normalized reference voltage [15], [41] are utilized to determine the transistor on-times for three H-Bridges, where the output voltages are modulated. The integers are used to indicate the positively or negatively connected H-Bridges where the output voltages are equal to ± DC-link voltage. In some solutions, the space vector hexagon is decomposed into two-level space vector hexagons to simplify the modulation algorithm and to reduce computational efforts [16], [17], [42].

The DC-link voltage balancing methods for CHB inverters with SVPWM strategies usually exploit an additional degree of redundancy internal to the phase legs. The DC link voltages within each phase are equalized by appropriate selection of negatively or positively connected H-Bridges. The choice of H-Bridges used to generate the output voltage depends on desired changes in DC-link voltages and the direction of the phase current [32] or power [23], [43], [44]. This is achieved by carrying out an ordering (via a sorting algorithm) of the capacitor voltages during each control period [23], [44].

Each leg of a CHB inverter is a single phase converter subject to power pulsations at twice the fundamental frequency. As a result, the DC-link voltages in different inverter legs cannot be equalized in this way and the DC-link voltage fluctuations may affect the accuracy of output voltage generation. The changes in output voltage caused by the DC-link voltage ripples can be determined and compensated as shown in [32]. The method proposed in [10] allows for mapping the reference voltage vector to the complex plane, where the coordinates change automatically with fluctuations of DC voltages. This approach allows to generate the output voltages correctly also in the case of DC-link voltage unbalance.

In this paper, the structure and SVPWM method for a Power-Electronic-Transformer based on two seven-level Cascade H-Bridge inverters is proposed. The DC-links of CHB inverters are coupled with nine Dual-Active Bridge (DAB) converters with Medium Frequency (MF) transformers. Appropriate interleaving of couplings made it possible to balance the load of individual phases of both inverters. The DC-link voltages are equalized through the control of DABs and through the SVPWM algorithm applied to both CHB inverters. The applied SVPWM method is based on the solution presented in [23]. In this solution, the ML

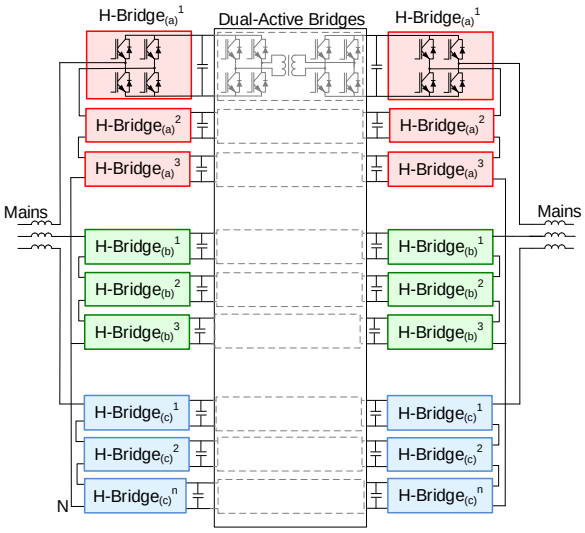

***Fig. 1**. The structure of Power Electronic Transformer with two seven-level CHB inverters and nine Dual-Active Bridges*

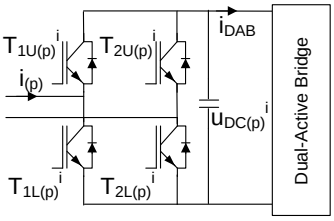

***Fig. 2.** The i-th (i=1..3) H-Bridge in the p-phase (p=a,b or c) of CHB inverter*

Table 1 The DC-link coupling configuration by Dual Active Bridges (DABs)

CHB inverter 1	coupled to (*via DAB*)	CHB inverter 2
$H\text{-}Bridge_{(a)}{}^{1}$	⇔	$H\text{-}Bridge_{(a)}{}^{1}$
$H\text{-}Bridge_{(a)}{}^{2}$	⇔	$H\text{-}Bridge_{(b)}{}^{1}$
$H\text{-}Bridge_{(a)}{}^{3}$	⇔	$H\text{-}Bridge_{(c)}{}^{1}$
$H\text{-}Bridge_{(b)}{}^{1}$	⇔	$H\text{-}Bridge_{(b)}{}^{2}$
$H\text{-}Bridge_{(b)}{}^{2}$	⇔	$H\text{-}Bridge_{(c)}{}^{2}$
$H\text{-}Bridge_{(b)}{}^{3}$	⇔	$H\text{-}Bridge_{(a)}{}^{2}$
$H\text{-}Bridge_{(c)}{}^{1}$	⇔	$H\text{-}Bridge_{(c)}{}^{3}$
$H\text{-}Bridge_{(c)}{}^{2}$	⇔	$H\text{-}Bridge_{(a)}{}^{3}$
$H\text{-}Bridge_{(c)}{}^{3}$	⇔	$H\text{-}Bridge_{(b)}{}^{3}$

CHB inverter is considered as a set of three-level inverters connected in series and controlled using the same algorithm. The analysis of the space-vector area takes into consideration the inequality of the DC-link voltages and its influence on the lengths and positions of active vectors. The influence of vector sequences on predicted DC-link voltages is also analyzed and the optimum vector sequence is selected in order to balance them.

The solution presented in [23] utilizes the classic method for selecting H-Bridges to generate the inverter output voltage, where the capacitor voltages are sorted at the beginning of each control period [44]. As a result, in the

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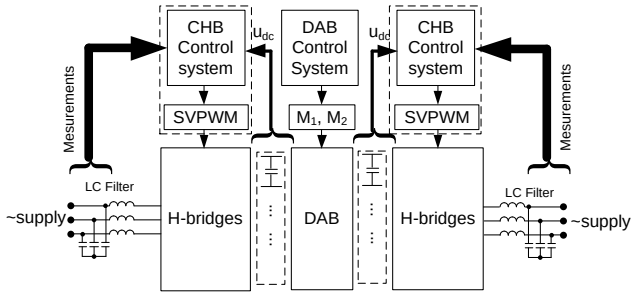

Fig. 3. *The PET control system*

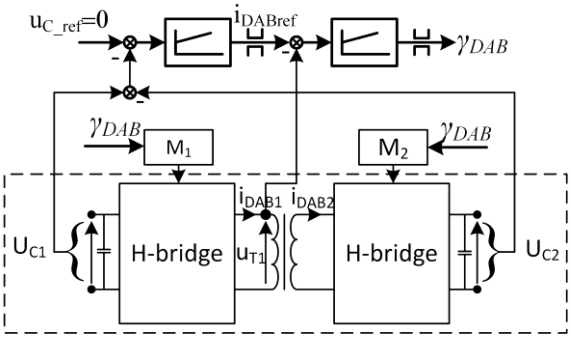

Fig. 4. *The control system for DAB converters*

initial stages of the modulation algorithm and for some positions of output voltage vector, some H-Bridges are indicated as a first to be balaced and work with zero duty cycle (they remain bypassed). At the same time, the other H-Bridges (with less unbalanced DC-link voltages) work with non-zero duty cycles and their DC-link voltages are equalized. This results in not optimal management of the DC-link voltage distribution. The solution proposed in this paper verifies the actual utilization of the H-Bridges in the voltage generation process. By reorganizing the order of H-Bridge utilization, the H-Bridges with most unbalanced DC-link voltages are used as first and they have non-zero duty cycles regardless of the length and position of the inverter output voltage vector. This enables further correction of DC-link voltage unbalance. The results of simulation research show the differences in voltage balancing for both methods. The experimental research was carried out on a fully loaded 600 kW /3.3 kV PET based on two seven-level CHB inverters and nine DABs. The results are presented in this paper.

2. The topology of a Power Electronic Transformer

The structure of a PET (Fig. 1) is based on two seven-level active-front CHB inverters. Each of them contains three H-Bridges per phase connected in series (Fig. 2). The DC-links of both CHB inverters are coupled using nine Dual Active Bridge (DAB) converters with Medium Frequency (MF) transformers. The adopted coupling method assumes the connection of each phase of the first CHB inverter with each phase of the second CHB inverter, as shown in Table 1. This is to ensure even loading of the branches of both inverters.

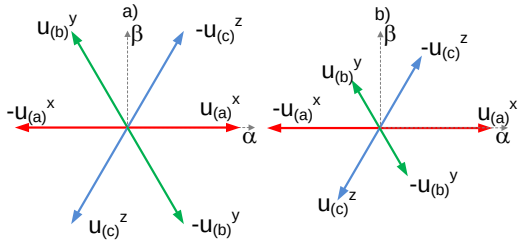

Fig. 5. *The active vectors obtained in three H-bridges in the case of* ***(a)*** *equal and* ***(b)*** *unequal DC-link voltages*

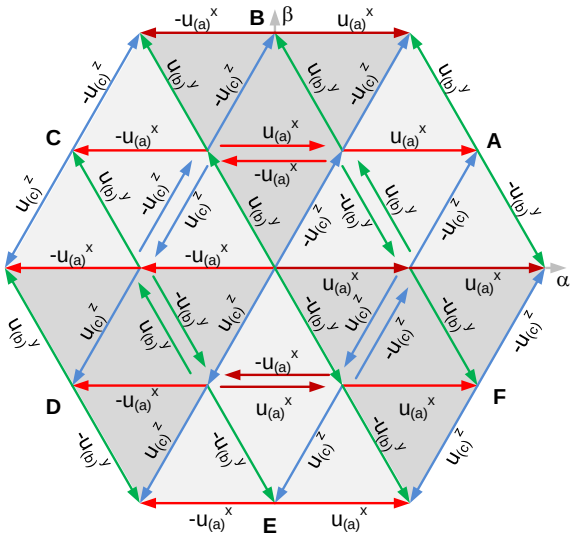

Fig. 6. *Active vectors of a three-level CHB converter in the case of equal DC-link voltages*

3. The control system for Dual Active Bridges

In the proposed solution, the nine Dual Active Bridge (DAB) converters were used to transfer the electrical energy between the DC-links of both CHB inverters. All the DAB converters are controlled independently, without information exchange about the control process with CHB inverters and other DABs (Fig.3). The DAB control system was designed to obtain the same voltages on both capacitors of a single CHB cell (the CHB cell contains one capacitor of the first and one capacitor of the second CHB inverter (Fig. 4)). As results – each DAB converter equalizes the single DC-link voltages of both CHB inverters. The utilised control strategy for DAB is based on mutual shifting of voltages on primary and secondary transformer windings, as presented in [21].

The applied superior control for both CHB inverters is grounded on a well-known control system with classic PI controllers, realized in coordinate system oriented with the grid voltages [48], [52].

4. The H-Bridge output voltage

The H-Bridges of the CHB inverter can be in active or zero state. During the zero state, two upper or two lower transistors are activated (Fig. 2). For active states, two transistors $T_{1U(p)}{}^{i}$, $T_{2L(p)}{}^{i}$ (for the positive output voltage) or $T_{2U(p)}{}^{i}$, $T_{1L(p)}{}^{i}$ (for the negative output voltage) are switched-on, where (p) is the phase (p=a, b or c), and i is the number of the H-Bridge in the CHB inverter topology (i=1..3) (Fig.1).

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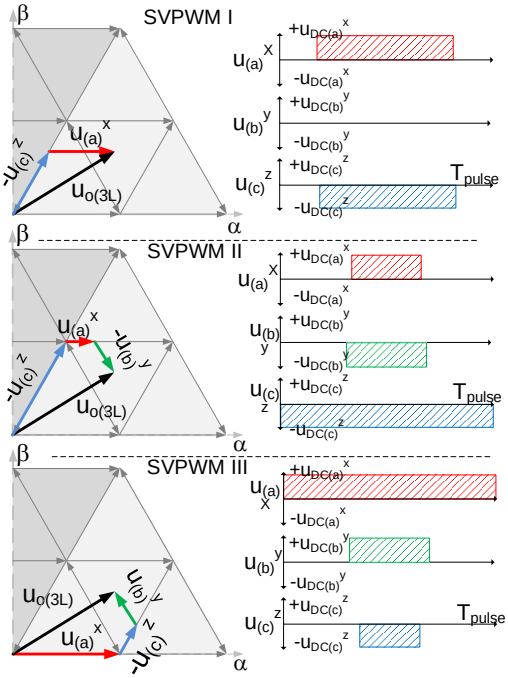

Fig. 7. *Generating of an output voltage vector in a three-level CHB converter using two (Modulation I) or three voltage vectors (Modulation II and III) and the corresponding phase voltage waveforms*

The duration of active and zero states can be calculated as:

$$t_{active(p)}{}^{i} = \gamma_{(p)}{}^{i} \cdot T_{pulse}, \qquad t_{zero(p)}{}^{i} = T_{pulse} - t_{active(p)}{}^{i}, \tag{1}$$

where: $t_{active(p)}{}^{i}$, $t_{zero(p)}{}^{i}$ are the durations of active and zero states in the *i*-th H-Bridge in *p*-phase and T_{pulse} is a pulse period.

The duty cycle γ can be calculated as:

$$\gamma_{(p)}{}^{i} = \frac{\left|u_{o(p)}{}^{i}\right|}{u_{DC(p)}{}^{i}}, \tag{2}$$

where: $u_{DC(p)}{}^{i}$ is a DC-link voltage, $u_{o(p)}{}^{i}$ is the H-Bridge output voltage, and:

$$0 \le \gamma_{(p)}{}^{i} \le 1. \tag{3}$$

If the duty cycle is equal to zero ($\gamma_{(p)}{}^{i}=0$) then the zero state is activated throughout the entire pulse period T_{pulse}, and the H-Bridge is bypassed. If the duty cycle is equal to 1 ($\gamma_{(p)}{}^{i}=1$), the H-Bridge is positively or negatively connected depending on the direction of the output voltage.

5. The output voltages of H-Bridges in a three-phase system

It is assumed that only one H-Bridge in each inverter phase is in an active state, while the other H-Bridges are bypassed. If the output voltages are generated by the following H-Bridges: "*x*" in the phase "*a*", "*y*" in the phase "*b*" and "*z*" in

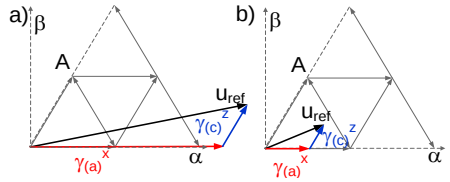

Fig. 8. *The duty cycles of SVPWM I in the case of* ***(a)*** *long and* ***(b)*** *short reference output voltage vector*

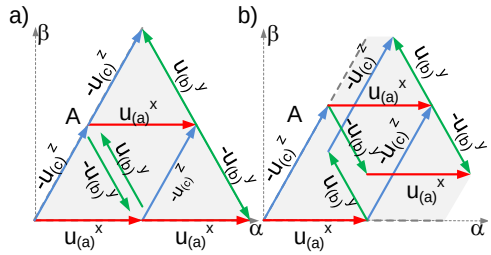

Fig. 9. *The shape of sector A and the lengths and positions of active vectors in the case of* ***(a)*** *balanced and* ***(b)*** *unbalanced DC-link voltages*

the phase "*c*" (*x=1..3; y=1..3; z=1..3;*) (Fig. 1), a three-phase system is obtained where the components of the voltage vectors can be calculated using Clarke's transformation (Fig. 5):

for a-phase H-Bridge:

$$u_{\alpha(a)}{}^{x} = \sqrt{\frac{2}{3}} \cdot u_{DC_a}{}^{x} \cdot \left(T_{1U(a)}{}^{x} - T_{2U(a)}{}^{x}\right), \qquad u_{\beta(a)}{}^{x} = 0, \tag{4}$$

for b-phase H-Bridge:

$$u_{\alpha(b)}{}^{y} = \sqrt{\frac{2}{3}} \cdot u_{DC(b)}{}^{y} \cdot cos\left(\frac{2\pi}{3}\right) \cdot \left(T_{1U(b)}{}^{y} - T_{2U(b)}{}^{y}\right), \qquad u_{\beta(b)}{}^{y} = \sqrt{\frac{2}{3}} \cdot u_{DC(b)}{}^{y} \cdot sin\left(\frac{2\pi}{3}\right) \cdot \left(T_{1U(b)}{}^{y} - T_{2U(b)}{}^{y}\right), \tag{5}$$

and for c-phase H-Bridge:

$$u_{\alpha(c)}{}^{z} = \sqrt{\frac{2}{3}} \cdot u_{DC(c)}{}^{z} \cdot cos\left(\frac{4\pi}{3}\right) \cdot \left(T_{1U(c)}{}^{z} - T_{2U(c)}{}^{z}\right), \qquad u_{\beta(c)}{}^{z} = \sqrt{\frac{2}{3}} \cdot u_{DC(c)}{}^{z} \cdot sin\left(\frac{4\pi}{3}\right) \cdot \left(T_{1U(c)}{}^{z} - T_{2U(c)}{}^{z}\right), \tag{6}$$

where: T_{1U}, T_{2U} are the gate signals for the upper transistors (Fig. 2) with values: *1* – when upper transistor is switched on, 0 – when lower transistor is activated, and u_{DC} are the DC-link voltages.

The active voltage vectors can be simultaneously generated by the H-Bridges in three phases. The components of the available voltage vectors can be calculated as:

$$u_{\alpha(3L)}{}^{j} = u_{\alpha(a)}{}^{x} + u_{\alpha(b)}{}^{y} + u_{\alpha(c)}{}^{z}, \qquad u_{\beta(3L)}{}^{j} = u_{\beta(a)}{}^{x} + u_{\beta(b)}{}^{y} + u_{\beta(c)}{}^{z}. \tag{7}$$

The active vectors generated by the three H-Bridges are shown in Fig. 6. It follows that these H-Bridges form a three-level inverter. The ML inverter with three H-Bridges per phase can be analyzed as a set of three three-level CHB inverters with the output voltage components equal to:

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$$u_{\alpha(ML)} = u_{\alpha(3L)}{}^{1} + u_{\alpha(3L)}{}^{2} + u_{\alpha(3L)}{}^{3},$$
$$u_{\beta(ML)} = u_{\beta(3L)}{}^{1} + u_{\beta(3L)}{}^{2} + u_{\beta(3L)}{}^{3}. \quad (8)$$

The ML CHB inverter can be properly controlled by successively activating one H-Bridge per phase until the reference voltage vector is reached. The resulting three-level inverters are controlled by the same SVPWM algorithm. If the obtained output voltage is different from the reference voltage, the next three-level CHB inverter is activated. It is obviously necessary to ensure that only one H-Bridge per phase provides a modulated output voltage, while the others are negatively / positively connected or bypassed.

The selection of H-Bridges, used to construct the three-level inverters, depends on the direction of the instantaneous power and the DC-link voltages. If the condition is fulfilled:

$$i_{(p)} \cdot u_{ref(p)} > 0\,, \quad (9)$$

the first three-level inverter will be constructed using the H-Bridges with the lowest DC-link voltages, where: $i_{(p)}$ is the "*p*"- phase current, $i_{(p)}>0$ denotes that the current flows to inverter (Fig. 2), $u_{ref(p)}$ is the "*p*"-phase reference voltage determined using reverse Clarke's transformation,
Otherwise, the H-Bridges with the highest DC-link voltages are utilized as the first. The next three-level inverters are built similarly, using available (previously unused) H-Bridges. As a result, the DC link voltages within each phase of the CHB inverter are equalized. The choice of H-Bridges used to construct the three-level inverters is realized at the beginning of each control period [23], [44].

6. The SVPWM for three-level CHB inverter

In the proposed solution, the output voltage vector of each three-level CHB inverter can be generated using one of three proposed SVPWM strategies. The SVPWM I utilizes two active vectors and the duty cycle of one of H-Bridges is equal to zero. This H-Bridge is bypassed, and the output voltages are modulated in two H-Bridges (Fig. 7a). SVPWM II and III utilize three H-Bridges in active states. The duty cycles are chosen to obtain at least one of the H-Bridges positively or negatively connected ($\gamma_{(p)}{}^{i} = 1$) (Fig.7b,c).

All the modulation strategies I—III are calculated in the same control period for any position and length of the reference voltage vector and the most suitable SVPWM method is chosen for implementation. The selection method is described in Section 8. The methods for the determination of duty cycles for all modulation strategies are shown below.

6.1. SVPWM I – one of the H-Bridges is bypassed

In the SVPWM I, the output voltage vector is generated using two active vectors (Fig. 7a). Two H-Bridges are in the active states and one H-Bridge is bypassed. If the position of the reference voltage vector is in the range of 0 to $2\pi/6$ rad, the reference voltage vector is assigned to sector A (Fig. 6)

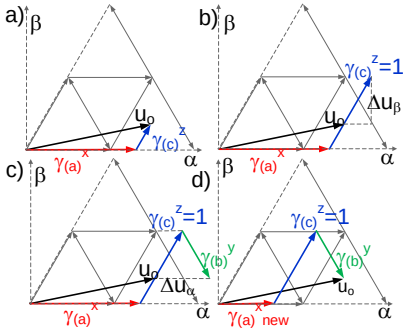

***Fig. 10**. The duty cycle selection steps in SVPWM II*

regardless of its length (Fig. 8) and DC-link voltage imbalance (Fig. 9).

If the reference voltage vector is in the sector A, the H-Bridge in phase "a" generates positive output voltage, the H-Bridge in phase "c" gives negative output voltage and the H-Bridge in phase "b" is bypassed (Fig.5a). The duty cycles can be determined as:

$$\gamma_{(a)}{}^{x} = \frac{u_{ref\alpha} \cdot u_{\beta(c)}{}^{z} - u_{ref\beta} \cdot u_{\alpha(c)}{}^{z}}{u_{\beta(c)}{}^{z} \cdot u_{\alpha(a)}{}^{x} - u_{\alpha(c)}{}^{z} \cdot u_{\beta(a)}{}^{x}},$$
$$\gamma_{(b)}{}^{y} = 0, \quad (10)$$
$$\gamma_{(c)}{}^{z} = \frac{u_{ref\beta} \cdot u_{\alpha(a)}{}^{x} - u_{ref\alpha} \cdot u_{\beta(a)}{}^{x}}{u_{\beta(c)}{}^{z} \cdot u_{\alpha(a)}{}^{x} - u_{\alpha(c)}{}^{z} \cdot u_{\beta(a)}{}^{x}},$$

where: $u_{ref\alpha}$, $u_{ref\beta}$ are the components of the reference voltage vector of the ML CHB inverter, $u_{\alpha(p)i}$, $u_{\beta(p)i}$ are the components of the active voltage vectors generated by the H-Bridges in the "p" phase (p= a,b or c) and "i" is the H-Bridge number (i=x, y, z) (x=1..3, y=1..3, z=1..3).

The equations (10) utilize the H-Bridge output voltages (4)-(6) determined taking into account the actual DC-link voltages. The DC-link voltage fluctuations do not have any effect on the correctness of generated output voltage vector.

It should be noted, that the calculated duty cycles can be greater than one for high amplitude of the reference voltage (Fig. 8a). They will be limited in the next step of the modulation algorithm, described in section 7.

6.2. SVPWM II – one of the H-Bridges is positively/negatively connected

If the reference voltage vector is located in sector A (Fig. 6), it can be also constructed using the following active vectors (Fig. 7b):

- the main active vector $\boldsymbol{u}_{(a)}{}^{x}$ generated in phase "a" H-Bridge,
- the complementary active vector $-\boldsymbol{u}_{(c)}{}^{z}$ generated in phase "b" H-Bridge,
- the auxiliary active vector $-\boldsymbol{u}_{(b)}{}^{y}$ generated in phase "c" H-Bridge.

The components of these active voltage vectors are determined using eq. (4)-(6) where the actual DC-link voltages are taken into account.

The choice of the H-bridges (x, y and z) in individual phases is based on eq. (9). The duty cycles for the H-Bridges

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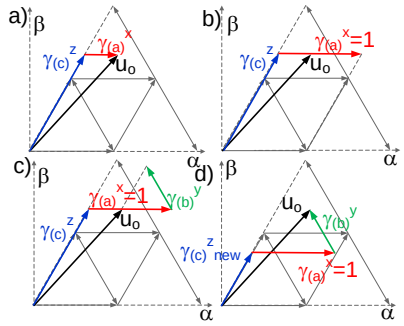

***Fig. 11**. The duty cycle selection steps in SVPWM III*

in phases "a" and "c" are calculated in the same way as in SVPWM I (10), assuming zero value of the duty cycle for the H-Bridge in phase "b" (auxiliary active vector) (Fig. 10a).

If the calculated duty cycles are less than 1, the active and passive states will be activated in the H-Bridges and it will be necessary to switch the transistors. The necessity of zero vector activation (and the necessity of transistor switching) in the phase "c" H-Bridge can be eliminated by modifying its duty cycle (Fig. 10b):

$$if\ \gamma_{(c)}{}^{z} < 1 \Rightarrow \gamma_{(c)}{}^{z} = 1, \quad (11)$$

by the value:

$$\Delta\gamma_{(c)}{}^{z} = 1 - \gamma_{(c)}{}^{z}. \quad (12)$$

The change in the duty cycle affects the length and position of the output voltage vector (Fig. 10b). The change in the β-component of the output voltage vector can be calculated as:

$$\Delta u_{\beta} = \left(\Delta\gamma_{(c)}{}^{z} \cdot \left|\boldsymbol{u}_{(c)}{}^{z}\right|\right) \cdot sin\left(\frac{\pi}{3}\right), \quad (13)$$

and compensated for by the auxiliary vector (Fig. 10c). The duty cycle for the H-Bridge, where the auxiliary voltage vector is generated, can be calculated as:

$$\gamma_{(b)}{}^{y} = \frac{\Delta u_{\beta}}{\left|\boldsymbol{u}_{(b)}{}^{y}\right| \cdot sin\left(\frac{\pi}{3}\right)}. \quad (14)$$

Substitution (13) to (14) gives:

$$\gamma_{(b)}{}^{y} = \Delta\gamma_{(c)}{}^{z} \cdot \frac{\left|\boldsymbol{u}_{(c)}{}^{z}\right|}{\left|\boldsymbol{u}_{(b)}{}^{y}\right|}. \quad (15)$$

Increasing the duration of the complementary vector and activation of the auxiliary vector affects the output voltage vector. The α-component of the output voltage vector is increased by the value (Fig. 10c) :

$$\Delta u_{o\alpha} = \left(\Delta\gamma_{(c)}{}^{z} \cdot \left|\boldsymbol{u}_{(c)}{}^{z}\right| + \gamma_{(b)}{}^{y} \cdot \left|\boldsymbol{u}_{(b)}{}^{y}\right|\right) \cdot cos\left(\frac{\pi}{3}\right). \quad (16)$$

The duty cycle for the "a" phase H-bridge, where the main voltage vector is activated, should therefore be reduced (Fig. 10d):

$$\gamma_{(a)}{}^{x}{}_{new} = \gamma_{(a)}{}^{x} - \frac{\Delta u_{\alpha}}{\left|\boldsymbol{u}_{(a)}{}^{x}\right|}. \quad (17)$$

where $\gamma_{(a)}{}^{x}{}_{new}$ is the reduced duty cycle.

All the modifications take into consideration the actual DC-link voltages. The DC-link voltage fluctuations do not have any effect on the correctness of generated output voltage vector.

The presented modification of the duty cycles provides equality of the output voltage vector and the reference voltage vector (Fig. 10d). One of the H-Bridges is positively connected and its transistors are not switched. The phase voltage waveforms of three-level CHB converter with SVPWM II are shown in Fig. 7b.

If the new duty cycle $\gamma_{(a)}{}^{x}{}_{new}$ is negative, the output voltage vector will be generated using two H-Bridges only. The duty cycles can be calculated similarly as in SVPWM I:

$$\gamma_{(a)}{}^{x}{}_{new} = 0,$$

$$\gamma_{(b)}{}^{y}{}_{new} = \frac{u_{ref\alpha} \cdot u_{\beta(c)}{}^{z} - u_{ref\beta} \cdot u_{\alpha(c)}{}^{z}}{u_{\beta(c)}{}^{z} \cdot u_{\alpha(b)}{}^{y} - u_{\alpha(c)}{}^{z} \cdot u_{\beta(b)}{}^{y}}, \quad (18)$$

$$\gamma_{(c)}{}^{z}{}_{new} = \frac{u_{ref\beta} \cdot u_{\alpha(b)}{}^{y} - u_{ref\alpha} \cdot u_{\beta(b)}{}^{y}}{u_{\beta(c)}{}^{z} \cdot u_{\alpha(b)}{}^{y} - u_{\alpha(c)}{}^{z} \cdot u_{\beta(b)}{}^{y}},$$

but with bypassed phase "a" H-Bridge. Because its duty cycle is equal to zero, its transistors will not be switched.

If the duty cycles of H-Bridges will be greater than 1, they will be limited in the next step of the modulation algorithm (Section 7).

6.3. SVPWM III – one of the H-Bridges is positively/negatively connected

In modulation SVPWM III the replaced main and complementary active vectors and the opposite auxiliary vector are used, all defined for modulation strategy II (Fig. 7c). If the output voltage vector is located in sector *A* (Fig. 6), the following active vectors will be exploited:

- the main active vector $-\boldsymbol{u}_{(c)}{}^{z}$ generated in phase "c" H-Bridge,
- the complementary active vector $\boldsymbol{u}_{(a)}{}^{x}$ generated in phase "a" H-Bridge,
- the auxiliary active vector $\boldsymbol{u}_{(b)}{}^{y}$ generated in phase "b" H-Bridge.

The choice of the H-Bridges (x, y and z) in individual phases is based on eq. (9). All the duty cycles are determined in the same manner as in SVPWM II taking account actual DC-link voltages. The duty cycles for the H-Bridges in phase "a" and phase "b*"* are increased, while the duty cycle for the phase "c" H-Bridge is decreased (Fig. 11 a-d). The phase voltage waveforms of three-level CHB converter with Modulation III are shown in Fig. 7c.

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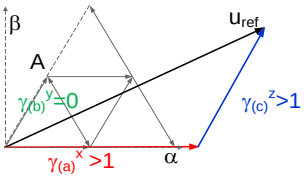

Fig. 12. *The duty cycles of SVPWM I in the case of long reference voltage vector*

7. Limitation of the duty cycles

All the calculated duty cycles can be greater than 1, especially if the modulation strategies are applied to the first of three-level inverters and the end of the reference voltage vector is located outside the hexagon shown in Fig. 6. In this case it is necessary to limit the duty cycles:

$$if\ \gamma_{(a,b,c)}{}^{x,y,z} > 1 \Rightarrow \gamma_{(a,b,c)}{}^{x,y,z} = 1. \quad (19)$$

For all presented SVPMWs I-III, the components of the output voltage vector are calculated using limited duty factors:

$$\begin{aligned} u_{o\alpha(3L)}{}^{j} &= \gamma_{(a)}{}^{x} \cdot u_{\alpha(a)}{}^{x} + \gamma_{(b)}{}^{y} \cdot u_{\alpha(b)}{}^{y} + \gamma_{(c)}{}^{z} \cdot u_{\alpha(c)}{}^{z}, \\ u_{o\beta(3L)}{}^{j} &= \gamma_{(a)}{}^{x} \cdot u_{\beta(a)}{}^{x} + \gamma_{(b)}{}^{y} \cdot u_{\beta(b)}{}^{y} + \gamma_{(c)}{}^{z} \cdot u_{\beta(c)}{}^{z}, \end{aligned} \quad (20)$$

where: $u_{o\alpha(3L)}{}^{j}$, $u_{o\beta(3L)}{}^{j}$ are the components of the output voltage vector of the j-th three level CHB inverter (j=1..3).

Because three equivalent modulation strategies have been prepared and their allowable output voltage vectors have been determined, the next step is to choose the optimal method of output voltage generating.

8. The choice of SVPWM strategy

The proposed solution makes it possible to obtain the output voltage vector using one of three equivalent SVPWM strategies. If the duty cycles were limited using (19) in all considered SVPWMs (I-III) it means that the reference voltage vector is located outside the hexagon shown in Fig. 6. In this case, the chosen SVPWM method (one of the SVPWM strategies I-III) should ensure the output voltage vector as close as possible to the reference voltage. To ensure this, a SVPWM method is chosen that provides a minimum value of the function:

$$\begin{aligned} &f\left(u_{o\alpha(3L)}{}^{j}, u_{o\beta(3L)}{}^{j}\right) = \\ &\left(u_{ref\,\alpha} - u_{o\alpha(3L)}{}^{j}\right)^2 + \left(u_{ref\,\beta} - u_{o\beta(3L)}{}^{j}\right)^2, \end{aligned} \quad (21)$$

where: $u_{o(3L)\alpha}$, $u_{o(3L)\beta}$ are the components of the output voltage vector calculated using (20) for each of the SVPWM strategies I-III, $u_{ref\alpha}$, $u_{ref\beta}$ are the components of the reference voltage vector.

For the chosen SVPWM strategy the obtainable voltage vector is calculated taking into account the limitation of duty cycles (20). If the reference voltage vector and the obtained

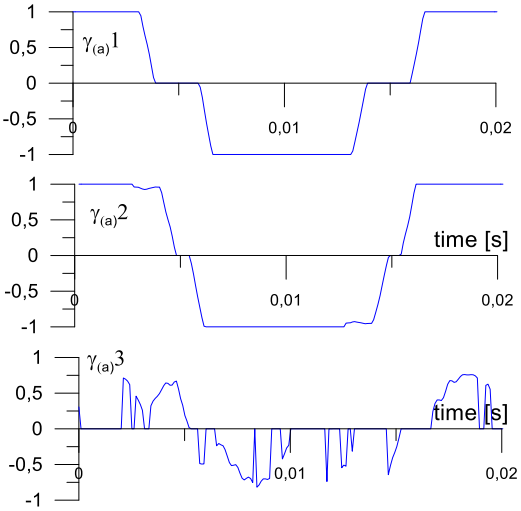

Fig. 13*. The duty cycles for the H-Bridges in one of the ML CHB inverter phases calculated in the first stage ($\gamma_{(a)}1$) (the first three-level CHB inverter), the second stage ($\gamma_{(a)}2$) (the second three-level CHB inverter) and the last stage ($\gamma_{(a)}3$) (the third CHB inverter) of the output voltage generation process. (Negative duty cycles denote negative values of H-Bridge output voltages). Simulation result.*

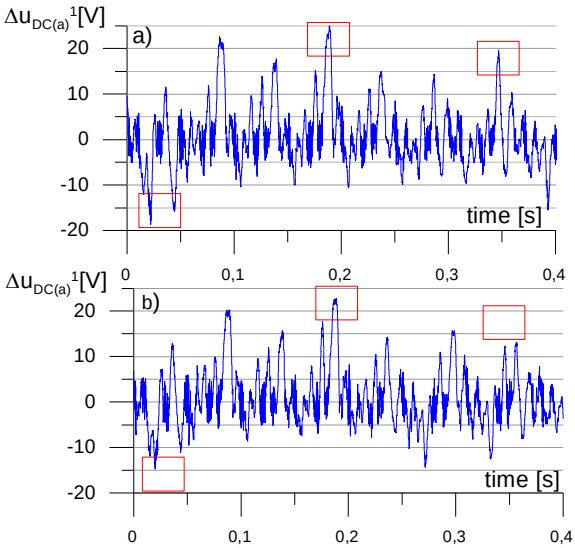

Fig. 14*. The unbalanced voltage of one of the H-Bridges* ***(a)*** *in the case of a single-choice of H-Bridge utilisation order and* ***(b)*** *in the case of re-use of the H-Bridges with zero duty cycles in the consecutive three-level CHB inverter. Simulation result.*

output voltage vector are not equal, the next three-level inverter is (the next three H-Bridges are) activated. There is another reference voltage vector applied to the next inverter. The new reference voltage vector components $u'_{ref\alpha}$, $u'_{ref\beta}$ for the consecutive three-level inverter are calculated as:

$$\begin{aligned} u'_{ref\,\alpha} &= u_{ref\,\alpha} - u_{o\alpha(3L),}{}^{j} \\ u'_{ref\,\beta} &= u_{ref\,\beta} - u_{o\beta(3L)}{}^{j}. \end{aligned} \quad (22)$$

where $u_{ref\,\alpha}$, $u_{ref\,\beta}$ are the components of the reference voltage for CHB inverter, calculated in a superior control system.

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The output voltage vector in the consecutive three-level inverters is generated in the same way. The three equivalent SVPWM strategies are considered, and the most suitable is chosen in the manner given above.

The consecutive H-Bridges are activated as long as it will be possible to generate the entire reference voltage. In the final stage of output voltage generation, at least one of the SVPWM strategies I-III will allow to obtain the reference voltage without the necessity of duty cycle limitation. It means that the reference vector $\mathbf{u'}_{ref}$ is already located in the hexagon shown in Fig. 6. In this case, the SVPWM strategy is chosen in a different way. The output voltage is generated using this SVPWM strategy, which ensures minimization of the predicted DC-link voltage unbalance:

$$\begin{aligned} & f\left(u_{DC(a)}{}^{x}, u_{DC(b)}{}^{y}, u_{DC(c)}{}^{z}\right) = \\ & \left(u_{DC(a)}{}^{x}(k+1) - u_{DC(AV)}\right)^2 + \\ & \left(u_{DC(b)}{}^{y}(k+1) - u_{DC(AV)}\right)^2 + \\ & \left(u_{DC(c)}{}^{z}(k+1) - u_{DC(AV)}\right)^2, \end{aligned} \quad (23)$$

where:

$$u_{DC(AV)} = \frac{u_{DC(a)}{}^{x}(k+1) + u_{DC(b)}{}^{y}(k+1) + u_{DC(c)}{}^{z}(k+1)}{3}, \quad (24)$$

and:

$$u_{DC(p)}{}^{i}(k+1) = u_{DC(x)}{}^{i}(k) + \frac{1}{C} \cdot \gamma_{(p)}{}^{i} \cdot T_{pulse} \cdot i_{(p),} \quad (25)$$

where: *p* is the phase of CHB inverter (p=a, b or c), "i" is the number of the selected H-Bridges (i=x, y, z; x=1..3; y=1..3; z=1..3), C is the DC-link capacitance, *(k)* and *(k+1)* denote the DC-link voltages determined for the actual and next pulse periods.

The condition (23) is considered only for those SVPWM strategies, in which the duty cycles were not limited.

9. Change in the order of H-Bridge utilisation

The proposed modulation strategy utilizes one of the three alternative switching sequences to generate the inverter output voltage vector. At the early stages of output voltage generating process, the reference voltage vector applied to the three-level CHB inverter is located outside the area shown in Fig. 6. It means, that the duty cycle of at least one of two H-Bridges is greater than 1, while one H-Bridge remain bypassed (SVPWM1). The algorithms SVPWM2 and SVPWM3 are designated to increase one of the duty cycles to 1, but it is possible only for the duty cycles in the range $0 \le \gamma < 1$. This means that for the reference voltage vector position close to the sector edge (Fig. 8a) only one of the algorithms (SVPWM2 or SVPWM3) can increase the duty cycle and can ensure nonzero duty cycles for all utilized H-Bridges.

If the reference voltage vector is located in the center of the sector, both the duty cycles calculated in the SVPWM1 algorithm can be greater than one while one duty cycle is

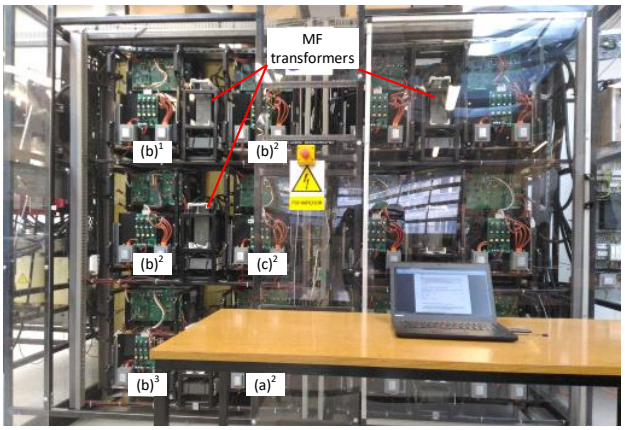

***Fig. 15**. The experimental stand with 600 kW / 3.3 kV PET, $(b)^1$,$(b)^2$,$(b)^3$ (on the left) – the H Bridges and the DABs in the "b" phase of the first CHB inverter, $(b)^2$,$(c)^2$,$(a)^2$- the H Bridges and DABs in the phases "a", "b" and "c" of the second CHB inverter (Tab.1)*

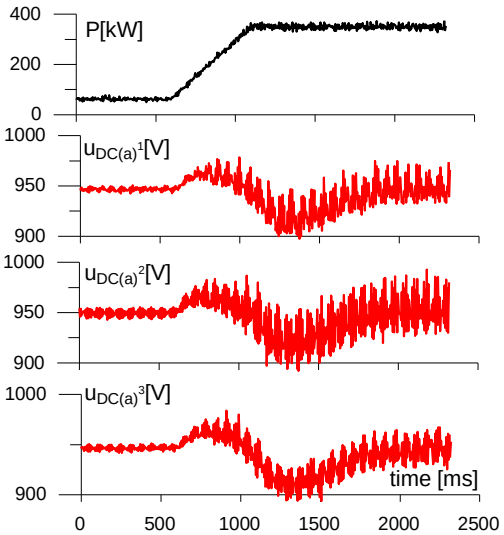

***Fig. 16**. The change in active power (50-350 kW) of the PET. P– active power, $u_{DC(a)}{}^{1\text{-}3}$ – phase "a" DC-link voltages, $^{1\text{-}3}$- H-Bridge number. Experimental result*

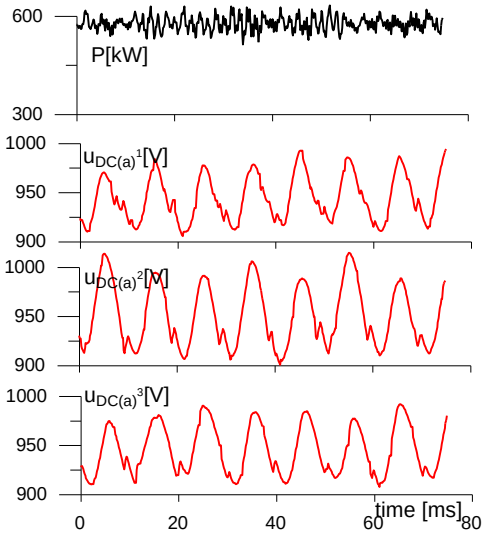

***Fig. 17**. The DC-link voltages in "a" phase of PET during active power transmission. $u_{DC(a)}{}^{1\text{-}3}$ – phase "a" DC-link voltages, $^{1\text{-}3}$- H-Bridge number. Experimental result*

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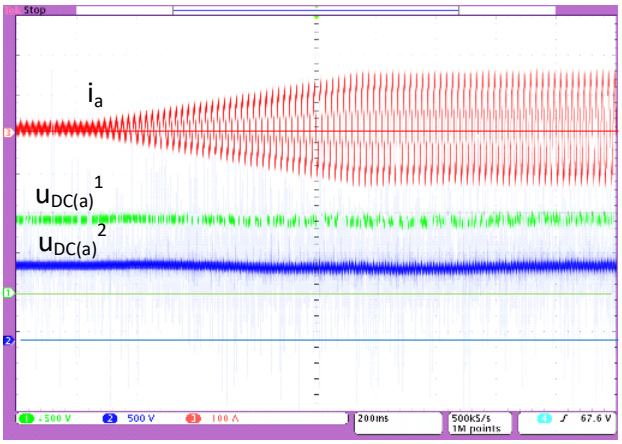

***Fig. 18**. The change in active power (50-550kW) of the PET. i_a– phase "a: current, $u_{DC(a)}^{1-2}$ – phase "a" DC-link voltages, $^{1-2}$- H-Bridge number. Scales: 100A/div, 500V/div, 200ms/div*

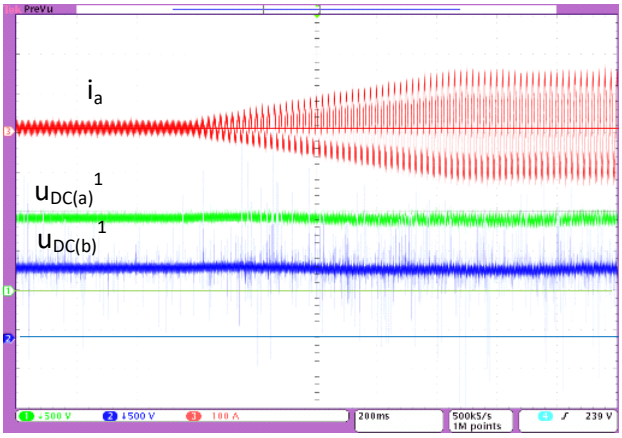

***Fig. 19**. The change in active power (50-550 kW) of the PET. i_a– phase "a: current, $u_{DC(a)-(b)}^1$ – the DC-link voltages on the first H-Bridge in the phases "a" and "b" Scales: 100 A/div, 500 V/div, 200 ms/div*

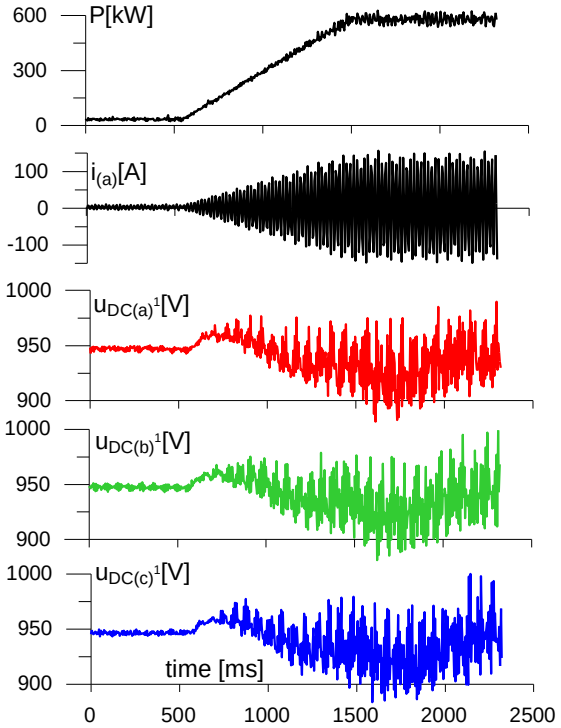

***Fig. 20**. The change in active power (50-600 kW) of the PET. P– active power, $i_{(a)}$- phase "a" current, $u_{DC(a-c)}^1$ – the DC-link voltages on the first H-Bridge in the phases "a", "b" and "c". Experimental result*

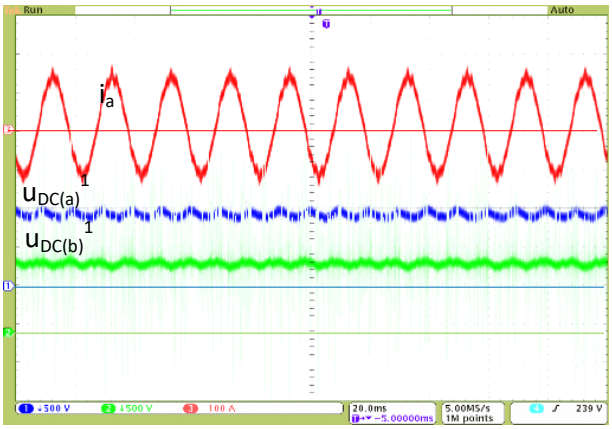

***Fig. 21**. The waveform of a phase current (i_a) and DC-link voltages on the first H-Bridge in the phases "a" and "b" ($u_{DC(a)}^1$, $u_{DC(b)}^1$) during active power transmission (P=550 kW). Scales: 100 A/div, 500 V/div, 20 ms/div*

equal to zero (Fig. 12). In this case, none of the modulation strategies (SVPWM2 and SVPWM2) can change the calculated duty cycles. The duty cycles with the values greater than one will be limited at the end of modulation algorithm, while the duty cycle equal to zero will not change (Fig. 13). As a results, the H-Bridge selected as the first to be balanced remains bypassed and its DC-link voltage does not change. This is the effect of a single selection of the order of H-Bridge utilization carried out at the beginning of control period (9).

The H-Bridges with zero duty cycles determined in the first stage of output voltage generating process can be reused in the consecutive stages. It is possible by simply changing the order of the H-Bridge utilization and it does not require recalculation of the SVPWM algorithm. The H-Bridge, selected as the first in the sorting procedure, with zero duty cycle determined in the first stage of the modulation algorithm can be reused in the second stage (in the second three-level CHB inverter). If the new value of the duty cycle determined in the second stage is non-zero, the DC-link voltage of this H-Bridge will be equalized (if not – this H-Bridge will be moved to the third stage). At the same time the H-Bridge initially assigned to the second stage (second three-level CHB inverter) is reassigned to the third stage (third three-level CHB inverter). The H-Bridge with most balanced DC-link voltage is reassigned to the first stage (first three-level CHB inverter) and its duty cycle remains equal to zero (it does not require recalculation of the SVPWM algorithm – this is just a replacement of the H-Bridge with zero duty-cycle). Such modification allows for further limitation of DC-link voltage unbalancing. The Fig. 14 presents the unbalanced DC-link voltage for the case when the sequence of H-Bridge utilization at the beginning of each control period is determined and for the case where the H-Bridges with zero duty cycles are reused in the next stages of output voltage generation algorithm (are reused to build the consecutive

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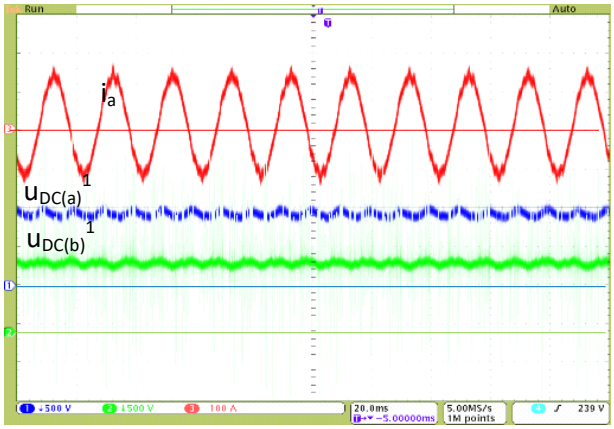

***Fig. 22**. The waveform of a phase current (i_a) and DC-link voltages on the first H-Bridge in the phases "a" and "b" ($u_{DC(a)}^1$, $u_{DC(b)}^1$) during active power transmission (P=550 kW). Scales: 100 A/div, 500 V/div, 20 ms/div*

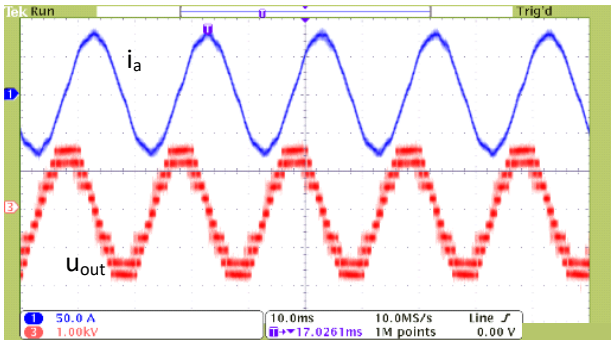

***Fig. 23**. The waveform of a phase current (i_a) and output voltage of PET based on two CHB active front inverters, Scales: 50 A/div, 1 kV/div, 10 ms/div*

three level CHB inverters). The unbalanced DC-link voltage shown in Fig.14 is calculated as:

$$\Delta u_{DC(a)}{}^{1} = u_{DC(a)}{}^{1} - \frac{1}{3}\sum_{k=1}^{3} u_{DC(a)}{}^{k}. \quad (26)$$

The improvement presented above allows further reduction of the DC-link voltage unbalance. The reduction is not large because the problem of using the H-Bridges with zero duty cycles occurs only for specific positions of output voltage vector as well because the DC-link voltages are simultaneously equalized through the DABs.

10. Results of experimental researches

The analysed PET topology consists of two 600 kW seven-level CHB (Fig.15). The DC-links of both inverters were coupled using 70 kW / 1 kV DABs with custom made MF transformers in the configuration shown in Table 1. The CHB inverter contains nine DC-links with the capacity of 2.4 mF. Switching frequencies are: DABs – 7kHz, inverters - 3.33 kHz. The PET was used to connect MV (3.3 kV) grids.

All the DABs have the same structure of control system (Fig. 4) and all these control systems work independently. The equalization of DAB capacitor voltages forced by the DAB control system can extort the uneven voltage distribution on the capacitors of both CHB inverters. Any change in DC-link voltages of a single CHB inverter is treated as a distortion and is reduced by the SVPWM algorithm.

The superior control system for both CHB inverters is a well-known control system for active-front converters with classic PI controllers, realized in coordinate system oriented with the grid voltages.

The proposed modulation strategy makes it possible to control the DC-link voltages in steady and transient states. The results of the experimental research of the seven level CHB inverter during a change in transmitted active power are shown in Figures: 16, 18-20 The waveforms of DC-link voltages are shown in Figures 17, 21, 22. All the DC-link voltages are almost the same and the output voltage is generated correctly. The amplitude of DC-link voltage oscillation is approximately 50 V for fully loaded inverter (Fig. 17). The changes in DC-link voltages have a negligible effect on the current waveforms. The waveforms of CHB inverter output voltage and current are shown in Figure 23. The THD of the phase current is equal to: THD_i=3.4 %.

The main limitation of the solution (which is mainly the result of the CHB inverter structure) is the problem of DC-link voltage balancing in the case of very low (close to zero) active power transmission. The DC-link voltages have to be balanced due to the presence of resistors used to discharge the DC-link capacitors. In this case, it is necessary to generate some reactive power to ensure the appropriate current flow through the inverter H-Bridges. The current value, which is necessary to equalize the DC-link voltages, depends on the repeatability of the discharging resistance parameters

In the proposed solution, the positively/negative connected or bypassed H-Bridges are utilised to generate the inverter output voltage vector. Only one H-Bridge in any of phases modulates its output voltage. This affects the efficiency of PET. The efficiency tests were provided for PET, in which both CHB inverters were working on the same grid. One of the CHB inverters absorbed the active power, while the second worked as a power source. The consumed power was equal to the inverter loses. The efficiency of fully loaded PET (without the power consumed by the cooling system) was equal to 94 %.

11. Conclusions

The paper presents the topology of PET based on two active-front CHB inverters coupled with nine Dual-Active Bridge (DAB) converters with Medium Frequency (MF) transformers. The PET topology and the proposed control method allows for balancing the load of DC-link capacitors. The DC-link voltages are equalized through the control of DAB voltages and through the proposed modulation strategy applied to both CHB inverters.

In the proposed Space-Vector Pulse Width Modulation (SVPWM), the influence of vector sequences on predicted DC-link voltages is analysed and optimum vector sequence is selected in order to balance them. The active vectors and their duty cycles are determined taking into account actual DC-link voltages. The output voltage vector is generated correctly, independently of the DC-link voltage imbalance.

The ML CHB inverters of PET are analysed as a sets of three-level inverters connected in series. Each of them is controlled by one of three equivalent modulation methods. This approach simplifies the implementation of SVPWM algorithm in the case of unbalanced DC-link voltages. It also allows for the use of the proposed method to control the CHB inverter with any number of levels.

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In the proposed solution, the utilisation of H-Bridges in the output voltage generation process is verified. The H-Bridges with zero duty cycles determined in the first stage of output voltage generating process are reused in the consecutive stages. By reorganizing the order of H-Bridge utilization, the H-Bridges with most unbalanced DC-link voltages are used as the first and they have non-zero duty cycles regardless of the length and position of inverter output voltage vector. This enables further correction of DC-link voltage imbalance. The results of simulation and experimental research were presented in the paper.

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