Hybrid-mode single-slope ADC with improved linearity and reduced conversion time for CMOS image sensors

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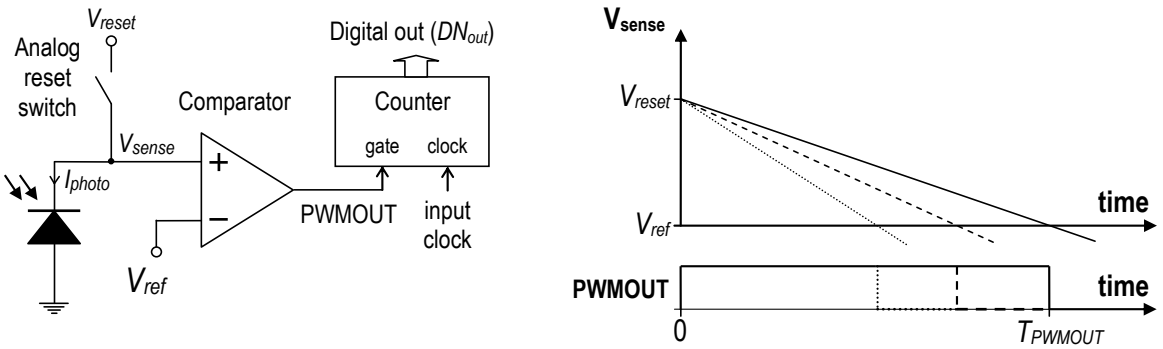
Abstract

In the paper, a single-slope analog-to-digital converter (ADC) for integrated CMOS image sensor applications with an improved technique of conversion has been proposed. The proposed hybrid-mode ADC automatically uses one of the following conversion techniques: time based (i.e. PWM) or voltage based (i.e. single-slope). During the ADC operation, the clock frequency and reference voltage are modified in order to reduce the conversion time and achieve the optimal linearity. Owing to this, the pixel using a photodiode working in the integration mode achieves a linear photoconversion characteristics (irradiance to digital number), and the conversion period, which is determined by the darkest parts of a scene, is reduced by an order of magnitude comparing to known ADC solutions. The proposed conversion technique has been validated with the ASIC prototype of a CMOS imager containing photosensors integrated with the ADCs. The ASIC was fabricated in standard 0.18 μm CMOS technology. A specialized measurement system has been used to optimize the hybrid-mode conversion to achieve very good linearity (integral nonlinearity below 2 LSB). The conversion period has been reduced 15 times compared to the standard technique. Measurements confirm functionality of the proposed approach, implemented within a small pixel area.

Keywords: CMOS image sensor, slope ADC, integration-mode photodiode, time-to-digital conversion.

1. Introduction

Time-to-digital conversion based ADCs, like single-slope ADCs, are often used in CMOS imaging arrays with massively parallel image acquisition [1-5], because they require a relatively small silicon area and can be integrated with the pixels. These ADCs can directly process, without a sample-and-hold circuit, the signal from a photodiode working in an integration mode, as shown in Fig. 1. The photodiode and electronic switch form a light-to-voltage-slope converter in which the light intensity is converted to the constant slope of the decreasing voltage on the V_{sense} node. An analog comparator forms a voltage-slope-to-time converter in which the V_{sense} slope is converted into the width of a pulse on PWMOUT. The pulse width is converted to digital value DN_{out} by a time-to-digital converter, for example a counter counting the gated clock pulses. All three conversions i.e. light-to-voltage-slope, voltage-slope-to-time and time-to-digital are realized simultaneously.



(a) (b)

Fig. 1 *Pixel ADC suitable for a massively parallel CMOS image sensor. (a) Simplified schematic diagram. (b) Waveforms of the V_{sense} and PWMOUT signals.*

The light-to-digital converter shown in Fig. 1a, in the simplest implementation, utilizes constant values for both V_{ref} and clock frequency. This solution, however, has some limitations that can be explained on the basis of the following short analysis.

In the circuit of Fig. 1a, the conversion cycle begins with the analog reset, which sets the initial voltage V_{reset} on the photodiode. Then, the reset switch is opened and the small sense-node capacitance is discharged with the photodiode current, according to the following formula:

$$dV_{sense} / dt = - I_{photo} / (C_j + C_{sense}) \quad (1)$$

where C_j is the photodiode junction capacitance, C_{sense} is the sense-node capacitance, and I_{photo} is the photocurrent of the photodiode. The V_{sense} voltage reaches the reference level V_{ref} after

the T_{PWMOUT} time (Fig. 1b) which can be easily derived from (1) assuming that the C_j, C_{sense} and I_{photo} are constant during the conversion:

$$T_{PWMOUT} = (V_{reset} - V_{ref}) (C_j + C_{sense}) / I_{photo} \quad (2)$$

The T_{PWMOUT} time is converted to a digital number (DN) by the counter, which counts the clock pulses during the PWMOUT pulse. The number of clock pulses (DN_{OUT}) is a digital representation of T_{PWMOUT} as well as the intensity of light. The total time of the light-to-digital conversion (T_{ADC}) is equal to T_{PWMOUT}. Therefore, the digital result and time of the conversion are inversely proportional to the photocurrent:

$$T_{ADC} \sim 1/I_{photo} \quad (3a)$$

$$DN_{OUT} \sim 1/I_{photo} \quad (3b)$$

The relationships (3a) and (3b) explain the fundamental limitations in operation of the converter from Fig. 1a. First, the light-to-digital conversion can take a long time for poor lighting conditions. As a result, the frame rate is limited by the darkest pixels of a scene. Secondly, the light-to-digital conversion is nonlinear i.e. the DN_{OUT} does not depend linearly on the illuminance (or irradiance); instead, it is a reciprocal type of dependence. Nonlinearity of the sensor response makes it difficult to compensate for photo-response non-uniformity. Several ways to circumvent the limitations have been proposed in the works [6-10].

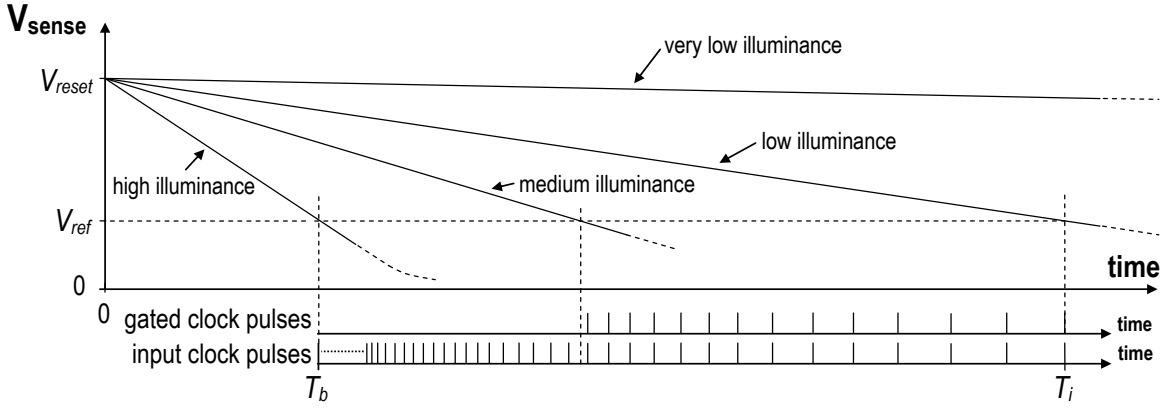


Fig. 2 *Principle of the nonlinear time mode conversion in pixel-ADCs (gated clock pulses for medium illuminance are presented).*

To obtain the linear response, a nonlinear time-to-digital conversion can be applied. Such conversion can be easily implemented by a digital counter working with a variable frequency clock [6]. The principle of the nonlinear conversion is presented in Fig.2. Unfortunately, this solution does not reduce the time of light-to-digital conversion. Dark scene would dramatically increase the conversion time. One of the conversion methods in which the

conversion time is much shorter is the classic voltage mode single-slope analog-to-digital converter, the operating principle of which is shown in Fig. 3.

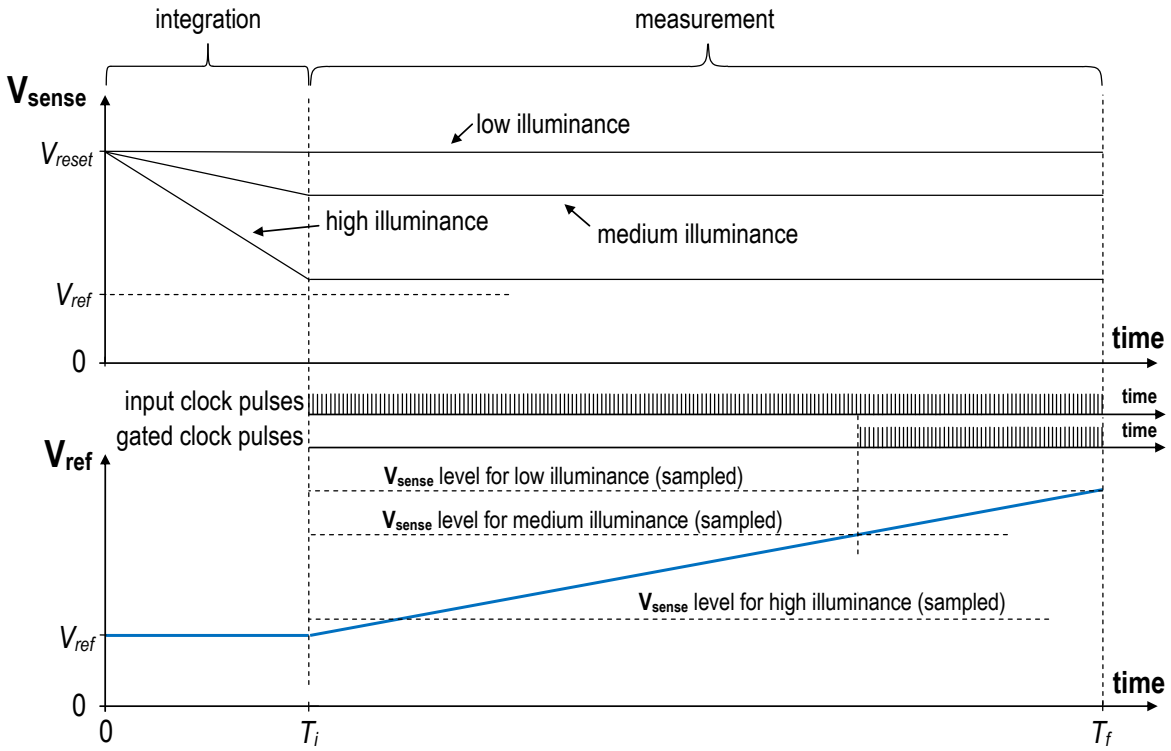


Fig. 3 *Principle of the voltage mode conversion in pixel ADCs (gated clock pulses for medium illuminance are presented).*

This mode of operation requires constant voltage on the sense-node during the measurement. This can be achieved using an additional sample-and-hold circuit. But in the presented imager the converter is implemented in a pixel so an additional sample-and-hold circuit would significantly increase its size. The sample-and-hold circuit will not be needed at all if the measurement time is much shorter than the integration time, which in typical conversion conditions is quite difficult to achieve (Fig. 3).

The voltage mode can be easily realized in the time mode converter by applying a variable reference voltage V_{ref}. In [7], discrete steps of V_{ref} were introduced during the time-to-digital conversion. In [8], a linear ramp of V_{ref} voltage was applied during the entire conversion process in order to obtain large dynamic range. In [9] a multi-ramp reference voltage readout scheme was proposed to extend the dynamic range and reduce the noise. In [10], an ADC with the functionality of a variable content-aware dynamic compression was presented, in which V_{ref}, after the time-to-digital conversion, increases in discrete steps (similarly as in a slope ADC), allowing the darkest parts of a scene to be visible.

The above examples show that existing ADC solutions do not allow simultaneous reduction of conversion time and preservation of linear light-to-digital characteristic. In this paper an improved technique of the analog-to-digital conversion with significantly shortened conversion time and good linearity is proposed. In the following sections, the principle of operation of the proposed ADC, conditions for obtaining linear conversion, and measurement results are presented and discussed.

2. Proposed ADC

2.1 Principles of operation

In a massively parallel imaging array, the control signals V_{reset}, V_{ref}, clock, reset pulse, etc. are common for all the pixel-ADCs. Waveforms of the V_{ref} and clock signals generated for the proposed conversion technique are shown in Fig. 4. The conversion cycle starts at the end of the reset pulse (zero on the time axis) and finishes at T_f. The clock pulses start after the blanking time T_b (this interval represents the illuminances exceeding the dynamic range of the converter) and stop at T_f. The intermediate time T_i defines the boundary between the time and voltage modes. Times T_b, T_i and T_f are the same for all the pixels. As can be seen in Fig. 4, in the proposed hybrid technique voltage mode is only used by dark pixels. If the V_{sense} capacitance discharges to the V_{ref} within time T_i, then the time mode is used, otherwise the voltage mode is realized.

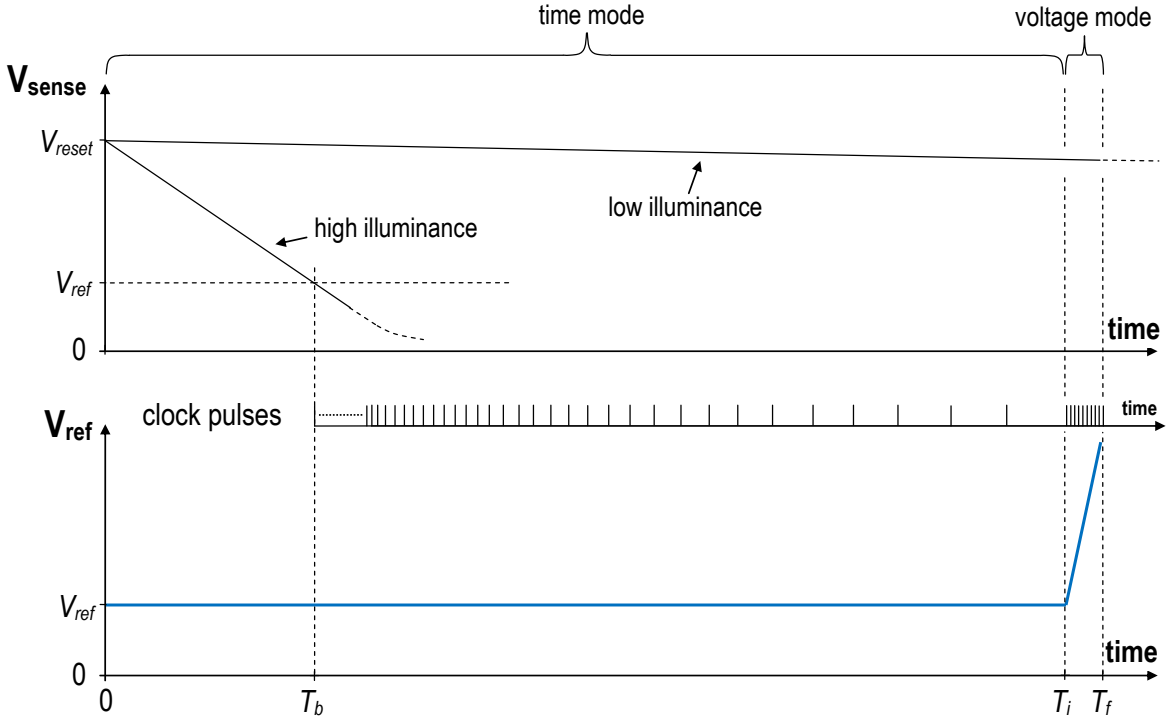


Fig. 4 *Principle of the hybrid conversion in the proposed pixel-ADC.*

Before T_i the voltage V_{ref} is constant. In order for the conversion of reciprocal characteristic like (3b) to be linear, the intervals between successive clock pulses are increased. T_b and time intervals between successive clock pulses can be calculated from the following equations:

$$T_b = (V_{reset} - V_{ref}) (C_j + C_{sense}) / I_{photo\_max} \quad (4a)$$

where I_{photo_max} is the photocurrent representing the maximum value of the ADC output.
The time $t(n)$ of the n-th occurrence of the clock pulse (counting from the end of the conversion) can be determined from the equation:

$$t(n) = \frac{(V_{reset} - V_{ref})(C_j + C_{sense})}{n \cdot I_{LSB}} \quad (4b)$$

where:

$(1+v) \leq n \leq (c - 1)$,

c is the number of counter states (for b-bit binary counter c is equal to 2^b),

v is the number of counter states assigned for the voltage mode,

I_{LSB} is the photocurrent representing one LSB of the ADC output.

I_{LSB} can be calculated from the following equation:

$$I_{LSB} = I_{photo\_max} / (c - 1) \quad (4c)$$

Finally, the time of the occurrence of the n-th clock pulse can be derived from:

$$t(n) = \frac{(c - 1)(V_{reset} - V_{ref})(C_j + C_{sense})}{n \cdot I_{photo\_max}} \quad (4d)$$

The time interval $\Delta t(n)$ between adjacent clock pulses can be determined from the following equation:

$$\Delta t(n) = t(n) - t(n + 1) \quad (4e)$$

where: $(1+v) \leq n \leq (c - 2)$

Finally, we get:

$$\Delta t(n) = \frac{(c - 1)(V_{reset} - V_{ref})(C_j + C_{sense})}{n(n + 1)\, I_{photo\_max}} \quad (4f)$$

Time delay between successive clock pulses as a function of the number of clock pulses for 9-bit counter with no voltage mode states is presented in Fig. 5. The largest distances

between clock pulses occur for the largest clock pulse count values. Assigning the final counter states to the voltage mode will reduce conversion time by orders of magnitude.

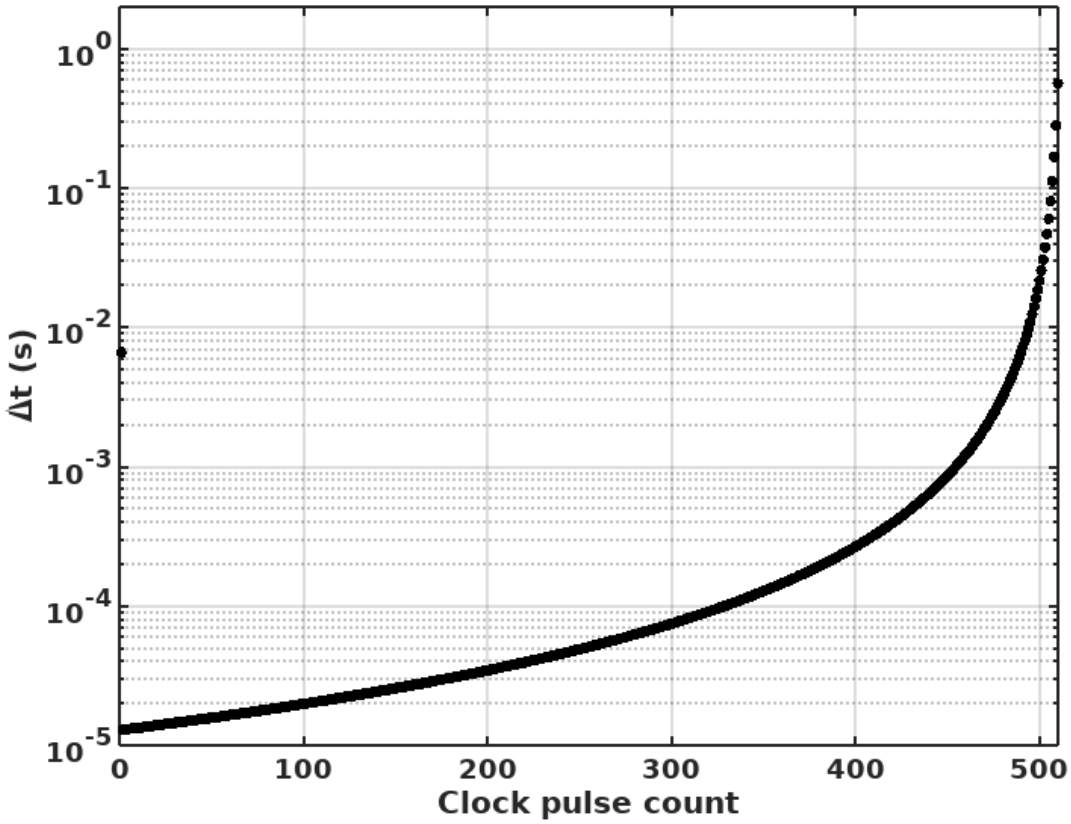


Fig. 5 *Time delay between successive clock pulses (Δt) as a function of the number of clock pulses for the time mode only operation.*

After time T_i, voltage V_{ref} takes the role of a ramp signal and V_{sense} is converted as in a single-slope ADC. In this mode, there is no need for a nonlinear clock, the clock frequency is immediately increased up to the maximum value (allowing the correct operation of a DAC used to generate V_{ref}), and the distance between clock pulses becomes constant.

In pixels under high illumination, pixel counters start counting when V_{sense} falls below V_{ref} (before the time T_i) and they count until T_f (the voltage mode cannot stop the counters). In pixels under low illumination, counters are not enabled before the time T_i. The counters start when the growing V_{ref} reaches V_{sense} level and they count until T_f. Owing to this the output value of ADC increases with increasing illuminance.

Before the time T_i, the V_{sense} signal is not constant, therefore this stage of conversion is called "time mode". During the next stage, the V_{sense} signal is treated as a constant sample, therefore the term "voltage mode" is used. The use of the voltage mode reduces the

conversion time of dark pixels (and thus the whole frame) by at least an order of magnitude. Fig. 4 shows that the maximum conversion time is T_f and it is not a function of light intensity:

$$\max(T_{ADC}) = T_f, \quad \text{and} \quad T_{ADC} \neq f(I_{photo}) \tag{4g}$$

2.2 Conversion linearity

Both conversion modes are linear. However, for the whole conversion to be linear, i.e. to satisfy:

$$DN_{OUT} \sim I_{photo} \tag{5a}$$

the modes must be properly "glued". This requires two conditions to be met. For better explanation, more detailed waveforms are shown in Fig. 6 and Fig. 7.

The first condition of the linear conversion is that the voltage-mode processing time (from T_i to T_f in Fig. 6) should be much shorter than the time interval between two last pulses of clock in the time mode (from T_z to T_i in Fig. 6):

$$T_f - T_i << T_i - T_z \tag{5b}$$

If inequality (5b) is satisfied, then the change of V_{sense} after T_i can be neglected (the voltage mode can be used directly, without a sample-and-hold circuit). In the ADC implemented in this work, the time interval from T_i to T_f is 18.4 μs and from T_z to T_i is 14 ms, so the condition of the linear conversion (5b) is fulfilled well. In Fig. 6, the time axis is drawn using different scales for the two modes, so the waveforms of V_{sense} seem to be flat after T_i = 225 ms.

The second condition is that one LSB should represent the same variation in the illumination level of the pixel, whatever conversion mode has been used (time mode or voltage mode):

$$V_{LSBt} = V_{LSBv} \tag{6a}$$

where:

V_{LSBt} is a voltage at the sense node representing one LSB of the time mode,

V_{LSBv} is a voltage at the sense node representing one LSB of the voltage mode.

At time T_i, the V_{sense} and V_{ref} signals change in the roles — the V_{sense} signal becomes a constant signal and the V_{ref} signal becomes a variable ramp signal (blue waveform V_{ramp} in Fig. 6). If the condition (6a) is satisfied, then this role change does not introduce nonlinearity to the analog-to-digital conversion. The condition (6a) can be met by choosing the proper number of clock pulses in both modes.

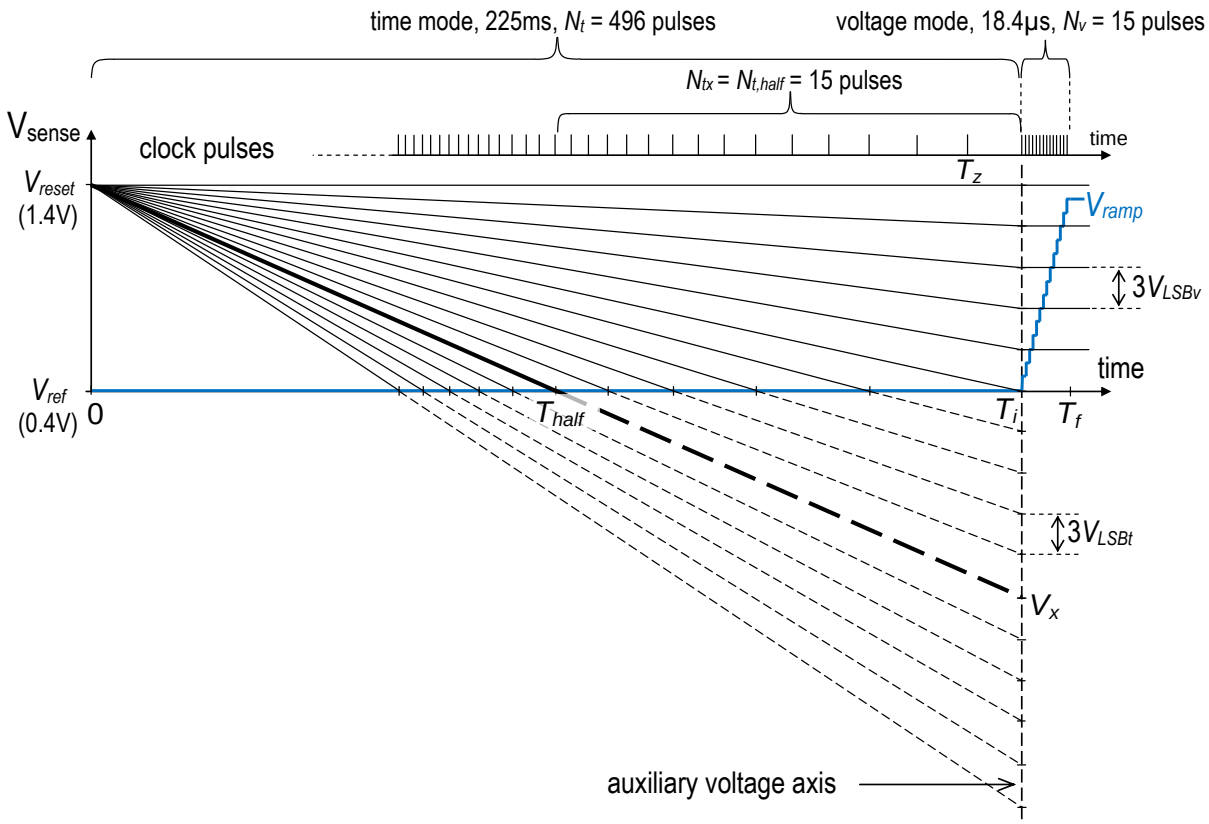


Fig. 6 *Waveforms of an analog-to-digital conversion in the hybrid mode (a time mode followed by a voltage mode).*

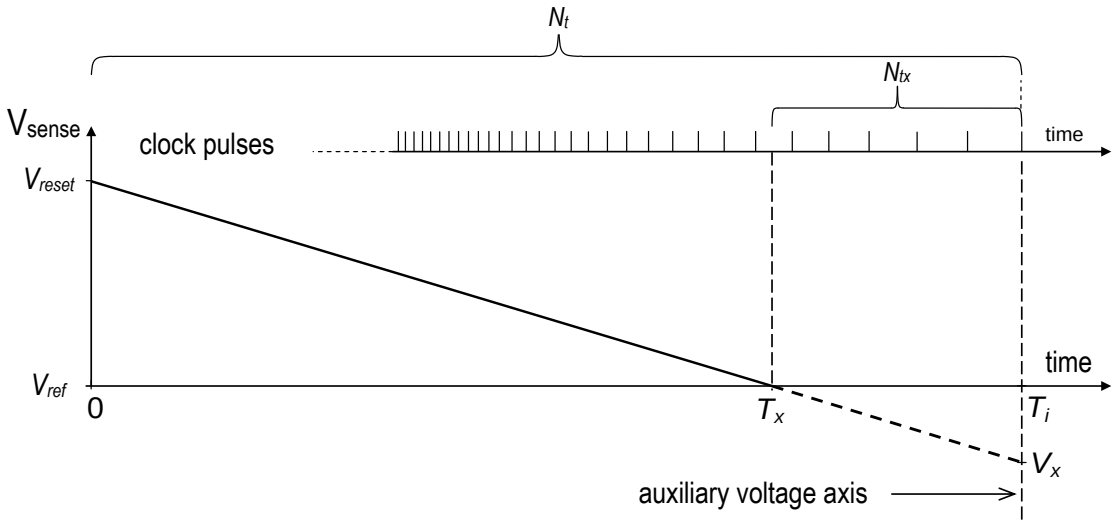


Fig. 7 *Definition of the V_x voltage.*

In the voltage mode, the value of V_{LSBv} is related to the number of clock pulses (quantization levels) assigned for this mode (N_v) and to the range of the sense-node voltage with the simple formula:

$$V_{LSBv} = (V_{reset} - V_{ref}) / N_v \qquad (6b)$$

For the time mode, the V_{LSBt} can be determined by a graphical method. For this purpose, in Fig. 6, on the additional time axis, clock pulses have been drawn (single pulse corresponds to 1 LSB). In addition, in Fig. 6, diagrams of V_{sense} are plotted for the quantized illuminance values (every 3 LSB to keep the graph clear). These graphs intersect with the time axis at the moments of clock pulses. The extensions of these diagrams (dashed lines) intersect with the auxiliary voltage axis. The voltage at the intersection point is denoted as V_x. Figure 7 shows a definition of the V_x voltage more clearly. This can be considered equivalent to the application of a voltage-mode approach, where the voltage variation $\Delta V_{LSBt} = V_{ref} - V_x$ is converted in digital by counting the N_{tx} pulses of the pixel clock from the time T_x to the time T_i (Fig. 7). As a consequence, the V_{LSBt} can be calculated using the following formula:

$$V_{LSBt} = (V_{ref} - V_x) / N_{tx} \tag{6c}$$

It can be seen from Fig. 6 that for V_x chosen that $T_x = T_{half} = 0.5\ T_i$ the following equation is satisfied:

$$V_{reset} - V_{ref} = V_{ref} - V_x \tag{6d}$$

Equations (6b), (6c) and (6d) show that condition (6a) will be satisfied when: $N_v = N_{tx}$ and $N_{tx} = N_{t,half}$. That is: $N_v = N_{t,half}$. Finally, the second condition is that the number of steps on V_{ramp} (i.e. the number of clock pulses in the voltage mode) must be equal to the number of clock pulses used for the second half of the time mode (from T_{half} to T_i).

In the presented ADC, $N_v = 15$ steps were used for the ramp signal (this is shown in Fig. 6). This number of steps was chosen as a trade-off between the conversion time and the linearity of the conversion resulting from the condition (5b).

2.3 Conversion time

Assuming the V_{sense} waveforms are straight lines, the light-to-digital conversion using the hybrid mode is exactly N_v times faster than the conversion using only the time mode [6] (this can also be deduced from the graphs in Fig. 6). In the implemented ADC, the conversion time in the hybrid mode is $T_{ADC} = 225$ ms + 18.4 μs. When using only the time mode, the conversion time would be $15 \cdot 225$ ms = 3375 ms.

The following algorithm (Matlab or Octave) can be used to calculate intervals between successive clock pulses for time mode only and for hybrid time and voltage mode. Main system clock is the constant frequency system clock which is used in the measurement system (described in section 3.2) to generate the variable pixel clock. The number of main system clock cycles should be set according to the chosen conversion time and frequency of the main

system clock. In the presented example 100 MHz is the frequency of the main system clock and the conversion time is set to 3375 ms (337,500,000 main system clock cycles). Number of pixel's counter states is set to 512 (9-bit counters) and the number of voltage mode cycles is set to zero (the following example uses time mode only).

```
% number of main system clock cycles before reduction:
clock_cycles = 337500000;
% number of pixel's counter states:
counter_states = 512;
% number of voltage mode clock cycles:
voltage_mode_cycles = 0;
% local variables:
previous = 0;
reduced_clock_cycles = 0;
% main loop:
for dn = counter_states-1:-1:voltage_mode_cycles+1
  current = round(clock_cycles/dn);
  diff = current - previous;
% number of main system clock cycles for every DN value is printed:
  fprintf('DN: %3d   cycles: %d\n', dn, diff);
  reduced_clock_cycles = reduced_clock_cycles + diff;
  previous = current;
end;
fprintf('Number of main system clock cycles for time mode conversion:
%d\n', reduced_clock_cycles);
```

The algorithm gives the following result (lines from the middle of the printout are omitted):

```
DN: 511   cycles: 660470
DN: 510   cycles: 1295
DN: 509   cycles: 1300
DN: 508   cycles: 1305
DN: 507   cycles: 1310
DN: 506   cycles: 1316
DN: 505   cycles: 1321
.....
DN:  15   cycles: 1406250
DN:  14   cycles: 1607143
DN:  13   cycles: 1854395
DN:  12   cycles: 2163462
DN:  11   cycles: 2556818
DN:  10   cycles: 3068182
DN:   9   cycles: 3750000
DN:   8   cycles: 4687500
DN:   7   cycles: 6026786
DN:   6   cycles: 8035714
DN:   5   cycles: 11250000
DN:   4   cycles: 16875000
DN:   3   cycles: 28125000
DN:   2   cycles: 56250000
DN:   1   cycles: 168750000
Number of main system clock cycles for time mode conversion: 337500000
```

The first calculated number of cycles (660,470) corresponds to a blanking time T_b (illumination exceeds the dynamic range of the converter). Each successive value means the number of main system clock cycles (100 MHz) corresponding to one successive cycle of the pixel clock (1 LSB step of the result).

To calculate the conversion time reduction after switching on the voltage mode the number of quantization levels in voltage mode has to be defined:

```
% number of voltage-mode clock cycles:
voltage_mode_cycles = 14;
```

and we get the following result of the algorithm (only final lines of the printout are presented):

```
.....
DN:  20   cycles: 803571
DN:  19   cycles: 888158
DN:  18   cycles: 986842
DN:  17   cycles: 1102941
DN:  16   cycles: 1240809
DN:  15   cycles: 1406250
Number of main system clock cycles for time mode conversion: 22500000
```

It is evident that the number of main system clock cycles needed for conversion in the time mode has been reduced from 337,500,000 to 22,500,000 (i.e. 15 times). The conversion time of the voltage mode (18.4 μs) has to be added to achieve the total conversion time. The cycle counts calculated by the presented algorithm were directly used to configure the variable frequency pixel clock generator implemented in the FPGA.

3. Measurements

3.1 Experimental pixel-ADCs

In order to verify the proposed technique, 128 pixel-ADCs were implemented in a prototype integrated circuit. The chip has been fabricated in the 0.18 μm 1.8 V CMOS process of ams AG. The pixel-ADCs form a line (bottom row of the array) and have pitch of 20 μm (Fig. 8). The number of 128 pixels is relatively small, however, it allows to obtain reliable results in statistical measurements of fixed pattern noise (FPN).

The simplified schematic diagram of the implemented pixel is presented in Fig. 9. The implemented pixel uses a latch to synchronize the PWMOUT signal with the clock. After the synchronization it can be safely used for clock gating. The analog reset switch was implemented as a n-channel MOS transistor. A 9-bit counter with an asynchronous reset has been used for the conversion. The digital output from the counter is connected through three-state buffers to the common bus (for all 128 pixels). Three-state buffers are activated by a

signals from a 7-bit address decoder. Owing to this it is possible to read the state of any counter. The photodiode Ph was implemented as an exposed drain to substrate junction of the n-channel MOS transistor (n+ diffusion to p substrate). This transistor can also act as a switch, which separates the photodiode from the comparator for experimental purposes. Such photodiode exhibits a relatively low sensitivity, but this is of secondary importance in this experiment. The pixel size is 20 μm x 20 μm.

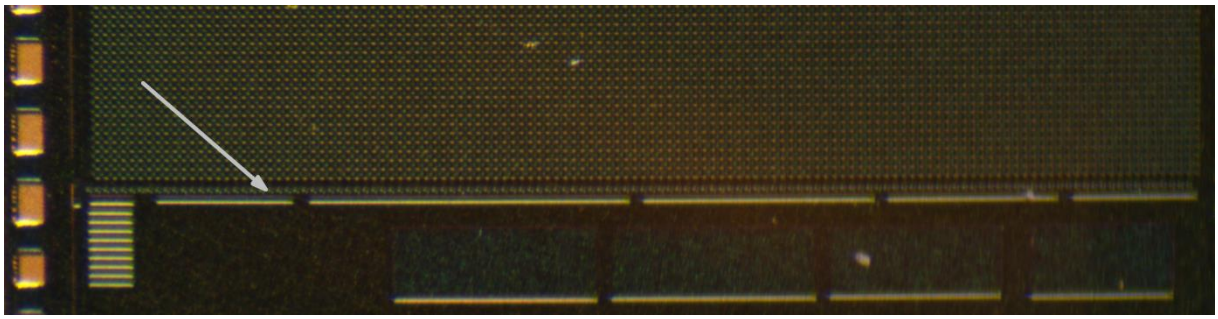


Fig. 8 *Chip microphotograph – the fragment with the 128 pixel-ADCs (bottom row indicated by arrow).*

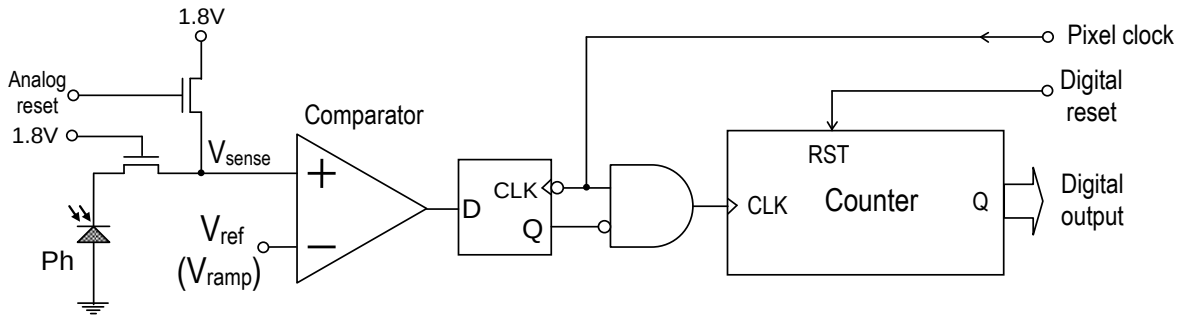


Fig. 9 *Schematic diagram of the measured pixel-ADC.*

3.2 Measurement system

The measurements were performed using a modified version of measurement system specialized for image sensors [11]. Figure 10 shows a simplified block diagram of the measurement system used for testing and measurements of the described CMOS image sensor. The measurement system, data acquisition and processing are controlled by a FPGA circuit and a PC computer. The generator of imager control signals and the measurement accelerator have been implemented in the hardware using Xilinx Virtex-6 FPGA. This module marked in Fig. 11 as Image Sensor Controller (ISC) allows for efficient and automated realization of various types of measurements. The unit generates the signals controlling the imager, acquires pixel data from the imager, and controls the DAC converter that generates

the V_{ref} signal. Furthermore, the ISC unit is responsible for communication with the MicroBlaze processor with on-chip program and data memory, working under Linux operating system. The Ethernet controller is responsible for communication with a PC. The USB permits realization of the console interface for Linux system in the MicroBlaze processor. The additional interval memory stores delay data (Fig. 5) for ISC's variable frequency pixel clock generator. This memory is written by the MicroBlaze processor with data calculated on the PC by the algorithm presented in section 2.3. The measurement data is processed and visualized in a PC machine equipped with a mathematical software Octave. The PC is also used to perform FPGA board configurations (using the JTAG programming interface) and to modify the measurement control software implemented in the MicroBlaze processor. The file system of the PC is made accessible for MicroBlaze through the Network File System (using the Ethernet interface), which facilitates access to the measurement data on the FPGA. The main control application (executed in MicroBlaze processor on the FPGA board) has been written in C programming language. It realizes the measurements described in the following sections.

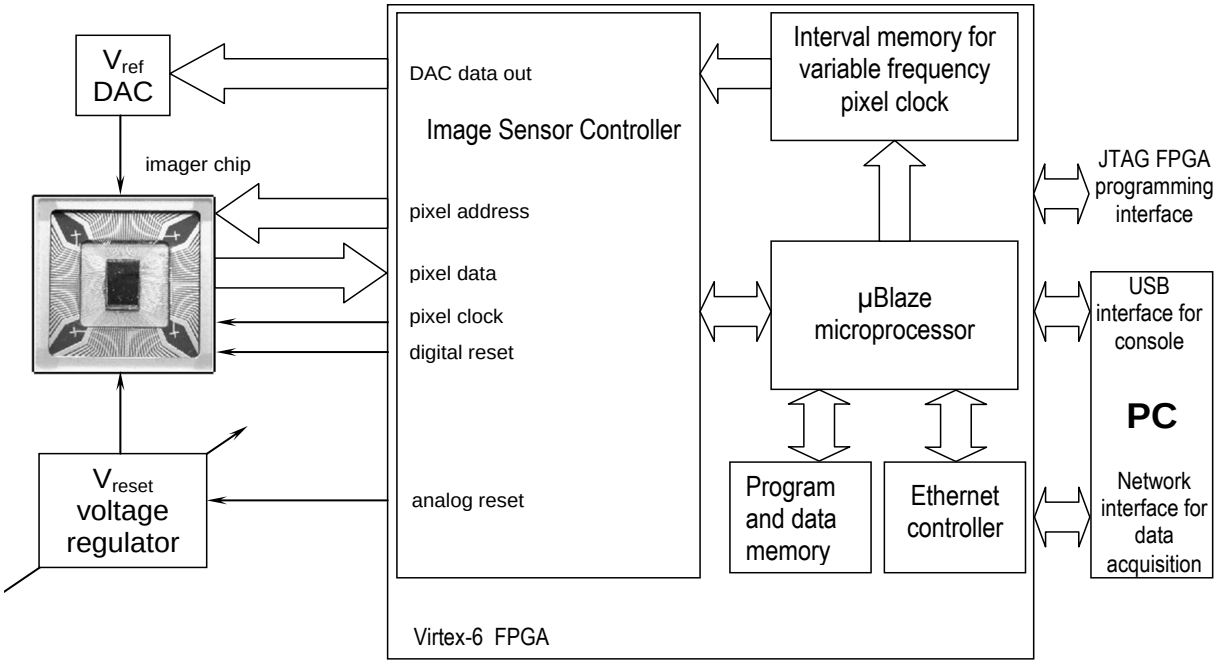


Fig. 10 *Simplified block diagram of the measurement system.*

3.3 Power consumption

In the Table 1 the measured power consumption of the single pixel during the conversion and the energy consumed per conversion for the single pixel are presented for the dark and for the light condition.

Table 1. *Power and energy consumption per pixel for the measured imager under dark and light conditions.*

Operating mode	Illuminance condition	Power consumption (analog part)	Power consumption (digital part)	Energy per conversion (analog part)	Energy per conversion (digital part)
Time only	Dark	232 nW	292 pW	783 nJ	986 pJ
Hybrid	Dark	127 nW	343 pW	28.58 nJ	77.18 pJ
Time only	Light	649 nW	286 pW	2190 nJ	965 pJ
Hybrid	Light	787 nW	472 pW	177.1 nJ	106.2 pJ

The analog part means the comparator and the analog reset circuit. The analog part is powered from the 1.8V source. The digital part consists of three components: the synchronizing flip-flop, the gate and the counter. Digital part is powered from the 1.2V source. The power has been measured during the conversion. The conversion time in the time mode is 3.375 s and in the hybrid mode it is shortened to 225 ms. The energy consumption per conversion in the hybrid mode is the lowest due to the reduced conversion time.

3.4 Integral nonlinearity

Figure 11 shows the measured integral nonlinearity (INL) of the pixel photoconversion characteristic for the time mode (exclusively) [6] and the proposed hybrid mode. The presented results are the average of 90 measurements of 128 pixels. The nonlinearity of ±2 LSB is observed in both modes because the reciprocal response is not fully compensated due to parasitic leakage currents and nonlinear capacitances of the photodiode and sense-node. The hybrid-mode INL is very similar to the time-mode INL with the exception of the low-irradiance region. In this region, the voltage mode is active and the INL is higher and changes rapidly. To analyze and explain this behavior, more measurements have been performed.

Figure 12 shows the low-irradiance part of the pixel photoconversion characteristics for the hybrid mode (average results of 90 measurements of 128 pixels are presented). For an output code equal to the number of ramp steps N_v, the transition from the voltage mode to the time mode takes place. Figure 12 shows the photoconversion characteristics for different number of ramp steps (10, 15 and 25). The graph indicates that the best linearity is achieved for the 15 ramp steps, which confirms the theoretical predictions from section 2.2. However, there is still a significant nonlinearity in the voltage-mode region compared to the time-mode region.

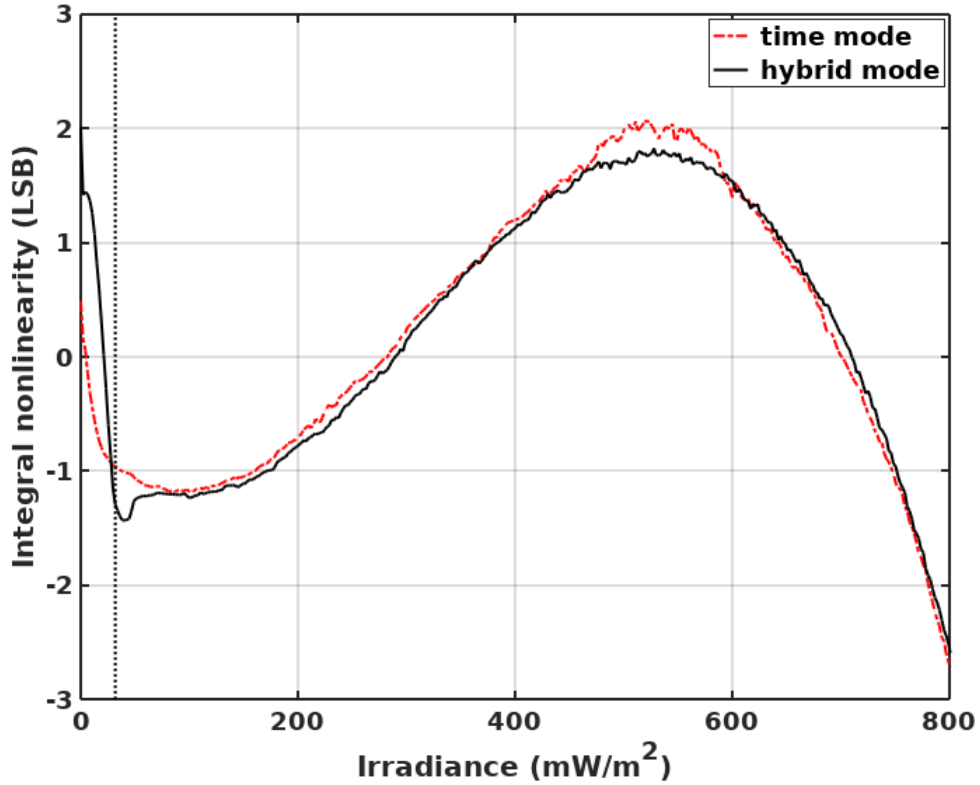


Fig. 11 *Measured INL of the photoconversion characteristic of a pixel operating in the time mode (only) and the proposed hybrid mode. The vertical dotted line shows the irradiance at which switching from voltage to time based conversion takes place in the hybrid mode.*

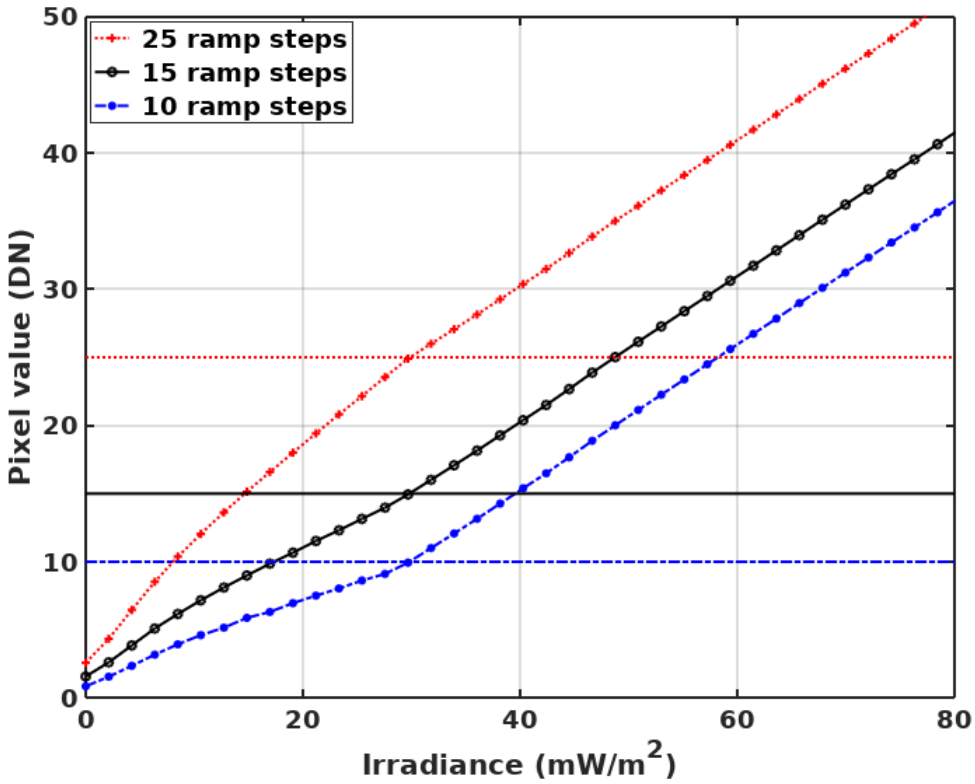


Fig. 12 *Measured photoconversion characteristics in the hybrid mode for different numbers of ramp steps: 10, 15 (theoretical optimum) and 25. Horizontal lines depict the boundary between voltage-mode (bottom part) and time-mode (top part) phase of the conversion.*

The voltage mode is less resistant to the nonlinearities of the photodiode and sense-node capacitances than the time mode (in the time mode the conversion always ends with the same voltage level at the photodiode and the sense-node whereas in voltage mode the voltage level at the photodiode and the sense-node is variable at T_f).

3.5 Optimization of the ramp signal

To reduce the voltage-mode nonlinearity (i.e. nonlinearity of hybrid mode at low irradiance), a ramp with unequal steps should be generated. The hardware-in-the-loop optimization implemented in the specialized measurement system [11] found the optimum levels for all the 15 steps of the ramp (the optimization was based on Luus-Jaakola stochastic algorithm [12]). It can be seen in Fig. 13 that the resulting ramp is nonlinear. With this ramp, the distortion of the photoconversion characteristic at low irradiance is substantially reduced, what is visible in Fig. 14.

The optimization was performed to also reduce the ADC conversion offset (the offset is mainly due to a leakage present at the sense-node). The optimization procedure succeeded to reduce most of the offset. The offset reduction has been achieved by lowering the final level (last step) of the ramp. The reduction of the offset resulting from the optimization procedure is visible in Fig. 14. The hybrid-mode photoconversion characteristics for the unequal-step ramp is almost identical to the original time-mode photoconversion characteristics, however in the hybrid mode the analog-to-digital conversion is much faster according to the results presented in section 2.3.

Figure 15 depicts measured integral nonlinearity of the low-irradiance region for hybrid mode with equal-step (original) ramp, for hybrid mode with unequal-step ramp (optimized), and for time mode (only). It is evident that the unequal-step ramp reduced the low-irradiance INL significantly.

3.6 Compensation of fixed pattern noise

The INL measurement is a typical test of a pixel's linearity. An alternative and interesting linearity test may be an indirect test involving the use of photo-response non-uniformity (PRNU) compensation. If the pixel responses are linear, then the simple PRNU compensation, which is based on a gain correction (multiplying the pixel response by a constant coefficient), will be effective. The PRNU compensation for all 128 pixels working in hybrid mode was performed and results are shown in Fig. 16. The PRNU, i.e. the light component of FPN, has been substantially reduced. A small dark-signal non-uniformity remains due to the lack of the correlated double sampling technique.

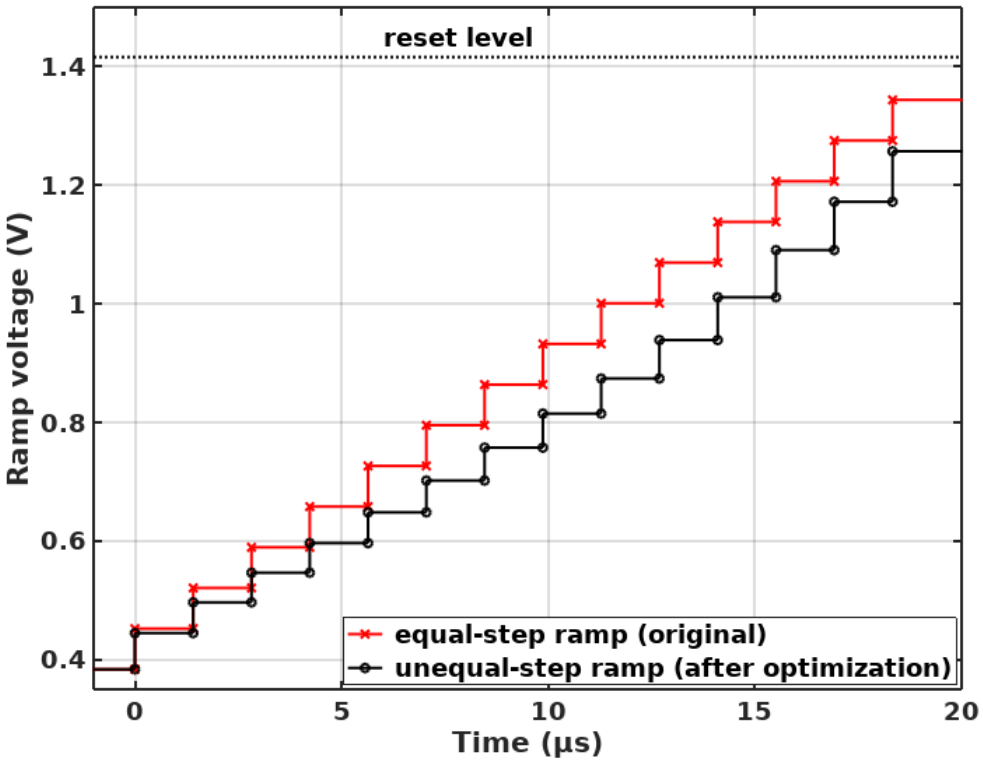


Fig. 13 *Ramp signal before and after offset and linearity optimization of the hybrid-mode pixel-ADC.*

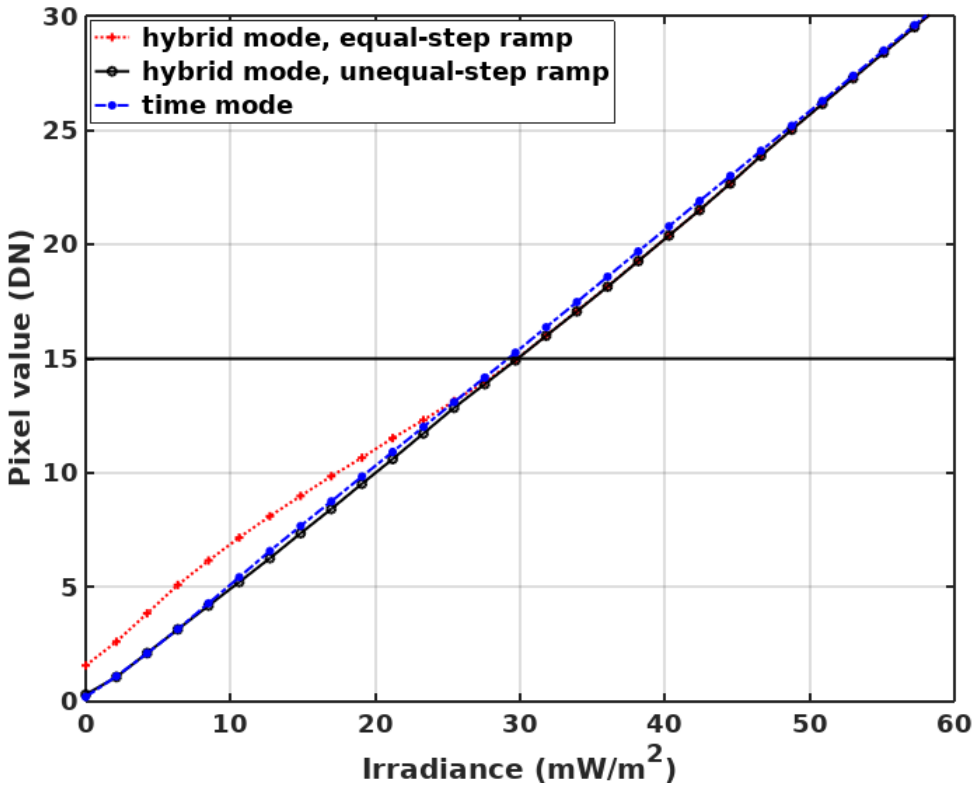


Fig. 14 *Measured photoconversion characteristics for different modes and ramps: hybrid mode with equal-step (original) ramp, hybrid mode with unequal-step ramp (optimized), and time mode (only). Horizontal line depicts the boundary between voltage-mode (bottom part) and time-mode (top part) phase of the conversion.*

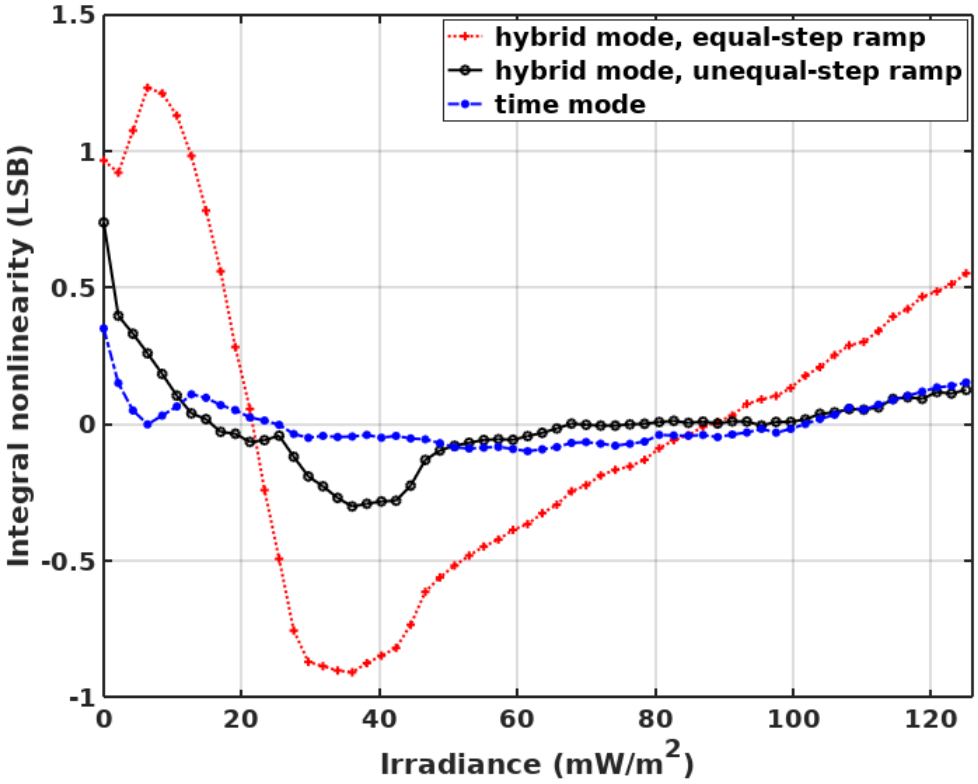


Fig. 15 *Measured INL of the low-irradiance region for different modes and ramps: hybrid mode with equal-step (original) ramp, hybrid mode with unequal-step ramp (optimized) and time mode (only).*

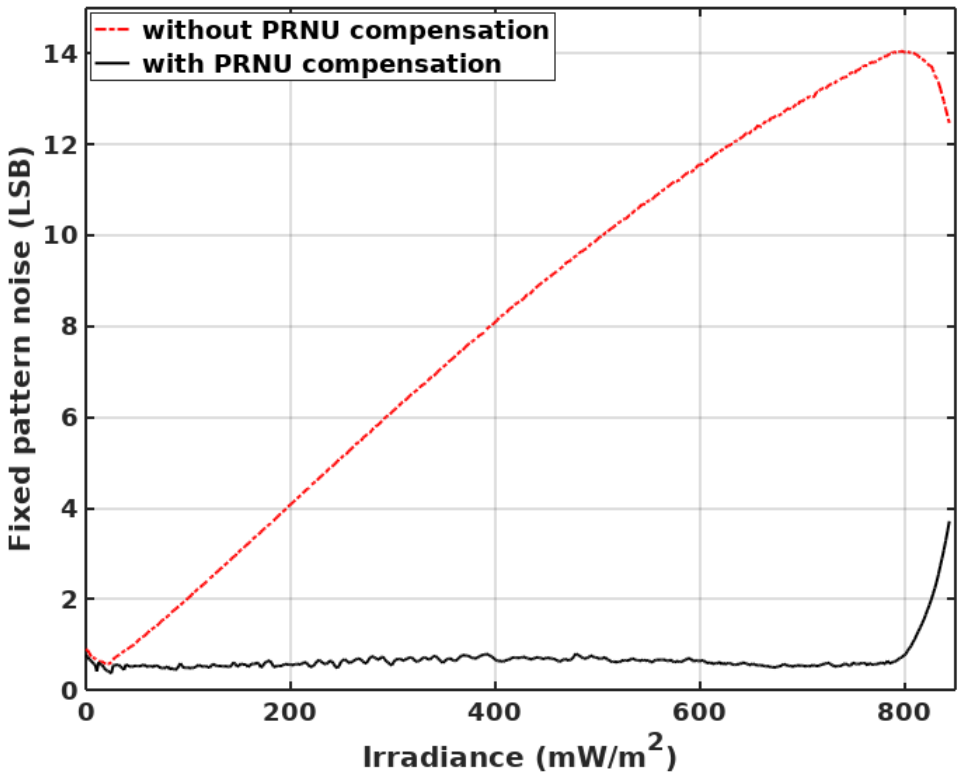


Fig. 16 *Measured FPN of 128 hybrid-mode pixels before and after the PRNU compensation.*

Fig. 16 also shows an increase in the PRNU for irradiance approaching saturation. Without the gain correction, the PRNU for irradiance close to the saturation region decreases (because all pixels reach the same maximum value). With the gain correction, the reverse process will take place — the saturation will cause the PRNU to appear again. This can be counteracted by enforcing the upper limit of the pixel output value after the PRNU compensation (the same limit for all the pixels). This limit can be defined as the lowest pixel saturation level after the PRNU compensation. More information on the PRNU compensation can be found in [13].

4. Conclusion

The paper presents a modification to the time-domain based integrating ADC that significantly accelerates the analog-to-digital conversion. The technique is based on changing the mode of ADC operation from time mode to single-slope mode (voltage mode) during the conversion. In the example presented the conversion time has been reduced 15 times (in [7] 70% reduction has been reported). Greater reduction is possible when more levels of a ramp signal are used. The linearity of the conversion is retained by careful selection of the mode change time and the number of ramp levels. This allows simple ADC gain correction and PRNU compensation, which is important for image quality. In addition, good PRNU compensation makes it difficult to use the sensor to identify the image source (PRNU can be used as a fingerprint of realized photographs [14]). The nonlinearity of a sensor may also limit its scientific applications (for example photometric). The image sensors nonlinearity can be effectively mitigated by improving the analog part of ADCs implemented in the sensors [15,16]. Another technique that can reduce the nonlinearity of the sense-node and photodiode is compensation using a nonlinear ramp calculated by the optimization algorithm (presented in section 3.5).

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