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A Single-Carrier-Based Pulse-Width Modulation Template for Cascaded H-Bridge Multilevel Inverters

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ABSTRACT Multiplicity of the triangular carrier signals is a criterion for the extension of sinusoidal pulse-width modulation, SPWM, to a number of output voltage levels per phase-leg in cascaded H-bridge (CHB) multilevel inverter (MLI). Considering medium and high voltage applications where appreciable number of output voltage levels from CHB MLI is needed, commensurate high number of carrier signals in either classical level- or phase-shifted SPWM scheme for this inverter is inevitable. High-quality output waveforms from CHB MLI system demands precise synchronization of these multi-carrier signals. Sampling issues, memory constraints and computational delays pose difficulties in achieving this synchronization for real-time digital implementation. This study presents a PWM template for CHB MLI. The developed control concept generates adequate modulation templates for CHB inverter wherein a sinusoidal modulating waveform is modified to fit in a single triangular carrier signal range. These templates can be used on CHB inverter of any level with no further control modification. Nearly even distribution of switching pulses, equal sharing of the overall real power among the constituting power switches and enhanced output voltage quality were achieved with the proposed modulation. For a 3-phase, 7-level CHB, simulation and experimental results, for an R-L load, were presented.

INDEX TERMS Cascaded H-bridge inverter, sinusoidal pulse-width modulation, total harmonic distortion.

I. INTRODUCTION

In recent time, the field of power electronics has witnessed appreciable boost in the areas of power-conditioning circuit topologies and their corresponding control/modulation strategies. This trend is a direct response to the global quest and search for sustainable and more environmental-friendly electrical power sources and utilizations. In this scenario, inverters/dc-ac converters are among the cardinal power electronics devices deployed in various key areas such as high-voltage direct-current (HVDC) transmission, [1], [2], Flexible AC Transmission Systems (FACTS), [3], [4], renewable energy grid integration, [5]–[8], railway and vehicle traction, [9]–[11], energy storage systems, [12], marine propulsion, [13], solar water pumping system, [14], grinding and rolling mills, [15], compressors and extruders, [16], to mention. Such deployment requires certain criteria to be met by the power electronics inverters of which high output voltage and a range of operational output power quality indices are crucial. The multilevel inverter, MLI, is the best device for the provision of these requirements, [17].

Awareness of the inherent potentials of MLIs and their positive impacts on series of industrial applications have led to the proliferation of multilevel inverter power circuit configurations, as reported in the literature, [18]–[20]. Critical assessment of these newly evolved MLI topologies shows that they are actually either a hybrid or an off-shoot of one of the conventional MLI configurations: cascaded H-bridge (CHB), diode-clamped and capacitor-clamped (flying capacitor) multilevel inverters. With the exception of the CHB MLI, the often-used fundamental MLI configurations have been limited to the syntheses of 3-level output voltages due to the inherent operational imbalance in the constituting capacitor banks' voltages. These 3-level configurations have attained

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industrial maturity and commercially available for the past years. On the other hand, the CHB MLI topological feature allows the syntheses of feasible multilevel output voltages, depending on application. Therefore, regarding scalability, modularity and overall improved power quality, the CHB MLI is often the chosen option for high-voltage/power deployment, [17].

The most popularly used modulation scheme for the control of the amplitude and frequency of the synthesized output voltage waveform of CHB MLI is the triangular carrier-based sinusoidal pulse width modulation, SPWM. Its concept of generating gating signals is inverter-phase-leg based. This precisely implies that the same control concept is repeated in each phase of the inverter; the only modulating parameter difference is the phase angle shift. Precisely, the control concept involves the comparison a high frequency triangular carrier wave with a fundamental frequency sinusoidal modulating signal; setting the zero-sequence signal to zero. In effect, SPWM presents no rigorous and complex computational difficulties and its extension to multilevel and/or multiphase systems involves only a multiplicity of the triangular carrier and sinusoidal modulating signals.

It is factual that the Level-shifted (LS) and Phase-shifted (PS) pulse width modulations are the two broad versions of the SPWM technique that have been well established in the literature, [21]–[25], for CHB MLI. In-phase disposition (IPD) variant of the LS PWM exhibits the best harmonic performance amongst all these modulation techniques; whereas the harmonic performance of the alternative phase-opposite-disposition (APOD) of the LS PWM is same with that of PS SPWM scheme, [23], [26]. Regarding uniform distribution of switching pulses among power switches of the constituting cascaded cells and even power delivery from each of the CHBs, the PS PWM claims superior modulation performance. In order to merge these good modulation features inherent in IPD and PS PWM schemes, various approaches have been proffered for this combinational concept as demonstrated in [27]–[30].

As aforementioned, multiplicity of the triangular carrier signals is a basic criterion for the extension of SPWM to a number of output voltage levels per inverter phase-leg. In other words, each of the synthesized output voltage levels in an inverter phase-leg is tagged to a generating triangular carrier. Considering medium and high voltage applications where appreciable number of synthesized output voltage levels from CHB MLI is needed, commensurate high number of triangular carrier signals in either classical LS or PS SPWM scheme for this inverter configuration is inevitable. And high-quality output parameter waveforms from the CHB MLI system demands precise synchronization of these multi-carrier signals. For real-time digital implementation of the SPWM techniques, sampling issues, memory constraints and computational delays pose difficulties in achieving this synchronization and tend to negatively affect the dynamic performance of digitally controlled CHB MLI, [31], [32].

In quest of removal of this conventional requirement of many carrier waveforms in SPWM, the works done in [33] proposed a modified SPWM scheme wherein the sinusoidal modulating signal is modified to fit in a single triangular carrier range of 0 to 1 in order to generate multi-level waveforms at the output of multilevel converter. In application, this modulation scheme was solely devoted to the more recently developed modular multilevel converter, MMC. Summarized overviews of the features of this SPWM approach are: only one triangular carrier signal is needed per phase; multi-carrier synchronization issues are completely avoided, resulting in easier digital controller implementation; involves simple mathematical operations, resulting in computationally less complex system; identical performance with the existing PS SPWM; it can be extended to MMC with a large number of sub-modules without further modifications. Narrowing down this modulation concept to CHB MLI adaptation, a modified SPWM scheme was proposed for CHB MLI in [34]. Therein, it was demonstrated that in-phase disposition (IPD) SPWM strategy could be deployed in the syntheses of multi output voltage levels in CHB MLI using only one triangular carrier signal irrespective of the number cascaded H-bridge units. It is factual that the authors in [34] did present a simplified implementation algorithm for their proposed control approach; however, it is glaring that the undesirable features of IPD SPWM still trail their modulation scheme: uneven distribution of switching signals among the constituting power switches and unequal sharing of the overall inverter output power among the CHB units. These are the modulation characteristic features that gave phase-shifted SPWM a leading edge over in-phase level-shifted SPWM in the control of CHB MLI. Therefore, integration of these features in the single carrier SPWM concept is thus needful to attenuate this gap.

To fill this gap, this paper presents a single carrier-based PWM template for cascaded H-bridge multilevel inverter. Its operational concept, as in [33], is derived from the operational principle of in-phase disposition level-shifted SPWM wherein the sine modulating waveform is modified to fit in a single triangular carrier signal range in order to generate the desired output waveform template for the MLI. The obvious innate drawback of this in-phase disposition level-shifted SPWM (non-distribution of switching signals to power switches and unequal output power sharing) is effectively removed from the modulation scheme following a simple reverse-voltage-sorting algorithm. In effect, the proposed control approach results in a hybrid modulation scheme that mediates between the phase- and level-shifted carrier-based SPWM techniques; thereby inheriting the good features in these two modulation schemes. Simulation and experimental results are shown for a 3-phase, 7-level CHB inverter.

II. CASCADED H-BRIDGE MULTILEVEL INVERTER

Basically, the power circuit configuration of a CHB MLI, shown in figure 1, is a series connection of H-bridge inverter unit cells. Each of the H-bridge cells has a capacitor bank

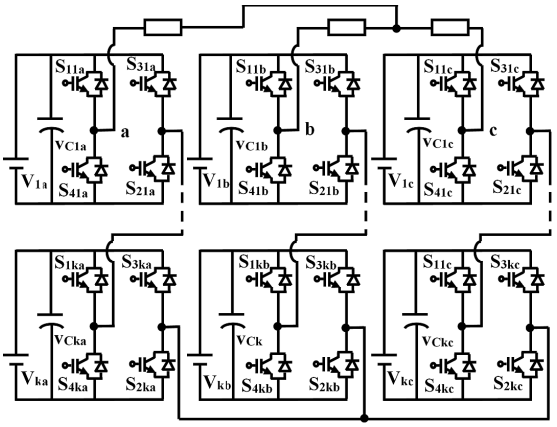

FIGURE 1. Cascaded H-bridge multilevel inverter power circuit.

TABLE 1. Comparison of phase-shift (PS) and proposed spwm schemes.

Compared parameter	Modulation scheme	
	PS PWM	Proposed scheme
Number of triangular carriers per phase	$2N$	1
Number of modulating signals per phase	1	2
Algorithm execution time (μs)	2.85	2.62

serving as the isolated dc-link voltage. The source to this capacitor bank is usually provided by either multi-winding transformer secondary via full bridge rectifier circuit or battery banks. High output voltages can be synthesized from this circuit arrangement by simply increasing the number of series unit cells with much lesser-voltage-rated components. Considering phase '*a*' in Fig. 1, for k number of cascaded inverter units, g_{1ja} g_{3ja} *and* g_{4ja} g_{2ja} are the switching functions of the upper and lower switches, respectively (where $j = 1, 2, 3, \ldots k$). Each of these switching functions has a value of 1 when the corresponding device is turned on and 0 otherwise; thus, they represent the switching states of their corresponding power devices. Also, in each inverter leg, the corresponding switching functions are complementary. Each inverter unit generates three output voltages of values $+V_{dc}$, 0 and $-V_{dc}$ (V_{dc} is the equal capacitor dc link voltages) from four different binary combinations of these switching functions. The complementary nature of the inverter switching functions greatly simplifies their logical truth-table representations.

It can then be inferred from table 1 that the overall inverter output voltage for k cascaded units in phase a is given by

$$\sum_{j=1}^{k} v_{aj} = V_{dc} \sum_{j=1}^{k} \left(g_{1j} - g_{3j}\right). \tag{1}$$

where g_{1j} and g_{3j} are the switching states of the upper switches in *jth* cascaded unit.

III. PROPOSED SINGLE-CARRIER-BASED SPWM TEMPLATE

As stated in the introductory section, the proposed modulation scheme is an offshoot of IPD level-shifted SPWM where the multi triangular carrier signals are virtually represented by a single carrier. Such representation still retains the

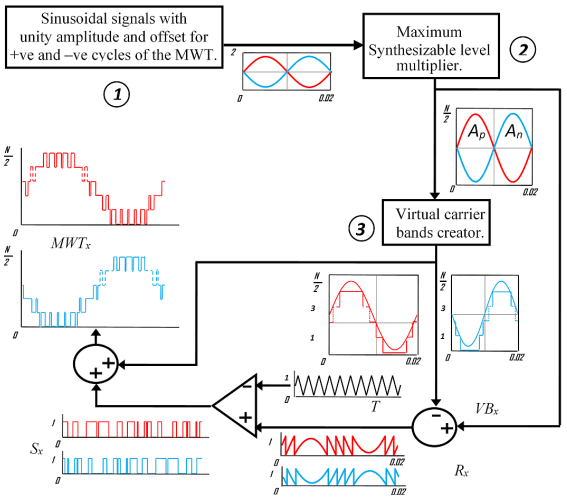

FIGURE 2. Per phase block diagram of the multilevel waveform template, MWT, generation.

contiguous bands occupied by these multi triangular carriers in the traditional level-shifted SPWM; since these bands are among the crucial prerequisites for proper stacking of the synthesized waveforms from each of the series H-bridges. Conceptually then, this modulation approach is based on the creation of multilevel waveform template, MWT, from which the power switches in all the H-bridge units are controlled. More interesting is that the CHB inverter system can attain equal power balancing among the constituting units irrespective of the fact that the MWT deployed has its formation from phase-disposition level-shifted SPWM concept. It is worthy acknowledging that the modeling of this MWT for any desired number of output voltage level simply involves already known facts about CHB MLI configuration, as documented in the literature. Hence in the subsections that follow, explanations on the MWT creation, for phase *a,* are given following the block diagram shown in figure 2.

A. REFERENCE SIGNAL GENERATION

Sinusoidal signals are among the base waveforms needed for the creation of the MWT. In figure 2, these waveforms are realized in the blocks labeled 1 and 2. Block 1 generates unity–offset sine waveforms that are 180 out of phase with each other. The unity offset is needful in view of the modulation algorithm that will be presented in later sections of this paper. The generalized expression for the maximum number of phase–leg voltage levels, N, synthesizable in a MLI configuration was given in [35]; this was demonstrated therein and in [36]. This expression is restated herein in (2),

$$N = \sum_{j=1}^{k} V_j \left(m_j - 1\right). \tag{2}$$

V_j and m_j are the per unitized voltage step and number of output voltage levels synthesized by the *jth* cascaded unit, per half-cycle, respectively. In Fig. 1, it can be observed that all H-bridges synthesize waveforms with the same voltage

step (voltage amplitude between two adjacent levels), that is (symmetrically connected; this implies that $V_1 = V_2 = \cdots V_k = 1$. And also that the number of output voltage levels synthesized in each H-bridge units per half cycle is same, that is, $m_1 = m_2 = \cdots m_k = 2$. Then for symmetrical CHB MLI in Fig. 1, (2) becomes

$$N = \sum (\text{number of CHB units}) . \tag{3}$$

Hence, in block 2, (3) is implemented; therein, the unity offset sine waves from block 1 is multiplied by a factor, resulting in the expression given in (4),

$$\begin{aligned} A_p &= \{1 + msin\,(2\pi ft)\}\left(\frac{N}{2}\right) \\ A_n &= \{1 - msin\,(2\pi ft)\}\left(\frac{N}{2}\right). \end{aligned} \tag{4}$$

where m is the modulation index and f is the frequency of the MWT for the positive and negative half-cycles, A_p and A_n, respectively. It can be observed that in [34], N was defined as the number of sub-modules in each of the two arms in a phase–leg of modular multilevel converter, MMC; and therein, no clue was given for the determination of the actual value of N.

B. VIRTUAL CARRIER BANDS CREATION

The concept of single triangular carrier signal in the deployment of SPWM for the control of multilevel inverters involves the creation of virtual carrier bands that mimic the contiguous bands occupied by real triangular carriers in the well-known level-shifted SPWM scheme. Understanding of the virtual carrier band creation concept can be facilitated by exploiting the idea of comparing reference sine waveform with constant levels in the works presented in [35], [36]. Though hybrid and unsymmetrical cascaded units were considered in these works, it is worthy to note that the concepts shown therein are universal; it is just a matter of adapting the analytical variables to the multilevel inverter topology under consideration. These analytically determined sequential constant levels of comparisons form the virtual carrier bands in this proposed modulation scheme for CHB MLI as typified in Fig. 3(b). Sequence of computing the values of these constant levels of comparisons for a given number of cascaded units is typified in Fig. 3. For CHB MLI shown in Fig. 1, the per phase reference signals of the system are given in (4). These signals are compared to a given number of constant levels; the *ith* comparison level of the *kth* cell, C_k, can be given as

$$C_k = \sum_{j=1}^{k-1} \left(m_j - 1\right) V_j + (i-1)\, V_k. \qquad j = 1, 2, \ldots m_k - 1 \tag{5}$$

But all H-bridges generate 2-level voltage waveforms per half-cycle; hence, $m_j = m_k = 2$. This implies that i can only be of value 1. This simplifies (5) to

$$C_k = \sum_{j=1}^{k-1} V_j. \tag{6}$$

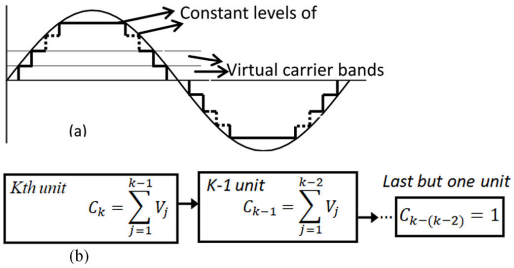

FIGURE 3. a) Virtual carrier band creation, (b) Sequence of computing the values of constant levels of comparisons.

As noted earlier, all the H-bridge units synthesize output waveforms with the same voltage step, that is, they are symmetrically connected in Fig. 1, therefore $V_j = 1$ for all j values in (6). Clarification of the expression in (6) can be done by taking only three H-bridges, per phase in Fig 1, for exemplary purpose. From Fig. 3, it can be seen that the first and only constant level of comparisons of the third and second H-bridge units are 2 and 1, respectively.

Instead of having individualized step modulation within the virtual bands formed by these constant levels as is the case in [35], [36], the floor function can be used directly on A_p and A_n, as given in (7),

$$VB_x = floor\,(A_x) \tag{7}$$

The subscript x assumes p and n for the positive and negative half-cycle notations, respectively.

This is exactly the intuitive result obtained in [34]. The two resulting stepped waveforms, VB_p and VB_n, provide information on the virtual carrier bands in terms of numerical numbers of 1, 2, 3…

Onwards, the remaining steps in the MWT creation involve simple mathematical summation and subtraction; as well as logical comparison. The output waveforms of block 3 can be viewed as temporary stacked fundamental frequency control outputs of all the series H-bridges except the last, in either half-cycles of the MWT. They can as well be seen as sequential stack of the virtual carrier bands void of real triangular signals. With such view then, the last unit cell will be pulse width modulated; its modulating signals (R_x), in either half-cycle, are sourced from the overall modulating signals of the system (outputs of block 2) less the stepped waveforms outputs of block 3. This is depicted in figure 2, where a summer is used with plus and minus input terminals. If the modulation index (m) is 1, then amplitudes of the resulting waveforms are each 1 because from (3), (4) and (6), the amplitude of A_p or A_n is 1 greater than the highest computed value of constant level of comparison in the *kth* cell.

$$R_x = A_x - VB_x \tag{8}$$

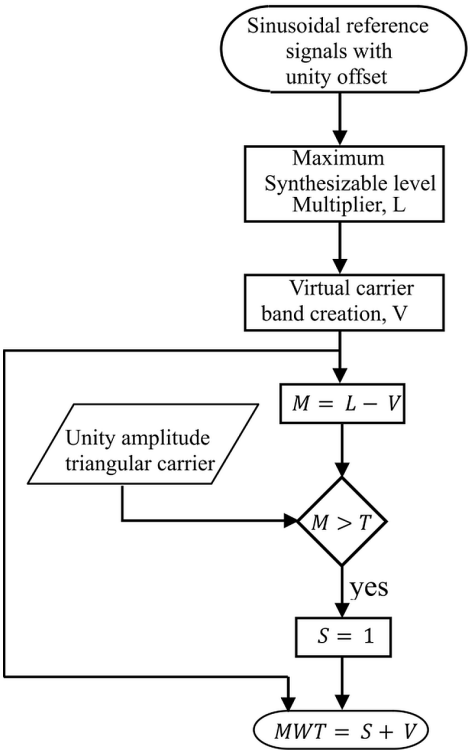

FIGURE 4. Flowchart for modulation waveform template generation.

R_x is compared with a unity-amplitude single triangular carrier wave, T, to generate train of pulses, S_x, of unity magnitude.

$$S_x = R_x > T \tag{9}$$

Note that in figure 1, the H-bridges share the same operational characteristics and are symmetrically connected. Therefore, the need to have varying modulation schemes for the cascaded units, as was obtainable in [35], [36], does not arise. It then implies that in each of the virtual carrier band, generation of such virtual train of pulses in needful. This is realized by adding to each of the stepped waveforms, VB_x, from block 3 the *PWM* signals S_x, in a second summer in figure 2. The resulting signals are the multilevel waveform templates for the CHB system, MWT_x, and this mimics the phase-disposition *PWM* scheme.

$$MWT_x = VB_x + S_x \tag{10}$$

The aforementioned detailed modulation waveform template generation is depicted in a flowchart of figure 4.

Performance of three-phase *SPWM* regarding the optimal usage of the dc-link voltage can be improved either by injection of the third-harmonic component or addition of the min-max function to the base sinusoidal reference waveforms. In either approach, addition of the zero-sequence component is achieved. This has the effect of flattening the peaks of the *3-leg* reference modulating waveforms and hence extends the linear modulation range; wherein increase in the synthesized inverter fundamental output voltage is achieved. The modified phase-leg reference signal expressions after the injection

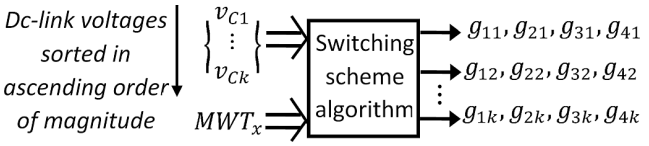

FIGURE 5. Per phase switching signal generator.

of the zero-sequence component, in accordance with the min–max function principle, [37], [38], are given in (11),

$$\begin{aligned} v_a &= msin\,(\omega t) - 0.5(v_{max} + v_{min}) \\ v_b &= msin\left(\omega t - \frac{2\pi}{3}\right) - 0.5(v_{max} + v_{min}) \\ v_c &= msin\left(\omega t - \frac{4\pi}{3}\right) - 0.5\,(v_{max} + v_{min})\,. \end{aligned} \tag{11}$$

where v_{max} and v_{min} are the instantaneous maximum and minimum values of v_a, v_b, v_c; which are the base processing signal inputs to block 1 in figure 2. In the following subsection, MWT_x is passed to the system switching signal generator; wherein sorted input dc- link capacitor voltages and MWT_x are sequentially compared to generate the switching signals for the power switches in each of the series H-bridges.

C. SWITCHING SIGNAL GENERATOR

The last step in the proposed single carrier *SPWM* scheme involves a simple comparison algorithm in a switching signal generator shown in figure 5.

In figure 1, the sources to the capacitor banks are provided by multi-winding transformer secondary via full bridge rectifiers in each of the phases; as is usually the case in most of the applications. Ideally, all the dc-link voltages of the H-bridge units should be equal, that is V_{dc}; but cognizance of the ripple variations in these capacitor voltages necessitates their being sorted before being used in the proposed modulation algorithm. In each phase, all the capacitor voltage values are sensed and arranged serially in a column matrix, with unit 1 dc-link voltage value being the first element in this array. The sorting process provides the index numbers occupied by these sensed dc-link voltages in this column matrix. These index numbers match in values with the earlier computed constant levels of comparisons in the formation of the virtual carrier bands in subsection 3.2; which are also the step values in the MWT_x waveform in figure 2. It should be noted that the whole steps taken in figure 2 to generate MWT_x are clearly a demonstration of the extension of the well-known bipolar *PWM* to multi-cascaded H-bridge units. Based on this very fact, the upper positive ($\mathrm{g}_{11}, \mathrm{g}_{12} \ldots \mathrm{g}_{1k}$) and negative ($\mathrm{g}_{31}, \mathrm{g}_{32} \ldots \mathrm{g}_{3k}$) switching functions are generated by comparing the positive and negative multilevel waveform templates, MWT_p and MWT_n, respectively, with the sorted dc-link voltages.

As commented in the last paragraph of the introductory section, even distribution of the generated switching signals among the constituting power switches is achieved by using reverse-sorted-voltage approach in the comparison algorithm. This approach mimics the operational feature of the conventional phase-shifted SPWM. This actually means that the

order of the elements (index numbers of the sorted dc-link voltages) in the input column matrix in figure 5 is reversed while executing the comparison algorithms in the positive and negative half-cycles.

IV. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

MATLAB/SIMULINK simulation models of the power and logic circuits of figure 1 were developed using the proposed modulation outlines in figures 2 and 5, as discussed in section 3. Arbitrary 7-level CHB configuration is considered for the simulation study. The three isolated dc-link voltages per phase are sourced from capacitor banks (capacitance value of 2200μF each) fed from the outputs of rectifier bridges. In each phase, the inputs to these bridges are the secondary voltages of a 3-winding transformer whose respective input terminals are connected to the utility power supply. Each dc-link voltage value is 100 V. An *RL* load (*R* and *L* are 25 Ω and 20 *mH*, respectively) is connected in each phase of the inverter whose depth of modulation is 0.95 at carrier frequency of 5 *kHz*. The proposed SPWM approach was applied on a 7-level, three- phase CHB configuration and the resulting simulated inverter output waveforms are shown in figure 6.

In figure 6(a), it can be seen that constant evenly distributed output voltage pulses were achieved in the 3 cascaded H- bridge units in phase a. The generated 7-level phase-leg and 13-level line voltage waveforms are shown in figure 6(b) and (c). Displayed in figure 6(d) are the corresponding line current waveforms from the simulation model. In Fig. figure 7(a), the dynamic variations of the three dc-link voltages in each of the phases are shown alongside with the aggregate plot of all dc-link voltages. These waveforms depict that balancing of the capacitor bank voltages is achieved in the proposed switching scheme algorithm in figure 5. The FFT analytical spectra of the inverter output voltage waveforms are shown is figure 7 (b). Therein, total harmonic distortion (THD) values of 20.5937% and 16.710% were obtained for the phase-leg and line voltage waveforms, respectively. In these analyses, harmonics up to the 300th harmonic order (15 kHz) were used in the THD computations.

For comparison purpose, corresponding simulated waveforms were generated using the conventional in-phase level-shifted and phase-shifted SPWM schemes. The obvious simulated results show that the synthesized phase- leg voltage waveform performances of the three considered SPWM schemes are relatively at par as shown in figure 7(b). However, the FFT analyses of the respective line voltage waveforms show THD values of 11.5534%,16.71% and 17.0106% for IPD, proposed and PS SPWM schemes, respectively. In each inverter phase, there are glaring differences in the waveform patterns of the individual H-bridge output voltages. With the two conventional SPWM schemes (IPD and PS), the individual H-bridge unit's output voltage formations are obvious and well-documented in the literature. But with the

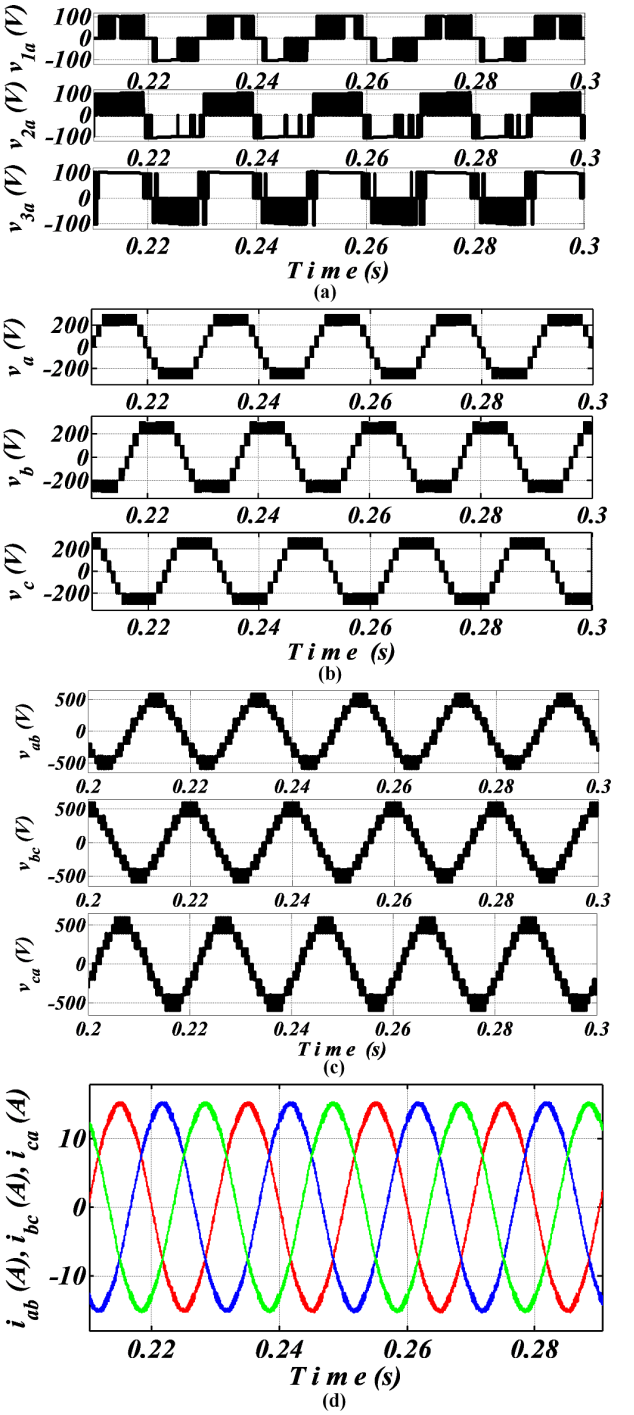

FIGURE 6. Simulated output voltage and current waveforms of the 7-level CHB MLI with the proposed PWM scheme. (a) Phase a individual H-bridge output voltages, (b) Phase-leg voltages, (c) Line voltages, (d) Line currents.

proposed PWM technique, it can be seen from figure 6(a) that the individual unit's output voltage pattern is actually hybridized. Non-regular evenly distributed output voltage pulses were generated in each of the three cascaded units. The resultant real output power waveforms generated in each of the 3 H-bridge units in all the phases are shown in figure 7(d). In comparison, application of IPD and PS SPWM schemes in the 7-level CHB MLI resulted in unequal and relatively

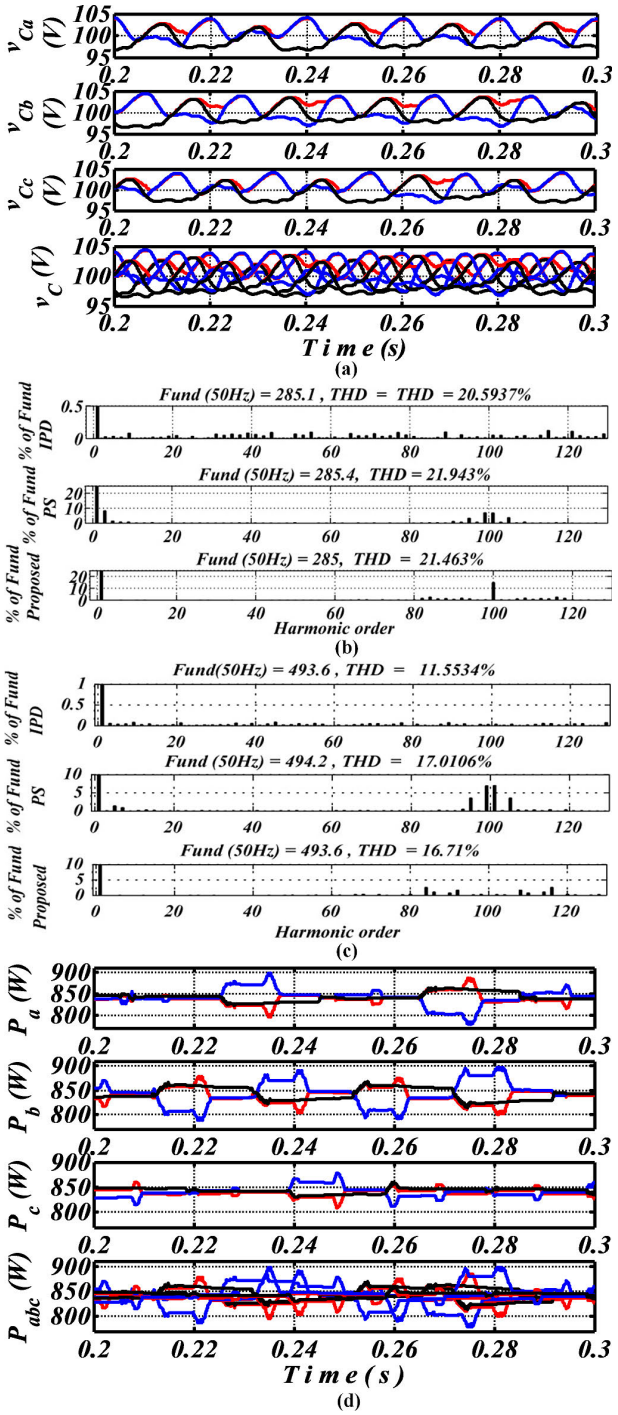

FIGURE 7. Simulated dc-link voltages, FFT analyses of the phase-leg and line voltage waveforms and Real output power waveforms. (a) Dc-link voltages for the whole phases, (b) FFT analysis of the phase-leg voltage waveform from IPD, PS and proposed modulation schemes, (c) FFT analysis of the line voltage waveform from IPD, PS and proposed modulation schemes, (d) Real output power waveforms of the individual H-bridges with the proposed SPWM scheme.

equal power sharing of the overall output power, respectively, among the 3 cascaded units; theses innate exhibitions are obvious and well documented in the literature, [27]. Similar to PS PWM output power performance, the proposed modulation scheme achieves relatively equal real power outputs

TABLE 2. Prototype specification.

Component	Specification
Power switches	MMG75S120B6C
Fundamental frequency	50 Hz
Carrier frequency	5 kHz
Capacitor bank	2200μF, 200 V
RL load	25 Ω and 20 mH
Each dc-link voltage	100 V
Output power	3.9KW

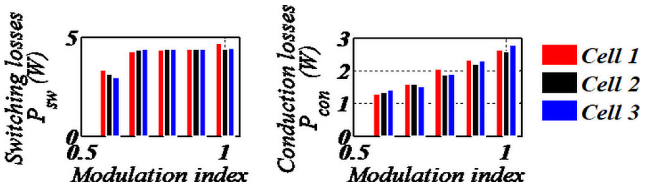

FIGURE 8. Inverter conduction and switching losses for modulation index range of 0.6 to 1.

FIGURE 9. Laboratory prototype stand for the 7-level CHB MLI.

in the 3 cascaded units in the three phases. In Table 1, the proposed modulation approach was compared with PS SPWM for the indicated parameters.

The power loss computations of the switching devices have been carried out using PSIM simulation package. PSIM thermal modules were used; all module parameters have been extracted from the corresponding datasheet provided for MMG75S120B6C power switch module. The system parameters listed in Table 2 are used in the PSIM simulation model of the inverter. In each switch module, the conduction losses in the IGBT and its anti-parallel diode are summed up to give the conduction loss for the switch module. The same computation and module loss assignment is done for the switching losses that are composed of turn-on and turn-off switching losses. The switching losses in the switch modules are computed based on their turn-on and turn-off switching losses and the turn-on energy loss equations given in (12)

$$P_{sw} = P_{sw-on} + P_{sw-off} = \left\{ \begin{array}{l} (E_{on} + E_{off}) * f * \\ * \left(V_{cc}/V_{cc,datasheet}\right) \end{array} \right\} \tag{12a}$$

$$E_{on}, E_{off} = \int V_{CE}(t) * i_C(t)\, dt \tag{12b}$$

where E_{on}/ E_{off} is the switch turn-on/ turn-off energy loss, V_{cc} is the actual dc bus voltage, and $V_{cc\_datasheet}$ is the dc bus voltage in the E_{on}/ E_{off} characteristics of the datasheet,

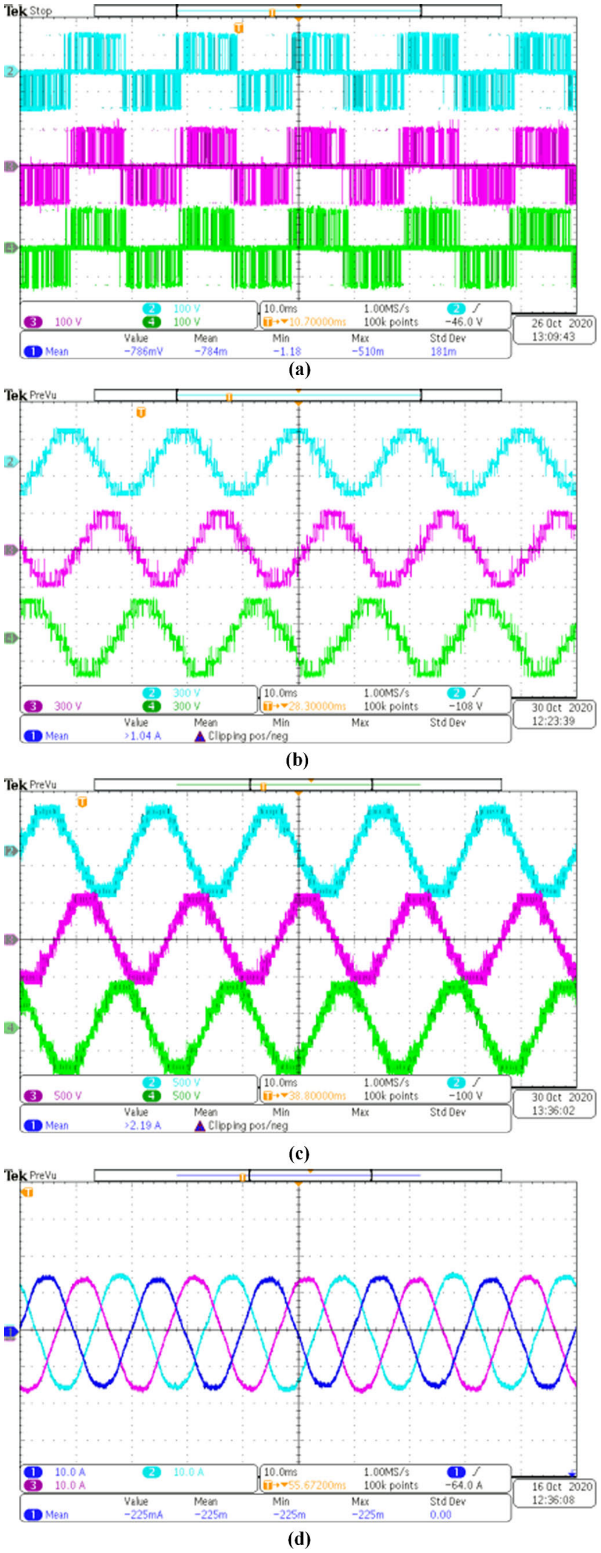

FIGURE 10. Experimental output voltages and currents. (a) Each H-bridge's output voltage in phase 'a', (b) Phase-leg output voltages in all the phases, (c) Output line voltages, (d) Output line currents.

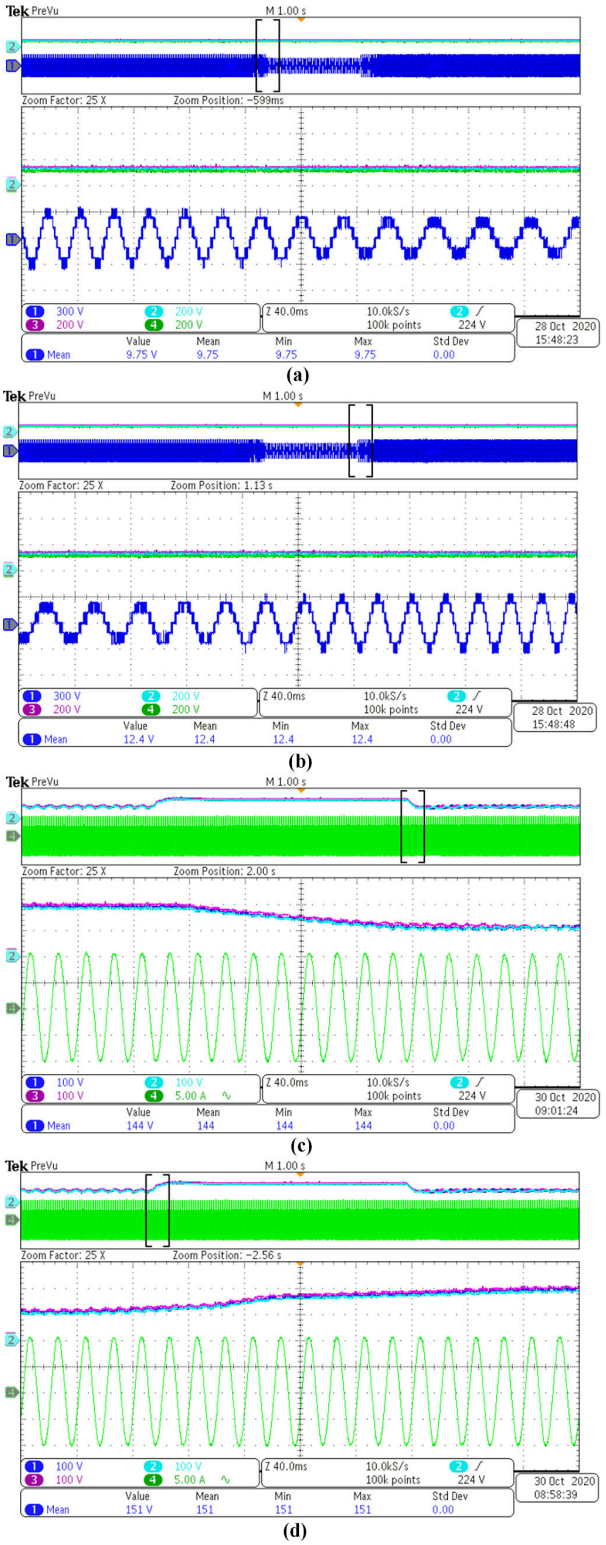

FIGURE 11. Experimental dynamic responses of the inverter system: (a), (b) Change in the modulation index value at constant input dc-link voltages; (c), (d) Change in the input dc-link voltages at constant output load current.

defined as 'dc bus voltage' in the test conditions, V_{CE} is the collector-Emitter voltage, and i_C is the collector current.

With the proposed modulation scheme, the computed losses for modulation indices of 0.6 to 1 are shown in figure 8.

B. EXPERIMENTAL RESULTS

The experimental prototype stand of the 7-level CHB with the load is shown in figure 9. Digital signal processing driver

board with a Sharc ADSP21363L floating-point signal processor and Altera Cyclone II FPGA were used to generate the PWM signals and to implement the H-bridges' dc-link balancing scheme. Table 2 gives the prototype specifications and parameters. The three isolated dc-link voltages per phase were sourced from capacitor banks fed from the outputs of rectifier bridges. These bridges were supplied by the three-phase ac power supply through a 3-winding transformer. Each dc-link voltage value is approximately 100 V. The modulation index was set to 0.95. figure 10 shows the measured experimental waveforms of the inverter output voltages and the corresponding load currents.

Comparatively, the experimental output voltage of each H-bridge in phase 'a' and their cascaded output depict 3- and 7-level waveforms as earlier simulated and displayed in figures 7 (a) and (b), respectively. Moreover, the obtained experimental line voltages are in conformity with the simulated output line voltages in figure 7(c). Both depict 13-level output waveforms. The simulated and experimental line current waveforms are in good agreement.

The dynamic behaviors of the inverter system were examined by changing the modulation index value from 0.95 to 0.5 and back to 1 again. The dc-link voltages were effectively balanced during these dynamic operations; each maintaining an approximate value of 100 V. Also, the dc-link voltages were varied from 200 V to 100 V and back to 200 V. The resulting output currents maintained constant peak value and their sinusoidal waveform. Figure 11 displays, for phase 'a', the experimental dynamic responses of the inverter system for these variations.

V. CONCLUSION

Presented in this paper is a hybridized single carrier-based pulse width modulation scheme for cascaded H-bridge multilevel inverter. Its operational concept wherein a sinusoidal modulating waveform is modified to fit in a single triangular carrier signal range in order to generate the desired output waveform template for the MLI has been explained in detail. The principle of generating the modulating templates is a furtherance of earlier established modulation approaches for multilevel inverters. It has been shown that the generation of the modulating templates is a clear demonstration of the extension of the well-known bipolar PWM to multi-cascaded H-bridge units. Once the templates are generated, it can be used on CHB inverter of any level with no further control modification; only the parameter N need to be specified. From industrial point of view, the presented concept of MWT will find its application in large number of cascaded H-bridge systems because with the proposed modulation, the inverter control system becomes insensitive to the traditional concept of multiplicity of carrier waves as the number of inverter level increases. This will be highly advantageous since the extra control effort of carrier synchronization will be by-passed in the control algorithm. The proposed SPWM ensures nearly even distribution of switching pulses among the constituting power switches using a reverse-voltage-sorting comparison algorithm. Consequently, the real power variations in the entire cascaded H-bridges are kept within a very narrow band. From our findings, the proposed control approach results in a hybrid modulation scheme that mediates between the phase- and level-shifted carrier-based SPWM techniques; thereby inheriting the good features in these two modulation schemes.

The performance of the proposed SPWM scheme has been presented through scaled down simulations and experiments on a 3-phase, 7-level CHB inverter; results have been adequately presented.

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