

A Five-Leg Three-Level Dual-Output Inverter

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Abstract— Classical 3-level dual-output inverter, 3-L DOI, involves two similar 3-level inverters that provides a pair of 3-phase output voltages with same or different frequencies from common input voltage source. Flexibility of either operation of the constituting inverters is evident in this DOI; but total duplication of power switches is a major drawback. State of the art coupled 3-L DOIs reduce this drawback by providing series-shared power devices between the two different 3-phase output terminals. Compared with the classical 3-L DOI, these newly developed coupled 3-L DOIs involves a smaller number of power switches; however, independent operation of the constituting inverters is lost. In this work, a 3-L DOI is proposed which involves lesser number of power devices and provides flexibility of either operation of the constituting inverters. The 3-L DOI feature hinges on the concept of parallel-common-inverter-leg representation. At the same or varying frequency mode operation, the proposed inverter can synthesize two 3-phase output voltages. Range and relation between the two modes of operations are defined for the DOI. The control strategy is based on the single triangular carrier sinusoidal pulse-width modulation perspective. Experimental results are presented that depict the DOI inverter performances.¹

Index Terms—Multilevel inverter, sinusoidal pulse-width modulation, F-type inverter, total harmonic distortion.

I. INTRODUCTION

Generally, classical dual-output inverters, DOI, constitute of two inverters (of the same configuration) that provides a pair of 3-phase output voltages to two independent 3-phase load from a common input voltage source. These sets of output voltage waveforms can be of the same or different amplitudes and frequencies. This class of DOI involves a duplication of the base inverter topologies and controls; resulting in much demand of significant number of power devices, [1]–[4]. The quest for optimal usage of power switches in DOIs gave rise to compact DOIs; wherein the supposed two power circuits are coupled together to share some of the constituting power switches. Three known conceptual approaches have been used in configuring these coupled power circuits, namely: split-capacitor-bank, [5], common-series-switch, [6]–[13] and common-parallel-phase approaches, [14].

Considering 2-level output voltage operation, these power circuits have been explored in series of applications. The split-capacitor-bank- and common-parallel-phase-based DOI were deployed in 3-phase drive systems, [1] and [10]. Also, expansive deployment of DOI with common-series-switch concept can be seen in these applications: power conditioner, [4]; distributed energy generation, [5]; matrix converter, [6]; DFIG, [7]; UPS, [8]; drive systems, [9].

For 3-level multilevel inverter system, the common-series-switch approach is predominant; it has been used in the configuration of recently proposed 3-level, compact DOIs, [15]–[17]. These DOI power circuits are derivatives of active-neutral-point converter topology, ANPC. In [15], two individualized phase voltage-clamping active switches were used in conjunction with the series-shared switches. Undue limitation in this power circuit switching states operation is evident; resulting in its loose grip on the input capacitor banks' voltage balancing. [16] proffered a solution to this drawback in [15] by deploying a mixture of active and passive switches in the voltage-clamping stages. This configuration involves a total of 20 active switches and 12 diodes as depicted in Fig. 1 (a). Besides, due to its concept of operation, the maximum modulation index of each inverter is clamped to 0.5; and obviously, its control/modulation scheme involves complex procedures. Based on the T-type topological concept, very compact DOI was presented in [17]. Therein, all shared power switches were per phase individualized, as shown in Fig. 1(b). Typical to T-type inverter configuration, the three outer switches that connect each phase directly to the positive dc rail have voltage stress of the input dc voltage value. The same voltage stress value has to be blocked by the corresponding three outer switches that connect each phase directly to the negative dc bus.

In the aforementioned compact 3-level DOIs ([15]–[17]), it is glaring that in each inverter-leg, the two output terminals are linked in series, with respect to the positive and negative terminals of the input dc source. Consequently, if any of the outermost switches in each inverter-leg is open, the corresponding outputs are lost. Also, in typical application scenario where either generation of 3-phase waveforms is needed, all the switches in each of the inverter-legs will still be involved. In view of these, this letter proposes a 5-leg, 3-level DOI based on the common-parallel-phase approach. Its base conceptual power circuit is derived from the F-type inverter, [18]. In the following sections, the organization of this letter follows as: configuration and operational principle of the power circuit are presented in section II; the control/modulation scheme based on carrier-based SPWM is given in section III; in section IV, experimental results are presented.

II. PROPOSED THREE-LEVEL DUAL-OUTPUT INVERTER CONFIGURATION.

The proposed 5-leg, 3-level DOI is shown in Fig. 2. The input terminals P , n and N correspond to the positive, mid-point (neutral-point) and negative input dc, V_{dc} , rails. With two-

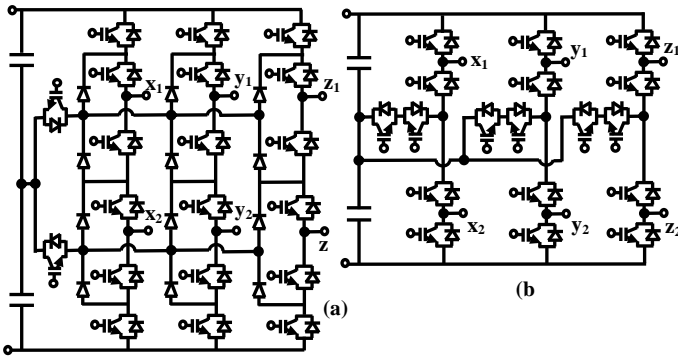


Fig. 1. Common-series-switch-based DOI (a). DOI in [16]; (b) DOI in [17].

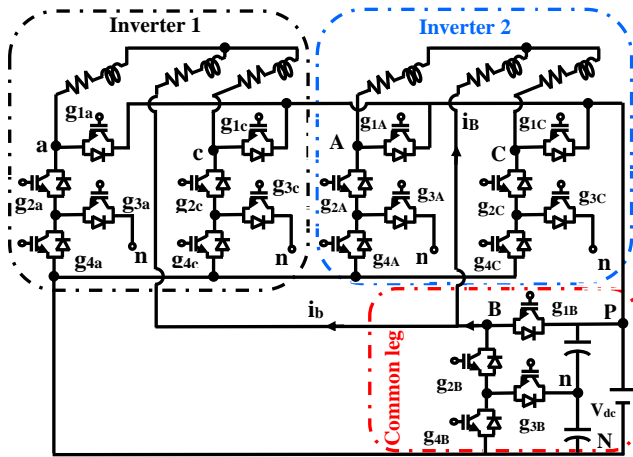


Fig. 2. Proposed 5-leg, 3-level dual-output inverter

switch combinational operation, each of the 5 inverter legs outputs 3 voltage values with reference to node n . $v_n = 0.5V_{dc}$ if g_{1x} and g_{3x} are switched ON; $v_n = 0$ when g_{2x} and g_{3x} are on the ON-state; $v_n = -0.5V_{dc}$ if g_{2x} and g_{4x} are switched ON; where $x = A, B, C, a, c$. These inverter-leg voltage syntheses are summarized in Table 1.

TABLE I

SWITCHING STATE AND OUTPUT VOLTAGE GENERATION

| g_{1x} | g_{2x} | g_{3x} | g_{4x} | Output voltage |
|----------|----------|----------|----------|----------------|
| ON | OFF | ON | OFF | $0.5V_{dc}$ |
| OFF | ON | ON | OFF | 0 |
| OFF | ON | OFF | ON | $-0.5V_{dc}$ |

The DOI power circuit in Fig. 2 consists of two F-type-based, 3-phase inverters that are classically fed from common input dc bus rails. Output node B of the common inverter-leg feeds corresponding middle-phase loads in the 2 inverters. Consequently, in both inverters, the middle phase is virtually represented. Two modes of operation are possible in the proposed DOI: common and different mode of operations; where the magnitudes and frequencies of the two 3-phase output voltage waveforms can be the same or different in the 2 inverters. The syntheses of these 2 output voltage waveforms in either of these modes of operation is better explained with the control scheme presented in the following section.

III. PROPOSED SPWM SCHEME FOR THE 3-LEVEL DUAL-OUTPUT INVERTER.

If two 3-phase, 3-level inverters are classically connected to

deliver independent pair of 3-phase output voltages, corresponding pair of 3-phase voltage reference signals are needed. In Fig. 2, one inverter-leg is common to both inverters. Hence, the supposed voltage references are modified to fit appropriately in the control of this power circuit by alternate addition of the middle-phase references to each set of 3-phase voltage reference signals as given in (1) and (2).

$$v_a = m_1 \sin(\omega_1 t) + m_2 \sin(\omega_2 t - 2\pi/3 - \theta) \quad (1a)$$

$$v_b = m_1 \sin(\omega_1 t - 2\pi/3) + m_2 \sin(\omega_2 t - 2\pi/3 - \theta) \quad (1b)$$

$$v_c = m_1 \sin(\omega_1 t + 2\pi/3) + m_2 \sin(\omega_2 t - 2\pi/3 - \theta) \quad (1c)$$

$$v_A = m_2 \sin(\omega_2 t - \theta) + m_1 \sin(\omega_1 t - 2\pi/3) \quad (2a)$$

$$v_B = m_2 \sin(\omega_2 t - 2\pi/3 - \theta) + m_1 \sin(\omega_1 t - 2\pi/3) \quad (2b)$$

$$v_C = m_2 \sin(\omega_2 t + 2\pi/3 - \theta) + m_1 \sin(\omega_1 t - 2\pi/3) \quad (2c)$$

where ω , m and θ are the frequency, modulation index and phase shift between the two inverters; subscripts 1 and 2 denote inverters 1 and 2 parameters, respectively. In the derived sets of reference waveforms, v_b and v_B are equal in all respect; thus, either of these serves correctly as the reference signal of the common inverter-leg.

Arbitrarily considering line voltages v_{BC} and v_{bc} referenced to phase voltages v_b and v_B , the line-to-phase voltage relationships are given in (3).

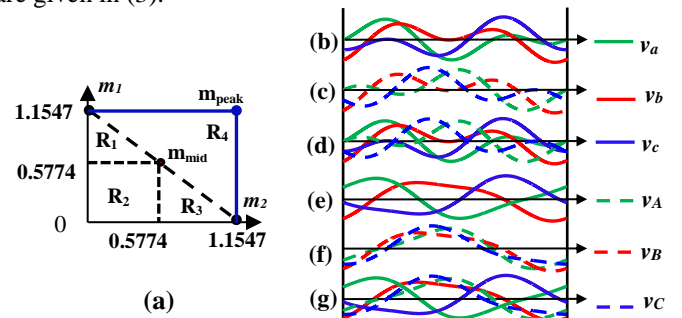


Fig. 3. Operational boundary definition and typical reference voltage waveforms for DOI. (a) Boundary definition; (b), (c) and (d) $m_1 > m_2$ and $\omega_2 = 2\omega_1$; (e), (f) and (g) $m_1 = m_2$ and $\omega_2 = 3\omega_1$.

$$/v_{BC}/ = \sqrt{3}/v_B/ \quad (3a)$$

$$/v_{bc}/ = \sqrt{3}/v_b/\sqrt{3} \quad (3b)$$

The sum of these line voltages is the DOI system's output voltage magnitude, v_s ; given in (4) in terms of the shared node voltage, v_B , in Fig. 2.

$$/v_s/ = /v_{BC}/ + /v_{bc}/ = \sqrt{3}/v_B/ + \sqrt{3}/v_b/ = 2\sqrt{3}v_B \quad (4)$$

Note that v_b and v_B are equal, as could be seen in (1b) and (2b). By definition, either of the inverter's modulation index, m_s , is defined as the ratio of the phase voltage fundamental peak value, v_B , and one-half of the dc bus voltage, V_{dc} ; that is

$$m_s = \frac{v_B}{0.5V_{dc}} \quad (5)$$

For different frequency mode operation in both inverters, maximum utilization of the input dc voltage is reached when the peak value of the system's voltage magnitude, v_s , becomes equal to the input dc voltage V_{dc} ; a condition that sets the limit of the linear modulation region. Thus,

$$/v_s/ = 2\sqrt{3}v_B = V_{dc} \quad (6)$$

When v_{dc} is substituted in (5) from (6), the modulation index, m_s , is given as

$$m_s = 0.57735 \quad (7)$$

This is the maximum equal modulation index for the two inverters in this different frequency mode operation. If m_1 and m_2 are the modulation indices for the inverters 1 and 2; and noting that maximum modulation index is 1.1547 for a 3-phase system, [19], then

$$m_1 + m_2 \leq 1.1547 \quad (8)$$

With (8), the variation of the modulation indices in the 3-L DOI is shown in Fig. 3(a). Therein, four operational regions R_1 , R_2 , R_3 and R_4 are depicted. In region R_1 , m_1 and m_2 can be varied between 0.5774 and 1.1547 for m_1 and correspondingly 0.5774 and 0 for m_2 . Hence, inverter 1 can generate 5-level line voltage waveforms; while generation of 3-level line voltages are possible from inverter 2. The reverse is the case in region R_3 . In region R_2 , the range of m_1 and m_2 are both 0.5774. Here, both inverters can only deliver 3-level line voltages to the respective dual loads. In region R_4 , only common frequency mode operation of the inverters is possible; wherein, the operational point m_{peak} can be reached with both inverters having maximum modulation index of 1.1547 each.

With (1) and (2), typical reference inverter-leg voltage waveforms are shown in Figs. 3(b) to (h) for regions R_1 and R_2 operations. v_a, v_c, v_A, v_C and v_b are the needed voltage references for the corresponding inverter-legs in Fig.2. Figs. 3(b), (c) and (d) correspond to the same operational point; the obtained references, from (1) and (2), for inverters 1 and 2 are shown in Figs. 3(b) and (c), respectively. The needed reference signal for the common inverter-leg and two pairs of reference signals for inverters 1 and 2 are combined in Fig 3(d) to obtain five modulating signals for the 5 inverter legs. Similar displays are shown in Figs. 3(e) to (g) with different parameter values. From this juncture onwards, the SPWM control concept, [20], presented for the F-type inverter in [18] is used individually to generate the gating pulses for the power switches in the proposed DOI power circuit. A recap of this modulation scheme is presented as follows.

For a period of the higher-frequency operated inverter, the 5 references, v_a, v_c, v_A, v_C and v_b , are sequentially sampled to determine the most positive (*max*) and most negative (*min*) reference waveform. Each inverter-leg's modulating waveform, v_x ($x=a, c, A, B, C$) is further split to obtain two modulating waveforms ($mod_{x,+}$ and $mod_{x,-}$) that are used to generate the positive and negative half-cycles of the respective inverter-leg output voltage. These waveforms are obtained by subtracting the *max* and *min* values from the respective voltage reference, v_x ; and adding unbalance compensation offset signals as given in (9).

$$mod_{x,+} = \begin{cases} 0.5 * (v_x - min) \\ -v_{com}(i_x - i_+) \end{cases} \quad (9a)$$

$$mod_{x,-} = \begin{cases} 0.5 * (v_x - max) \\ +v_{com}(i_x - i_-) \end{cases} \quad (9b)$$

$$v_{com} = (v_{c,low} - v_{c,up})k_{com} \quad (9c)$$

$v_{c,low}$ and $v_{c,up}$ are the lower and upper capacitor bank voltages in Fig. 2; k_{com} is a proportional gain; i_x is the respective phase current; i_+ and i_- are the currents of the particular phases for which their voltage reference signals attain their minimum and maximum values, respectively in Fig. 3(d) or (g). A flowchart

that shows the needed steps for generating the control pulses of the inverter power switches is shown in Fig. 4.

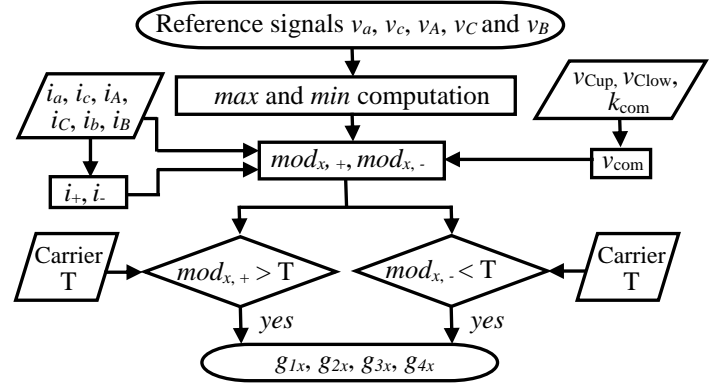


Fig.4. Flowchart of the modulating scheme.

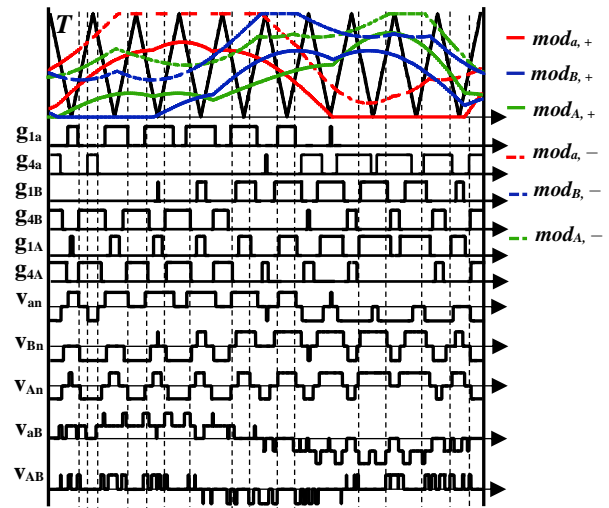


Fig.5. Typical deployed modulation scheme for the syntheses of dual output line voltages, v_{aB} and v_{AB} , in the DOI.

In Fig. 5, the modulation signals of inverter-legs 'a' and 'A' of inverters 1 and 2, along with that of the common inverter-leg 'B' are typified for different frequency operational mode. In this figure, the presented modulation scheme is demonstrated whereby the switching signals are obtained by comparing the respective obtained modulating waveforms with the single triangular carrier signal, T , in simple logic operations as

$$g_{1x} = mod_{x,+} > T \quad (10a)$$

$$g_{2x} = !g_{1x} \quad (10b)$$

$$g_{4x} = mod_{x,-} < T \quad (10c)$$

$$g_{3x} = !g_{4x} \quad (10d)$$

IV. EXPERIMENTAL RESULTS.

A laboratory prototype of the DOI was built; a photo of this is shown in Fig. 6(a). On-board ADSP21363L DSP processor and Altera Cyclone II FPGA were used to implement the SPWM control scheme. Table II gives the prototype parameters and specifications. In the following displayed experimental results, two phase quantities were shown because the oscilloscope we used has 4-channels. Shown in Fig. 6(b) and (c) are the experimental output line voltage and current waveforms of the DOI with frequencies of 50 and 100 Hz; and modulation indices of 0.3024 and 0.8523 swapped between the inverters. Therein,

TABLE II
PROTOTYPE SPECIFICATION

| Component | Specification |
|----------------------------|---------------------|
| Power switches | NGTB25N120F |
| Fundamental frequency, f | 50 and 100 Hz |
| Carrier frequency | 3.350 kHz |
| Capacitor bank | 1000 μ F, 600 V |
| RL load | 20 Ω , 20 mH |
| Dc-link voltage | 400 V |

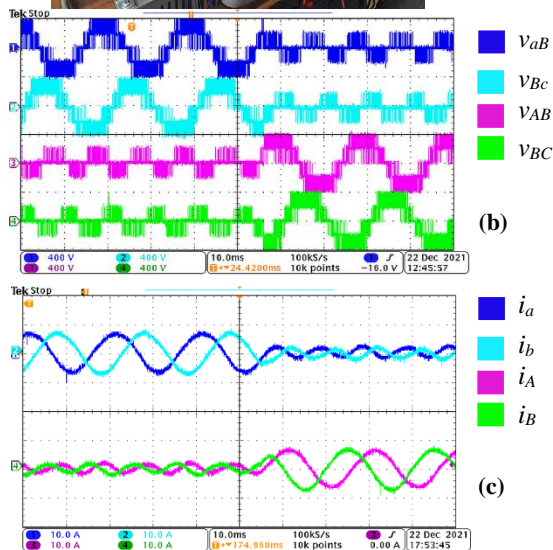


Fig. 6. Prototype, output line voltages and currents of the DOI at 50 and 100 Hz; and modulation indices of 0.3024 and 0.8523. (a) Laboratory setup. (b) v_{aB} , v_{Bc} , v_{AB} , v_{BC} . (c) i_a , i_b , i_A and i_B .

3- and 5-level output line voltage waveforms were synthesized. Furthermore, inverter 1 was run at constant frequency of 50 Hz and modulation index of 0.8523; correspondingly, inverter 2 has constant frequency of 100 Hz and modulation index of 0.3024. With same constant frequencies for inverter 1 and 2, the DOI was run with inverters 1 and 2 now having modulation indices of 0.3024 and 0.8523. Individual experimental output voltage waveforms for the indicated operations are shown in Fig. 7. Experimental harmonic profiles of the 5-level inverter output line voltage waveforms in both inverters are displayed in Figs. 7(a) and (b) for 50 and 100 Hz fundamental frequencies, respectively. In these figures, the sidebands appear around the inverter switching frequency of 3.350 kHz. Also, experimental THD values (16.8 and 16.6) of the synthesized 5-level output line voltages in both inverters were shown in Fig 7(c) and (d).

The DOI peak- and mid-point operations with common modulation indices of 1.1547 and 0.57735 were experimentally typified with output frequencies of 50 and 100 Hz swapped between the first and second inverters. Experimental output voltage and current waveforms corresponding to these regional inverter operations are shown in Fig. 8. The two inverters

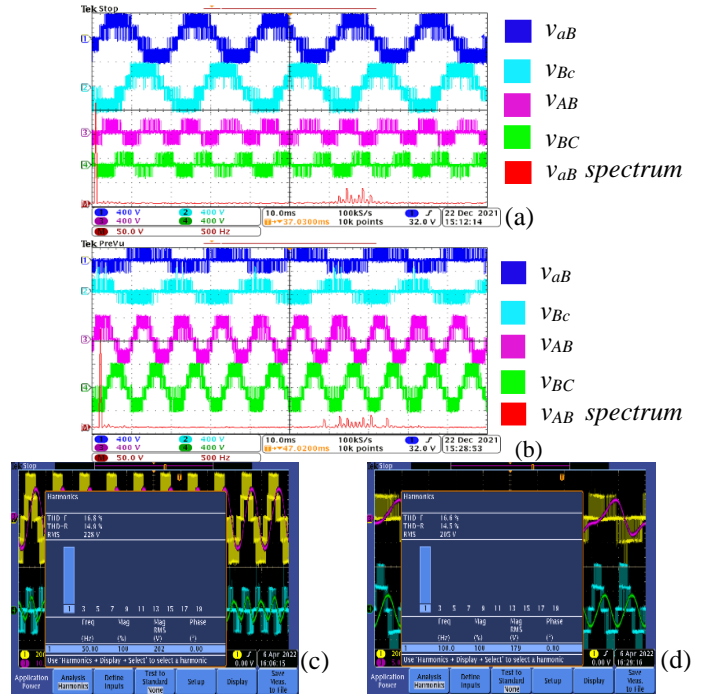


Fig.7. Output line voltage waveforms, harmonic spectra and THD values of the DOI for output frequencies of 50 and 100 Hz and modulation indices of 0.8523 and 0.3024. (a) $m_1 = 0.8523$, $f_1 = 50$ Hz, $m_2 = 0.3024$, $f_2 = 100$ Hz (b) $m_1 = 0.3024$, $f_1 = 50$ Hz, $m_2 = 0.8523$, $f_2 = 100$ Hz (c) THD value of v_{aB} at $m_1 = 0.8523$, $f_1 = 50$ Hz (d) THD value of v_{AB} at $m_2 = 0.8523$, $f_2 = 100$ Hz

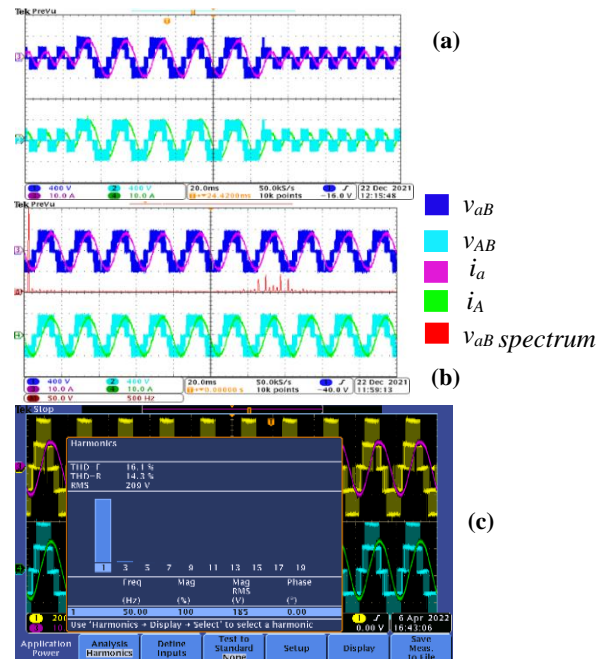


Fig. 8. Experimental output line voltages, currents and THD value of the DOI for common frequency operation of 50 Hz and modulation indices of 1.1547 and 0.57735. (a) v_{aB} , i_a , v_{AB} , i_A ; at $m_1 = m_2 = 0.57735$, $m_1 = m_2 = 1.1547$ and $f_1 = f_2 = 50$ Hz. (b) v_{aB} , i_a , v_{AB} , i_A ; at $m_1 = m_2 = 1.1547$, $f_1 = f_2 = 50$ Hz; and v_{aB} spectrum. (c) THD value of v_{aB} at $m_1 = 1.1547$, $f_1 = 50$ Hz

generate similar output waveforms. In this figure, experimental harmonic profile and THD value (16.1) of the synthesized 5-level inverter output line voltage waveform is also displayed.

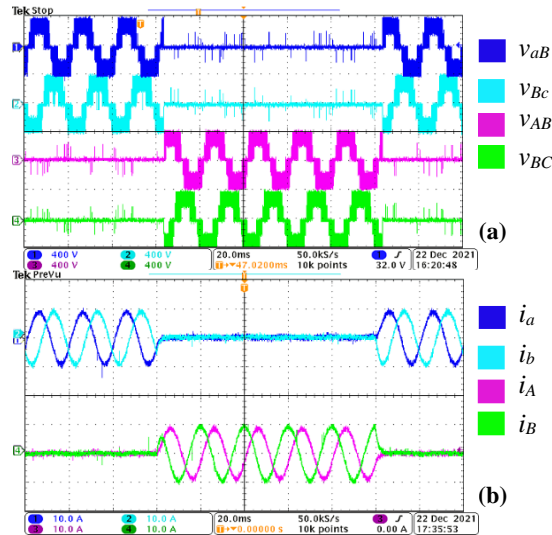


Fig. 9. Experimental output line voltages and currents of the dual-output inverter for either operation of inverter 1 or 2 in region R_4 at $f_1 = f_2 = 50$ Hz (a) V_{aB} , V_{Bc} , V_{AB} , V_{BC} , (b) i_a , i_b , i_A and i_B .

Experimental demonstration of the possibility of alternately operating inverters 1 and 2 of the proposed 3-level DOI is shown in Fig. 9. Therein, the output line voltage and current waveforms were generated for peak operation of the DOI ($m_1 = m_2 = 1.154$ and $\omega_1 = \omega_2 = 100\pi$ rad).

From the foregoing experimental verifications of the proposed 3-level DOI topological features, prototype results in Fig. 5 actually validate the capability of the inverter providing two sets of 3-phase output voltage and current waveforms to corresponding two sets 3-phase loads. Experimental results in Figs. 7 and 8 depict firm control of the deployed SPWM scheme on the operational mode boundary definition for the DOI. This is evidenced in the displayed output voltage frequency spectra and THD values in these figures. These results further portray that there is no frequency interference between inverters 1 and 2. The possibility of either operation of the inverter 1 or 2 in the proposed DOI power circuit was typified in Fig. 9; a unique feature that differentiates the parallel-common-leg approach from the series-common-switch approach.

V. CONCLUSION

A five-leg, three-level dual-output inverter topology has been presented in this letter. Detailed operational principle and control scheme for the inverter have been given. The reduced complexity in both the power circuit component-count and control/modulation approach is an innate attractive feature of the proposed DOI. For expansive experimental investigations, the inverter showed smooth transitions between specified ranges of operational modulation indices; for both common and different frequency operational modes. Moreover, additional possibility of alternate generation of one out of the two sets of 3-phase output voltage waveforms is offered by the proposed DOI configuration. The performance of the proposed dual-

output inverter has been presented through experiments on a prototype unit; results have been adequately presented.

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