# Space Vector Pulsewidth Modulation Strategy for Multilevel Cascaded H-Bridge Inverter With DC-Link Voltage Balancing Ability

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***Abstract*—Space vector pulsewidth modulation (SVPWM) algorithms for cascaded H-bridge multilevel (CHB ML) inverter usually provide the possibility of using several combinations of active voltage vectors to generate the same output voltage vector. For preselected H-bridges, some of them may generate output voltages opposite to the assumed direction. This results in the change of the dc-link voltages of these H-bridges in the opposite direction to the assumed direction in the ordering algorithm. Consequently, these algorithms are characterized by undue constraints and narrow possibilities of dc-link voltage balancing. In the proposed control algorithm, CHB ML inverter is treated as groups of successively activated three-level inverters; depending on the length of the reference voltage vector. These three-level inverters consist of three H-bridges selected from each phase. The proposed extended selection method enables firm-grip control of the dc-link voltages. For a given direction of phase currents, the possibility of using H-bridges with lowest and highest dc-link voltages is simultaneously analyzed. Additionally, each of the three-level inverters is controlled by one of three proposed alternative modulation methods for which both the attainable output voltage vectors and unbalanced dc-link voltages are predicted. Simulation and experimental results confirm the correctness of the algorithm execution.**

***Index Terms*—Cascade H-bridge multilevel inverter, cascaded H-bridge (CHB) inverter, dc-link voltages balancing, space vector pulse width modulation (SVPWM).**

## I. Introduction

THE growing popularity of multilevel inverters is due to the possibilities of generating output voltage magnitudes exceeding the blocking voltage ratings of the constituting semiconductor devices and obtaining output voltage/current waveforms similar to sinusoids. They are especially prevalent in medium voltage and high-power applications. One of the most interesting conventional topologies of multilevel inverters (MLI) is the cascaded H-bridge (CHB) inverter. It consists of H-bridge modules connected in series. Its inherent modular feature allows for easy design and maintenance, less-complex control strategies, and overall reduced production costs. Fundamentally, introduction of additional H-bridge module (with separate dc source) to the CHB inverter structure results in unit voltage step/level increase in the inverter output voltage waveform. As this configurational concept proceeds, the inverter output voltage waveform nears a sinusoid; with less harmonics content. CHB inverters are popularly deployed in power electronic transformer applications, [1]–[3], static synchronous compensator (STATCOM) [4], [5] energy storage system, [6], [7], [8]. They also have wide application in renewable generation systems, [9]–[11]; as well as in electric drive applications, [12], [13] and charging stations [14].

For proper operation of the CHB MLI, control and equalization of the separate dc-link voltages is a prerequisite. This necessity is prompted by the presence of large number of separate dc-links in the inverter power circuit structure. Most often, CHB MLIs are deplored in high-power power electronics power-conditioning systems. Hence, it is expected that individual H-bridges will be activated with a maximum or zero duty factor (actively connected or bypassed) in order to reduce commutation losses. Additionally, the legs of a CHB inverter are single phase and are subject to power pulsations at twice the fundamental frequency, [15]. This, in turn, makes it impossible to obtain identical voltages on the dc-link capacitors.

The fluctuations of dc-link voltages make it difficult to develop space vector pulse width modulation (SVPWM) control for CHB MLI. This is because the length and position of active vectors vary depending of the dc-link voltages [16], [17]. The developed SVPWM solutions in the literature mainly include methods of identifying the active vectors that can be used to generate the output voltage vector [18]. Some solutions rely on dividing the multilevel space vector diagram (SVD) into several lower level SVDs [19], [1], [20], [21]. Due to the difficulty of developing an effective SVPWM algorithm, the most popular modulation strategies used in CHB MLIs are carrier-based

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sinusoidal pulsewidth modulations (SPWM) [22]–[25]; and selective harmonic-elimination pulsewidth modulation (SHE-PWM) [26]–[29]. The SPWM strategies for an *n*-level MLI utilize the sinusoidal reference waveform and *n-1* carriers (*n* is the number of cascaded H-bridges) shifted vertically (level-shifted, LS-PWM) or horizontally (phase-shifted, PS-PWM) [30].

In general, methods of dc-link voltage balancing are related to the adopted modulation strategy. If PS-PWM strategy is used, the dc-link voltages can be equalized by sharing the reference voltage between the H-bridges [31] or by modifying their modulation indices [32]. In CHB inverters with LS-PWM, the carrier signals can be rotated between the H-bridges in every modulation cycle, [33], for the respective dc-link voltages to be equal to one another. With SHE-PWM, dc-link voltage balancing is achieved by the management of the H-bridges that will take part in the modulation, [26].

In CHB inverters with SVPWM strategies, the dc-link voltages are equalized by appropriate selection of negatively or positively connected H-bridges, where the ordering of the H-bridges used in the syntheses of the output voltage waveform depends on the direction of the power in a phase leg [15], [19]. The phase power is obtained as the product of the phase current and the reference phase voltage. The respective reference phase voltages can be obtained from the reference voltage vector using inverse Clark's transformation, [1]. The limitations of this method are related to the necessity to adopt the directions of the voltages generated by the H-bridges in each of the inverter phases. This results in rigid adoption of the order of activation of these H-bridges before starting the modulation algorithm. SVPWM algorithms usually provide the possibility of using several combinations of active voltage vectors to generate the same output voltage vector. For the preselected H-bridges, some of these active voltage vectors may generate the output voltage opposite to the assumed direction. As a result, the dc-link voltages of these H-bridges will be changed in the opposite direction to the direction assumed in the ordering algorithm.

The solution proposed in this article is based on the modification of H-bridges' voltage sorting process. The proposed sorting algorithm allows the use of both H-bridges with the highest and lowest dc-link voltages for a given phase power direction. This approach extends the possibilities of balancing the dc link voltages: Capacitors with the lowest voltage can be charged or capacitors with the highest voltage can be discharged; while generating a given reference voltage vector for any direction of phase current flow. Additional benefit is the automatic possibility of reusing preselected H-bridges for which the modulation algorithm will give a zero value of the duty factor. This usually requires complicated modifications of the sorting algorithm [1]. The results presented herein prove that by relatively small modification of the SVPWM algorithm presented in [1], it is possible to reduce the voltage fluctuations on the dc-link capacitors.

## II. Three Level Cascaded H-Bridge Inverter

The topology of a seven-level CHB inverter is shown in Fig. 1. The constituting H-bridges of the CHB inverter can be in active or zero state. In Fig. 1, considering the upper H-bridge in phase a, during the zero state two upper or lower switches ($T_1$, $T_2$ or $T_3$, $T_4$) are activated. For positive output voltage, two transistors $T_1$, $T_4$ are activated; while negative output voltage is synthesized by closing switches $T_2$ and $T_3$. The H-Bridge duty factor can be described by

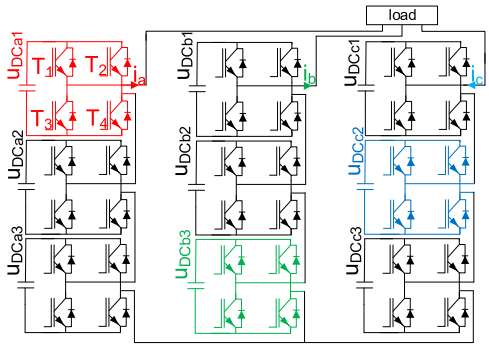



Fig. 1. Seven-level CHB inverter topology and the H-bridges selected by the ordering algorithm to form the three-level CHB inverter (red, green, and blue) controlled by the SVPWM algorithm presented in Section III.

$$\gamma = \frac{|u_o|}{u_{DC}}, \text{ where } 0 \le \gamma \le 1 \tag{1}$$

where $u_{\mathrm{dc}}$ is a dc-link voltage and $\gamma$ is a duty factor.

In Fig.1, each inverter leg consists of three series H-bridges. Three H-bridges, one from each of the inverter legs, form a three-level inverter. For a typical arbitrary inverter operation, the H-bridges selected from each phase of the inverter by the ordering algorithm to form the three-level inverter are highlighted in color in Fig. 1; red, green, blue denote selected H-bridges in phases a, b, and c, respectively. The other H-bridges are inactive (they are bypassed, with zero duty factor).

The components of the output voltage vector generated in such a three-level inverter are described by

$$\begin{aligned} u_{\alpha(3L)} &= u_{\alpha(a)} + u_{\alpha(b)} + u_{\alpha(c)} \\ u_{\beta(3L)} &= u_{\beta(a)} + u_{\beta(b)} + u_{\beta(c)} \end{aligned} \tag{2}$$

and the output vector components generated in individual H-bridges are described as

$$\begin{aligned} u_{\alpha(a)} &= \pm\sqrt{\tfrac{2}{3}} \cdot u_{DC_a},\ u_{\beta(a)} = 0 \\ u_{\alpha(b)} &= \pm\sqrt{\tfrac{2}{3}} \cdot u_{DC(b)} \cdot \cos\left(\tfrac{2\pi}{3}\right),\ u_{\beta(b)} \\ &= \pm\sqrt{\tfrac{2}{3}} \cdot u_{DC(b)} \cdot \sin\left(\tfrac{2\pi}{3}\right) \\ u_{\alpha(c)} &= \pm\sqrt{\tfrac{2}{3}} \cdot u_{DC(c)} \cdot \cos\left(\tfrac{4\pi}{3}\right), u_{\beta(c)} \\ &= \pm\sqrt{\tfrac{2}{3}} \cdot u_{DC(c)} \cdot \sin\left(\tfrac{4\pi}{3}\right) \end{aligned} \tag{3}$$

where the indexes $_{(a)}$, $_{(b)}$, and $_{(c)}$ denote the inverter phases.

The active vectors generated by the three H-Bridges (the three-level inverter) are shown in Fig. 2. It is worth noting that the multilevel CHB inverter with more than one H-bridge in each of the phases can be treated as a group of three-level inverters. In this case, subsequent groups of three-level inverters are activated when the needed output voltage is more than and cannot be generated within the previous triangle in the SVD shown in

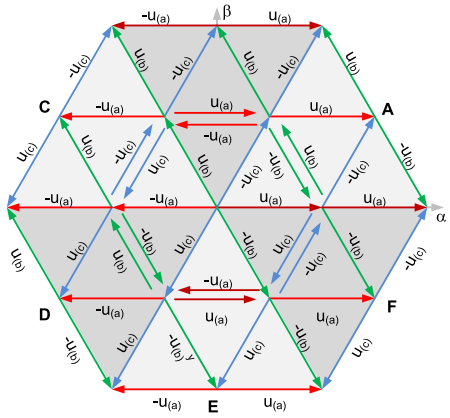



Fig. 2. Space vector diagram (SVD) of active vectors of a three-level CHB converter.

the Fig. 2. In this case, the reference voltage vector to be generated in the subsequent inverter is designated as

$$\boldsymbol{u}_{\mathrm{ref2}} = \boldsymbol{u}_{\mathrm{ref}} - \boldsymbol{u}_{\mathrm{out1}} \tag{4}$$

where $\boldsymbol{u}_{\mathbf{ref}}$ is a reference voltage vector to be generated in a multilevel CHB inverter, $\boldsymbol{u}_{\mathbf{out}}$ is the output voltage vector of the first three-level CHB inverter, $\boldsymbol{u}_{\mathbf{ref2}}$ is the output voltage vector to be generated in the next three-level inverters, as proposed in [1].

## III. Proposed Space Vector Pulsewidth Modulation Method for Three-Level Cascaded H-Bridge Inverter

In the presented solution, the CHB ML inverter is treated as group of successively activated three-level inverters (Fig. 1). The subsequent groups of three-level inverters are activated when the required output voltage is more than, and cannot be generated, in previously activated three-level inverter. Each of the three-level inverters is controlled with the SVPWM method presented below.

In most modulation algorithms, the selection of the H-bridges forming individual three-level inverters is made on the basis of information about the reference phase voltages and phase currents. The reference phase voltages can be determined using inverse Clark transformation and the reference voltage vector components. If the power drawn from the inverter phase is positive, the H-bridge with the highest dc-link voltage is activated first; and if it is negative, the H-bridge with the lowest dc-link voltage will be first used. Thus, before determining the duty factors for particular H-bridges, the polarities of the output voltages that have to be generated in the preselected H-bridges are known.

If the voltages on the dc-link capacitors are not identical, the subsectors shown in Fig. 2 no longer form symmetrical triangles (Fig. 3). The active vectors can be selected based on the angular position of the reference voltage vector, without the need to identify the subsector where its end is located. Taking into account the instantaneous values of the reference phase voltages and phase currents, the three-level CHB-inverters will be formed using the H-bridges with the lowest (index "L") or the highest

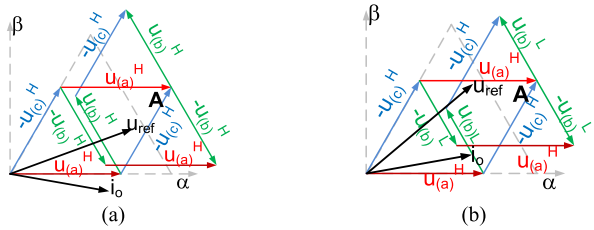



Fig. 3. Preselected active vectors for the case of unbalanced dc-link voltages and the reference voltage vector position (a) $\alpha_{\mathrm{u}} = \pi/9$ and (b) $\alpha_{\mathrm{u}} = 2\pi/9$. The output current vector position $\alpha_{\mathrm{i}} = \alpha_{\mathrm{u}} - \pi/6$. Indexes: "H" – the H-bridge with highest dc-link voltage, "L" – H-bridge with the lowest dc-link voltage, (-u) denotes negative H-bridge output voltage.

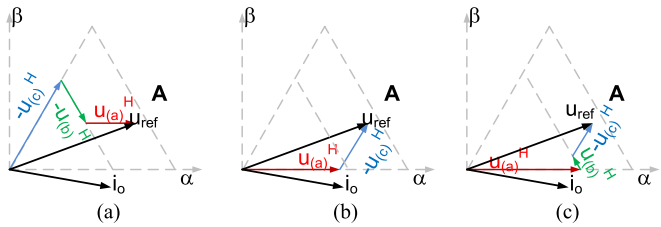



Fig. 4. Three methods to generate the reference voltage vector shown in the Fig. 3(a). The H-brides in phases a (a) or c (c) are actively connected and the H-bridge in phase b (b) is bypassed.

(index "H") dc-link voltages (as shown in Fig. 3); depending on the active power direction. Fig. 3(a) presents the situation where the reference phase voltage is as follows: $u_a>0$, $u_b<0$, and $u_c<0$; while the phase current directions are $i_a>0$, $i_b<0$, $i_c<0$. It means that the H-bridges with highest, "H", dc-link voltages will be first used in all inverter phases. The phase voltages in the situation presented in Fig. 3(b) are $\mathrm{u_a}>0$, $\mathrm{u_b}>0$, $\mathrm{u_c}<0$; while the phase current directions remain unchanged. It means that H-bridge with the lowest, "L," dc -link voltage in phase "b" will be utilized first.

The SVPWM algorithms make it possible to use more than one combination of active vectors to create a reference voltage vector. For the case shown in Fig. 3(a), the reference voltage vector can be composed using the active vectors: $+u_{(\mathrm{a})}{}^{\mathrm{H}}$, $-u_{(\mathrm{b})}{}^{\mathrm{H}}$, $-u_{(\mathrm{c})}{}^{\mathrm{H}}$; $+u_{(\mathrm{a})}{}^{\mathrm{H}}$, $-u_{(\mathrm{c})}{}^{\mathrm{H}}$, and $+u_{(\mathrm{a})}{}^{\mathrm{H}}$, $+u_{(\mathrm{b})}{}^{\mathrm{H}}$, $-u_{(\mathrm{c})}{}^{\mathrm{H}}$ in Fig. 4(a)–(c), respectively, (+/- denotes the direction of generated output voltage in individual H-bridges). This means that for the negative current in the phase "b," the highest value of the dc-link voltage $u_{\mathrm{DC(b)}}$ will be reduced in Fig. 4(a), will remain unchanged in Fig. 4(b) or will be increased in Fig 4(c). It is worth noting that each of the analyzed cases ensure one of the H-bridges to be bypassed or actively connected.

The conclusion is that the active vectors for particular sectors should be dynamically rearranged. One of the solutions to this problem is to ensure the possibility of using both the H-bridges with the lowest and highest dc-link voltage for any direction of active power flow. The sorting procedure proposed in this article assumes the possibility of using both H-bridges with the highest and the lowest dc-link voltage to generate the reference output voltage vector. For a positive active power value, determined on the basis of the reference phase voltages and the phase current, two indices are created simultaneously for each of the inverter

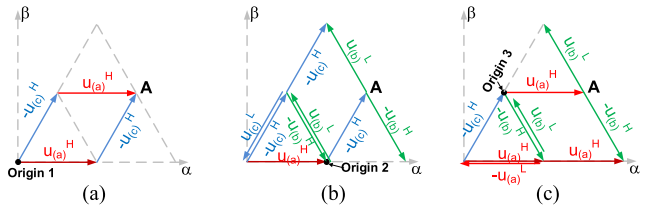



Fig. 5. Three methods of active vector selection with the use of: the H-bridges with (a) the highest (H) dc-link voltages in phases a and c, (b) the highest (H) dc-link voltages in phase a and highest or lowest (L) in phases b and c, and (c) highest dc-link voltages in phase c, and highest or lowest in phases a and b.

phases: "H" – the H-bridges with the highest dc voltage and "L"– the H-bridges with the lowest dc voltage. In the first stage, it is assumed that "H" equals "1" (which means the H-bridge with the highest dc-voltage in the analyzed phase) and "L" equals "*n*" (which means the H-bridge with the lowest dc-link voltage, "*n*" is the number of H-bridges connected in series in the inverter phase). The choice of the H-bridge ("H" or "L") that will eventually be used to generate the output voltage vector depends on the polarity of the H-bridge output voltage determined in the modulation algorithm shown below.

The modulation algorithm uses three potential scenarios/methods of generating the output voltages. The final choice of the method used to generate the output voltages depends on the possibilities of generating the reference voltage vector and balancing the dc-link voltages.

### A. Scenario 1: The Use of Two Active Vectors

The first method uses two nonzero voltages generated in two H-bridges. For positive active power, these will be the H-bridges with the highest ("H") dc-link voltages, [Fig. 5(a)]. The duty factors for three H-bridges are determined as

$$\begin{aligned}
\gamma_{(a)}{}^{H} &= \frac{u_{\mathrm{ref}\alpha}\cdot u_{\beta(c)}{}^{H} - u_{ref\beta}\cdot u_{\alpha(c)}{}^{H}}{u_{\beta(c)}{}^{H}\cdot u_{\alpha(a)}{}^{H} - u_{\alpha(c)}{}^{H}\cdot u_{\beta(a)}{}^{H}} \\
\gamma_{(b)}{}^{H/L} &= 0 \\
\gamma_{(c)}{}^{H} &= \frac{u_{ref\beta}\cdot u_{\alpha(a)}{}^{H} - u_{ref\alpha}\cdot u_{\beta(a)}{}^{H}}{u_{\beta(c)}{}^{H}\cdot u_{\alpha(a)}{}^{H} - u_{\alpha(c)}{}^{H}\cdot u_{\beta(a)}{}^{H}}
\end{aligned} \tag{5}$$

where $u_{\mathrm{ref}\alpha}$ and $u_{\mathrm{ref}\beta}$ are the components of the reference voltage vector $\boldsymbol{u}_{\mathbf{ref}}$; and $u_{\alpha(\mathrm{p})}{}^{\mathrm{H}}$ and $u_{\beta(\mathrm{p})}{}^{\mathrm{H}}$ are the components of the active voltage vectors generated by the H-bridges with the highest dc-link voltages in the "p" phase ($p = a$, $b$, or $c$). It is worth noting that a zero duty factor is provided for one of the H-bridges and this H-bridge remains bypassed throughout the pulse period.

For the active vectors shown in Fig. 5(a), both calculated duty factors $\gamma_{(a)}{}^{\mathrm{H}}$ and $\gamma_{(c)}{}^{\mathrm{H}}$ will be positive and limited to a maximum value of 1

$$if\,\gamma_{(a)}{}^{H} > 1 \Rightarrow \gamma_{(a)}{}^{H} = 1;\ \gamma_{(c)}{}^{H} > 1 \Rightarrow \gamma_{(c)}{}^{H} = 1. \tag{6}$$

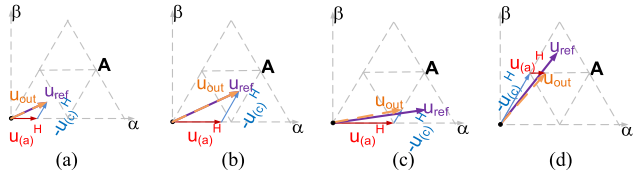



Fig. 6. Generating a reference voltage vector $u_{\mathrm{ref}}$ located in individual subsectors of sector A (a)–(d) using method 1. $u_{\mathrm{out}}$ – an output voltage vector.

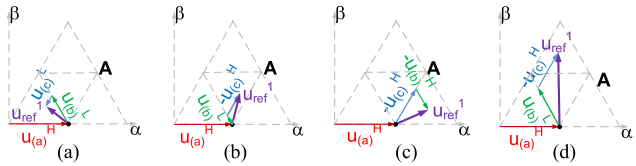



Fig. 7. Generating a reference voltage vector $u_{\mathrm{ref}}$ located in individual subsectors of sector A (a)–(d) using method 2. The reference voltage vector $u_{\mathrm{ref1}}$ components are determined as (7).

This limits the possibility of obtaining an output voltage vector with a given position and amplitude, as shown Fig. 6(c) and (d).

### B. Scenario 2: With the Origin Located at the End of the First Active Voltage Vector

The SVPWM algorithm presented in [1] was aimed at obtaining a duty factor of 0 or 1 for one of the H-bridges forming three-level CHB inverter. The same effect can be obtained more easily by shifting the origin of the reference voltage vector to the end of one of the active vectors shown in the Fig. 5(a). If the origin of the reference vector is shifted to the end of the vector $\boldsymbol{u}_{(\mathbf{a})}{}^{\mathbf{H}}$ Fig. 5(b)], the new values of its components can be determined as [Fig. 7(a)]

$$\begin{aligned}
u_{\mathrm{ref}\alpha}{}^{1} &= u_{\mathrm{ref}\alpha} - u_{a\alpha}{}^{H} \\
u_{\mathrm{ref}\beta}{}^{1} &= u_{\mathrm{ref}\beta} - u_{a\beta}{}^{H}.
\end{aligned} \tag{7}$$

For the phase currents, $i_a>0$, $i_b<0$, and $i_c<0$, the possibility of generating a reference voltage vector with such defined components is first analyzed for the active vectors with the highest, "H," dc-link voltage. Hence, the duty factors of H-bridges with the highest dc-link voltages, $\boldsymbol{u}_{(\mathbf{a})}{}^{\mathbf{H}}$, $\boldsymbol{-u}_{(\mathbf{b})}{}^{\mathbf{H}}$, and $\boldsymbol{-u}_{(\mathbf{c})}{}^{\mathbf{H}}$, can be determined as

$$\begin{aligned}
\gamma_{(a)}{}^{H} &= 1 \\
\gamma_{(b)}{}^{H} &= \frac{u_{\mathrm{ref}\alpha}{}^{1}\cdot u_{\beta(c)}{}^{H} - u_{ref\beta}{}^{1}\cdot u_{\alpha(c)}{}^{H}}{u_{\beta(c)}{}^{H}\cdot u_{\alpha(b)}{}^{H} - u_{\alpha(c)}{}^{H}\cdot u_{\beta(b)}{}^{H}} \\
\gamma_{(c)}{}^{H} &= \frac{u_{ref\beta}{}^{1}\cdot u_{\alpha(b)}{}^{H} - u_{ref\alpha}{}^{1}\cdot u_{\beta(b)}{}^{H}}{u_{\beta(c)}{}^{H}\cdot u_{\alpha(b)}{}^{H} - u_{\alpha(c)}{}^{H}\cdot u_{\beta(b)}{}^{H}}.
\end{aligned} \tag{8}$$

Note that, duty factor of 1 is provided for one of the H-bridges and this very one remains actively connected throughout the pulse period.

Both (5) and (8) use the actual values of dc-link voltages of the utilized H-bridges. Thus, the dc-link voltage changes will not affect the correct generation of the inverter output voltage. The determined duty factor for one or two remaining H-bridges can be positive or negative depending on the reference voltage vector length and position. This means that these H-bridges will be used to generate the output voltages of opposite polarity to that assumed in the sorting algorithm, and this results in their dc-link voltages being charged instead of discharged. Therefore, it is necessary to replace these H-bridges with the H-bridges with the lowest dc-link voltages [as shown in Fig. 7(a) where $\mathbf{-u_{(b)}^{H}}$ and $\mathbf{-u_{(c)}^{H}}$ are replaced with $\mathbf{u_{(b)}^{L}}$ and $\mathbf{u_{(c)}^{L}}$, respectively; and in Fig. 7(b) and (d), where $\mathbf{-u_{(b)}^{H}}$ is replaced with $\mathbf{u_{(b)}^{L}}$); recalculating their duty factors

$$\begin{aligned} &if \gamma_{(b)}{}^{H} < 0 \Rightarrow \ \gamma_{(b)}{}^{L} = \left|\gamma_{(b)}{}^{H}\right| \cdot \frac{\left|\boldsymbol{u}_{(b)}{}^{H}\right|}{\left|\boldsymbol{u}_{(b)}{}^{L}\right|}, \gamma_{(b)}{}^{H} = 0 \\ &if \gamma_{(c)}{}^{H} < 0 \Rightarrow \ \gamma_{(c)}{}^{L} = \left|\gamma_{(c)}{}^{H}\right| \cdot \frac{\left|\boldsymbol{u}_{(c)}{}^{H}\right|}{\left|\boldsymbol{u}_{(c)}{}^{L}\right|}, \gamma_{(c)}{}^{H} = 0. \end{aligned} \tag{9}$$

Such scaling of the duty factors, taking into account the actual dc-link voltages, ensures correct generation of the output voltages in the newly indicated H-bridges.

Only the position of the reference voltage vector shown in Fig. 7(c) provides positive duty factors calculated for all the preselected active vectors $\mathbf{u_{(a)}^{H}}$, $\mathbf{-u_{(b)}^{H}}$, and $\mathbf{-u_{(c)}^{H}}$. This is the main difference between the proposed solution and the solution demonstrated in [1] and [19]; therein, the negative value of the duty factor resulted in the need to generate a output voltage vector using only two active vectors with a limited value of the duty factor.

Since the determined duty factors may be greater than 1, specified constraints are needful

$$\begin{aligned} &if\ \gamma_{(b)}{}^{H} > 1 \Rightarrow \gamma_{(b)}{}^{H} = 1; \quad if\ \gamma_{(c)}{}^{H} > 1 \Rightarrow \gamma_{(c)}{}^{H} = 1 \\ &if\ \gamma_{(b)}{}^{L} > 1 \Rightarrow \gamma_{(b)}{}^{L} = 1; \quad if\ \gamma_{(c)}{}^{L} > 1 \Rightarrow \gamma_{(c)}{}^{L} = 1. \end{aligned} \tag{10}$$

Generating an output voltage vector with the use of H-bridges with the highest (H) and the lowest (L) dc-link voltages is depicted in Fig. 7.

### C. Scenario 3: With the Origin Located at the End of the Second Active Voltage Vector

The third modulation scenario is based on the same active vectors $\mathbf{u_{(a)}^{H}}$, $\mathbf{-u_{(b)}^{H}}$, and $\mathbf{-u_{(c)}^{H}}$ as the scenario 2. The origin of the reference vector is shifted to the end of the second active vector $\mathbf{-u_{(c)}^{H}}$ [ Fig. 5(c)]

$$\begin{aligned} u_{\mathrm{ref}\alpha}{}^{2} &= u_{\mathrm{ref}\alpha} - u_{c\alpha}{}^{H} \\ u_{\mathrm{ref}\beta}{}^{2} &= u_{\mathrm{ref}\beta} - u_{c\beta}{}^{H} \end{aligned} \tag{11}$$

and the duty factors are determined for the active vectors $\mathbf{u_{(a)}^{H}}$, $\mathbf{-u_{(b)}^{H}}$, and $\mathbf{-u_{(c)}^{H}}$ as

$$\begin{aligned} \gamma_{(a)}{}^{H} &= \frac{u_{\mathrm{ref}\alpha}{}^{2} \cdot u_{\beta(b)}{}^{H} - u_{ref\beta}{}^{2} \cdot u_{\alpha(b)}{}^{H}}{u_{\beta(b)}{}^{H} \cdot u_{\alpha(a)}{}^{H} - u_{\alpha(b)}{}^{H} \cdot u_{\beta(a)}{}^{H}} \\ \gamma_{(b)}{}^{H} &= \frac{u_{ref\beta}{}^{2} \cdot u_{\alpha(a)}{}^{H} - u_{ref\alpha}{}^{2} \cdot u_{\beta(a)}{}^{H}}{u_{\beta(b)}{}^{H} \cdot u_{\alpha(a)}{}^{H} - u_{\alpha(c)}{}^{H} \cdot u_{\beta(b)}{}^{H}} \\ \gamma_{(c)}{}^{H} &= 1. \end{aligned} \tag{12}$$

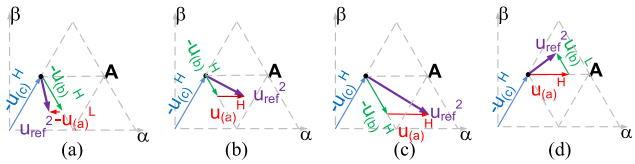



Fig. 8. Generating a reference voltage vector $u_{\mathrm{ref}}$ located in individual subsectors od sector A (a)–(d) using method 3. The reference voltage vector $u_{\mathrm{ref2}}$ components are determined as (11).

Duty factor of "1" is assigned to one of the H-bridges. In this case, either or both of the remaining two duty factors may be positive or negative. Because negative duty factors indicate that the corresponding polarity of the H-bridge output voltage will be opposite to the assumed one, it is necessary to replace the H-bridges with those with the lowest dc-link voltage

$$\begin{aligned} &if \gamma_{(a)}{}^{H} < 0 \Rightarrow \gamma_{(a)}{}^{L} = \left|\gamma_{(a)}{}^{H}\right| \cdot \frac{\left|\boldsymbol{u}_{(a)}{}^{H}\right|}{\left|\boldsymbol{u}_{(a)}{}^{L}\right|}, \gamma_{(a)}{}^{H} = 0 \\ &if \gamma_{(b)}{}^{H} < 0 \Rightarrow \ \gamma_{(b)}{}^{L} = \left|\gamma_{(b)}{}^{H}\right| \cdot \frac{\left|\boldsymbol{u}_{(b)}{}^{H}\right|}{\left|\boldsymbol{u}_{(b)}{}^{L}\right|}, \gamma_{(b)}{}^{H} = 0. \end{aligned} \tag{13}$$

Since the determined duty factors may be greater than 1, they must be limited

$$\begin{aligned} &if\ \gamma_{(a)}{}^{H} > 1 \Rightarrow \gamma_{(a)}{}^{H} = 1; \ if\ \gamma_{(b)}{}^{H} > 1 \Rightarrow \gamma_{(b)}{}^{H} = 1 \\ &if\ \gamma_{(a)}{}^{L} > 1 \Rightarrow \gamma_{(a)}{}^{L} = 1; \ if\ \gamma_{(b)}{}^{L} > 1 \Rightarrow \gamma_{(b)}{}^{L} = 1. \end{aligned} \tag{14}$$

Generation of an output voltage vector with the use of H-bridges with the highest (H) and the lowest (L) dc-link voltages is shown in Fig. 8(a), where $\mathbf{u_{(a)}^{H}}$ is replaced with $\mathbf{-u_{(a)}^{L}}$, and in Fig. 8(d), where $\mathbf{-u_{(b)}^{H}}$ is replaced with $\mathbf{u_{(b)}^{L}}$. Only the position of the reference voltage vector, shown in Fig. 8(b) and (c), provides positive duty factors calculated for all the preselected active vectors $\mathbf{u_{(a)}^{H}}$, $\mathbf{-u_{(b)}^{H}}$, and $\mathbf{-u_{(c)}^{H}}$.

## IV. SVPWM Method for Multilevel CHB Inverter

The presented solution uses the division of a CHB multilevel inverter into series three-level inverters. A single three-level inverter is formed by three H-bridges selected from each of the phases. In each of these three-level inverters, the algorithms presented in Section III determine the nonzero duty factors for the H-bridges with the highest (H) or lowest (L) dc-link voltages using three alternative modulation methods. For each of the modulation methods, the resulting output vector components and resulting duty factors are determined as

$$\begin{aligned} &if(\gamma_{(a)}{}^{H} \neq 0) \Rightarrow \ u_{\alpha(a)} = u_{\alpha(a)}{}^{H}, u_{\beta(a)} = u_{\beta(a)}{}^{H} \\ &u_{DC(a)} = u_{DC(a)}{}^{H}, \ \gamma_{(a)} = \gamma_{(a)}{}^{H} \\ &\vdots \\ &if(\gamma_{(c)}{}^{L} \neq 0) \ \Rightarrow \ u_{\alpha(c)} = u_{\alpha(c)}{}^{L}, u_{\beta(c)} = u_{\beta(c)}{}^{L} \\ &u_{DC(c)} = u_{DC(c)}{}^{L} \ \gamma_{(c)} = \gamma_{(c)}{}^{L} \end{aligned} \tag{15}$$

and the synthesizable output voltage vector components are determined as

$$\begin{aligned} u_{\mathrm{out}1\alpha} &= \gamma_{(a)} \cdot u_{\alpha(a)} + \gamma_{(b)} \cdot u_{\alpha(b)} + \gamma_{(c)} \cdot u_{\alpha(c)} \\ u_{out1\beta} &= \gamma_{(a)} \cdot u_{\beta(a)} + \gamma_{(b)} \cdot u_{\beta(b)} + \gamma_{(c)} \cdot u_{\beta(c)} \end{aligned} \tag{16}$$

where the components of active vectors $u_{\alpha(a..c)}$ and $u_{\beta(a..c)}$ are defined by (3).

The duty factors constraint in (6), (10), and (14) applies. For each of the modulation scenarios, the reference voltage vector components for the next three-level CHB inverter are determined using (4). At the same time, for each modulation scenario the imbalance factor is determined as proposed in [1]

$$f\left(u_{DC(a)}, u_{DC(b)}, u_{DC(c)}\right) = \left\{ \begin{array}{l} \left(u_{DC(a)}\left(k+1\right) - u_{DC(AV)}\right)^2 + \\ \left(u_{DC(b)}\left(k+1\right) - u_{DC(AV)}\right)^2 + \\ \left(u_{DC(c)}\left(k+1\right) - u_{DC(AV)}\right)^2 \end{array} \right\} \tag{17}$$

where

$$u_{DC(AV)} = \frac{u_{DC(a)}\left(k+1\right) + u_{DC(b)}\left(k+1\right) + u_{DC(c)}\left(k+1\right)}{3} \tag{18}$$

$$u_{DC(p)}\left(k+1\right) = u_{DC(p)}\left(k\right) + \frac{1}{C} \cdot \gamma_{(p)} \cdot T_{\text{pulse}} \cdot i_{(p)} \tag{19}$$

where $p$ is the phase of CHB inverter ($p = a$, $b$, or $c$); $C$ is the dc-link capacitance; and $k$ and $k+1$ denote the dc-link voltages determined for the actual and next pulse periods.

If the amplitude of the output voltage vector, $|\boldsymbol{u}_{\text{ref2}}|$, determined for the next three-level inverter in (4) will be equal to zero for at least one of the analyzed modulation scenarios, the modulation scenario that provides zero length of reference voltage $|\boldsymbol{u}_{\text{ref2}}|$, and the smallest value of the imbalance factor in (17) will be used to generate the inverter output voltage. If none of the analyzed strategies provide zero length of $|\boldsymbol{u}_{\text{ref2}}|$vector, the output voltage vector is generated using the modulation strategy providing the output voltage vector closest to the reference voltage vector [minimum value of the function (20)]

$$f\left(u_{\text{out1}\alpha}, u_{out1\beta}\right) = \left(u_{ref\alpha} - u_{out1\alpha}\right)^2 + \left(u_{ref\beta} - u_{out1\beta}\right)^2 \tag{20}$$

which ensures the possibility of using the minimum number of dc-links to generate the output voltage vector.

At this juncture, the modulation scenario was selected, which can be used to generate the output voltage in three H-bridges (in three-level CHB inverter).

Generating the output voltage in successive three-level inverters (next three H-bridges) of multilevel CHB inverter requires the indication of successive, previously unused H-bridges with the highest and the lowest dc link voltages. It is, therefore, necessary to increment/decrement the counter indicating the next usable H-bridges. These H-bridges will be considered in the generation of the output voltage in subsequent three-level inverters. In the case of zero duty factor, the counter indicating the next usable H-bridge will not be changed

$$\begin{array}{l} if\ \left(\gamma_{(a)}{}^{H} \neq 0\right) \Rightarrow\ H_{(a)} = \left(H_{(a)} + 1\right)\ \text{else}\ H_{(a)} = H_{(a)} \\ \qquad\qquad \vdots \\ if\ \left(\gamma_{(c)}{}^{L} \neq 0\right) \Rightarrow\ L_{(c)} = \left(L_{(c)} - 1\right)\ else\ L_{(c)} = L_{(c)} \end{array} \tag{21}$$

where $H_{(a)}$ denotes the H-bridge with the highest dc-link voltage in the phase "a," while $L_{(c)}$ denotes the H-bridge with the lowest dc-link voltage in the phase "c." In this way, the H-bridges with zero duty factors can be reused to generate the output voltage vector in the successive three-level CHB inverters of a multilevel CHB inverter.

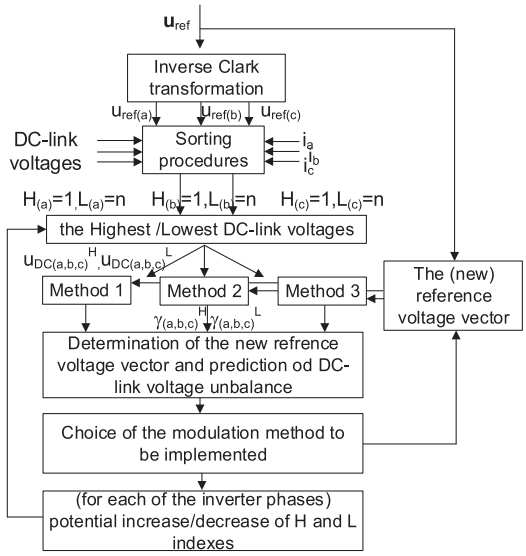



Fig. 9. Diagram of the proposed SVPWM method.

The diagram presenting the proposed SVPWM algorithm is showed in Fig. 9. In the presented solution, the CHB ML inverter is treated as a group of successively activated three-level inverters (Fig. 1). The subsequent groups of three-level inverters are activated when the required output voltage cannot be generated in previously activated three-level inverters. Each of the three-level inverters is controlled with the SVPWM method presented in Section III. In practice, this modulation strategy has to be executed one, two, or "$n$" times, depending on the length of the reference voltage vector ("$n$" is the number of cells connected in series). That means, that the short reference vector can be generated using only one of the three-level inverter, the rest of the cells will remain bypassed (with zero value of duty factors). The first execution of SVPWM can select one of "$n$" cells in each of the inverter phases. The next execution is based on "$n$-1" or "$n$" cells, depending on whether nonzero or zero duty factors were determined for the cells selected in the first execution of the SVPWM algorithm. The entire algorithm is repeated until the entire reference voltage is obtained.

## V. Simulation and Experimental Results

In order to demonstrate the features of the proposed solution with respect to dc-link voltage stabilization, simulation studies were carried out and the results were compared with those from the modulation strategy proposed in [1]. Both algorithms were implemented in the PLECS simulation software for a seven-level CHB inverter (three H-bridges connected in series per phase). For these algorithms, the same supply, load parameters, and switching frequency were used. The inverter dc-links were supplied by single phase diode rectifier. The detailed parameters are shown in Table I. In order to present the voltage imbalance

TABLE I
SIMULATION TEST CONDITION

| | |
|---|---|
| rectifier | Single phase diode rectifiers |
| inverter | 7L CHB (3 H-Bridges connected in series per phase) |
| supply | 3x400V, 50Hz |
| DC-link capacitance | 2400 μF in each cell |
| switching frequency | 3.33 kHz |

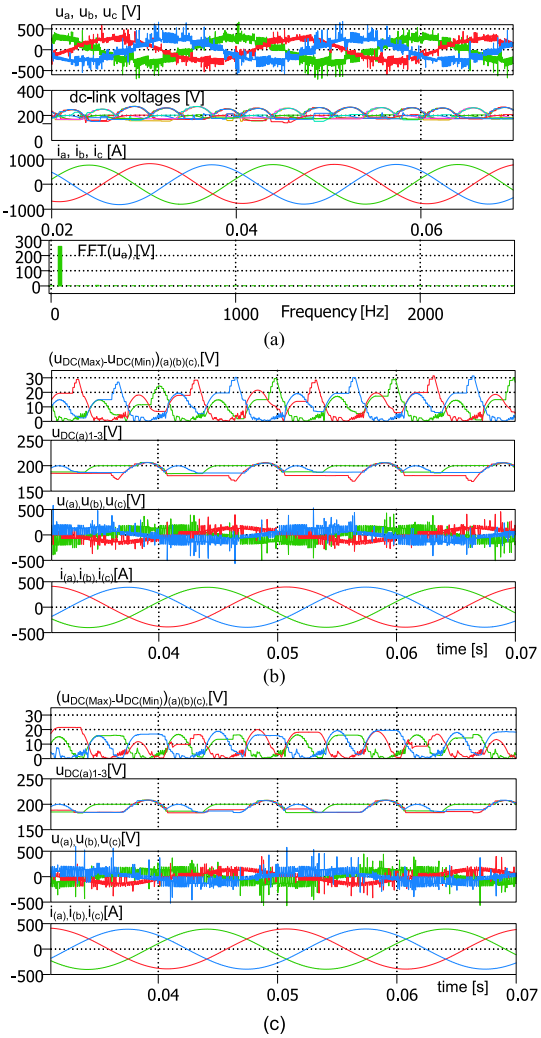



Fig. 10. Waveforms of the output phase voltages and currents, (a) the dc-link voltages in one of inverter legs and phase voltage harmonics. (b), (c) Difference between the highest and the lowest dc-link voltage in a seven-level CHB inverter phases, the dc-link voltages, the output phase voltages, and currents obtained using the SVPWM strategy proposed in [1](b) and proposed in this article (c), The length of the reference voltage vector 320 V.

in the dc circuit, the simulation tests were carried out for large values of the load currents, with three-phase $RL$ load ($R = 0.1\ \Omega$ and $L = 1$ mH). The length of the reference voltage vector was equal to 320 V. Fig. 10(a) shows the waveforms of the output phase voltages and currents obtained using proposed algorithm and also phase voltage harmonics. Shown in the same figure are the waveforms of dc-link voltages in one of the inverter legs; as well as the dc-link voltages in one corresponding H-bridges in

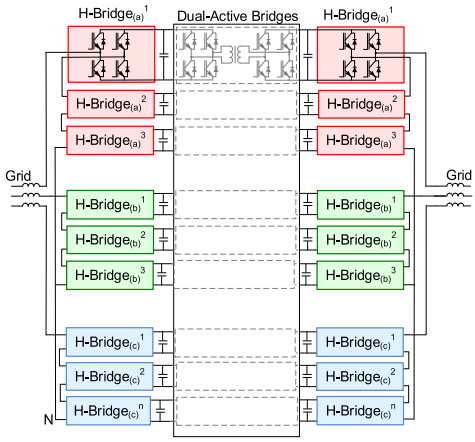



Fig. 11. Structure of CHB inverters coupled with dual active H-bridges.

all the phases. From these simulated figures, it is apparent that despite the voltage fluctuations on the inverter capacitors, the output voltages were generated correctly without undesirable harmonics. This is due to the fact, that the values of the active vector components used in (5), (8), and (9) depend on the instantaneous values of the dc link voltages (3).

Fig. 10(b) and (c) show the difference between the highest and lowest dc-link voltages in all the inverter phases obtained using the modulation strategy proposed in [1] [Fig. 10(b)] and that proposed herein [Fig. 10(c)]; for the same supply and loading conditions. The length of the reference voltage vector is 160 V. The proposed solution helps depress the low-frequency fluctuations on the dc-link capacitors. This is due to the ordering of H-bridges based not on the basis of the reference phase voltage and current but on the basis of the actual voltage generated in the H-bridges and the phase currents.

The experimental tests were performed on a seven-level CHB converter containing two active-front inverters working on the same grid (in loop) (Fig. 11). The nominal parameters are: Power 600 kW, dc-link voltage 1-kV/ H-bridge, and supply voltage $3 \times 3.3$ kV. The dc-links of both inverters were coupled using 70 kW/1-kV dual active bridge (DABs) with custom-made MF (7 kHz) transformers and dc-link capacitance of 2.4 mF. The supply voltage was reduced to $3 \times 400$ V. Both CHB inverters on either side of the DABs were controlled using a single control board containing ADSP20363 (DSP processor) and Cyclone II FPGA. The DABs have their own separate control boards. The control systems of both CHB inverters and the DABs were not coupled; only the information about switching state (ON or OFF) of the inverters were sent. The detailed parameters are shown in Table II.

This inverter system was used to convert up to 20 kW of power, Fig. 12. The reference dc-link voltage was set to 200 V/per cell. The waveforms of the line output voltage and phase current are presented in Figs. 13 and 14. The output voltage harmonics are shown in Fig. 13, while the output current harmonics are presented in Fig. 14. Fig. 15 presents the output voltage THD and harmonics. The THD-R of the output voltage is 2.56%. The harmonics shown there are due to the dead-time effect. The

TABLE II
EXPERIMENTAL TEST CONDITION

| | |
|---|---|
| rectifier | 7l CHB active front rectifier |
| inverter | 7L CHB inverter |
| supply / load | 3x400V, 50Hz (work in the loop) |
| DC-link capacitance | 2400 µF in each cell |
| switching frequency (inverters) | 3.33 kHz |
| Switching frequency (DABs) | 7 kHz |
| Utilized transistors | MMG150D170B6EN IGBTs |

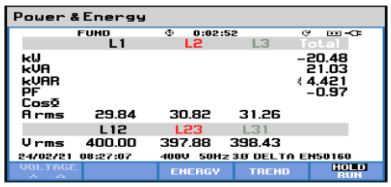



Fig. 12. Supply parameters during the experimental tests.

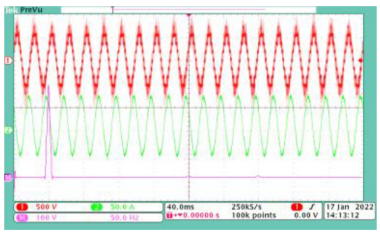


Fig. 13. Output voltage (1), Phase current (2), and output voltage harmonics obtained using proposed SVPWM algorithm. Scale: Waveforms 50 A/div, 500 V/div, 40 ms/div, harmonics 100 V/div, 50 Hz/div.

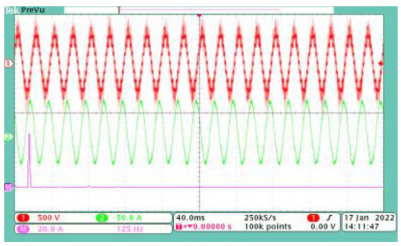


Fig. 14. Output voltage (1) and current (2) and the output current harmonics obtained using proposed SVPWM algorithm. Scale: Waveforms 50 A/div, 500 V/div, 40 ms/div, harmonics 20 A/div, 125 Hz/div.

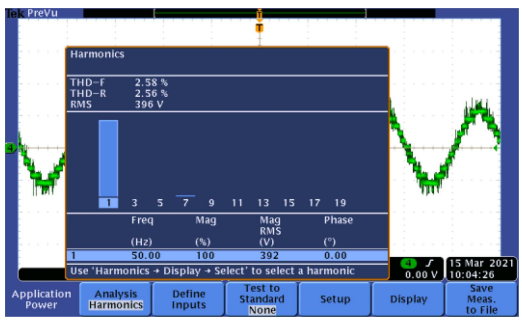



Fig. 15. Output voltage and output voltage harmonics and THD obtained using proposed SVPWM algorithm.

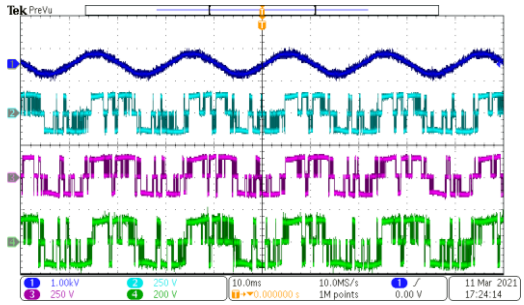


Fig. 16. Waveforms of inverter output voltage (1) and the output voltages of three H-bridges in the same inverter phase (2–3). Scale 1 kV/div (1), 250 V/div (2-3), 200 V/div (4), 10 ms/div.

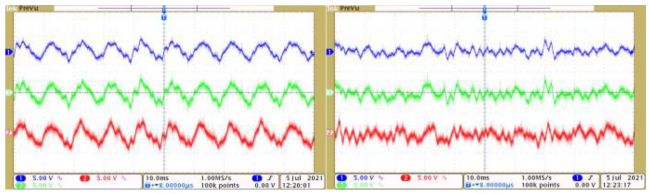


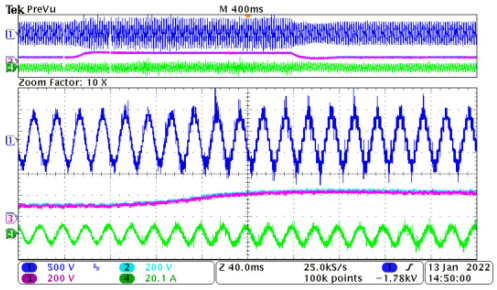

Fig. 17. AC components of dc-link voltages of three H-bridges in the same inverter phase. Scale 5 V/div, 10 ms/div (a) With SVPWM algorithm in [1], and (b) With SVPWM algorithm proposed in this article.

dc-link voltage variations do not affect the harmonic distribution, as shown in Fig. 10.

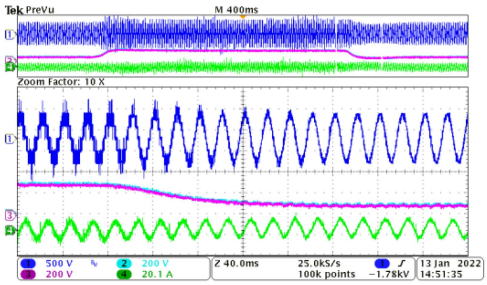
The waveform of seven-level CHB inverter output voltage and the output voltages of all the H-bridges in a single inverter phase are shown in Fig. 16.

The structure of 7L CHB converter used in experimental tests includes independently controlled inverters and DABs (Fig. 11). The energy fed by DAB into the separate capacitors constitutes a disturbance that must be reduced by the SVPWM algorithm. In turn, the SVPWM equalizes the dc-link voltages in a single CHB inverter and consequently disrupts the operation of DAB. This means that the system works constantly in a transient state, where one system interferes with the operation of the other (DAB disrupts the operation of SVPWM algorithms, SVPWM algorithm disrupt the operation of DABs). Fig. 17 compares the experimental ac components of the dc-link voltages obtained in one of the inverter phases for the same supply and loading conditions. In this figure, the SVPWM methods in [1] [Fig. 17(a)] and that presented herein [Fig. 17(b)] were used. In both cases, the control system structure and the parameters of PI controllers remain the same.

The low-frequency fluctuations on the dc-link capacitors are reduced [Fig. 17(b)]. The high-frequency dc-link voltage changes evidenced and visible in Fig. 17(b) are the result of simultaneous influencing the dc-link voltages by the proposed modulation algorithm and DABs, where DAB disrupts the operation of SVPWM algorithms and SVPWM algorithm disrupt the operation of DABs. It should be emphasized that even a small deviation in both dc voltages causes the operation of both algorithms (there is no deadband).

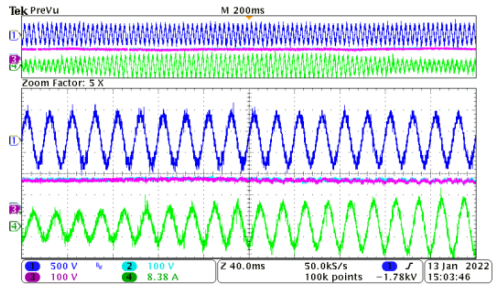



(a)

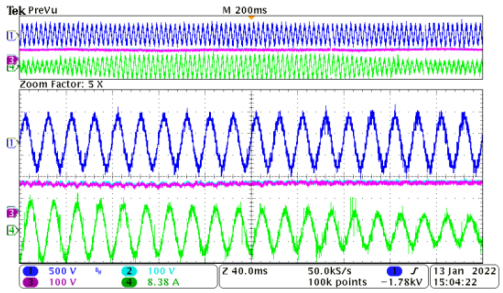



(b)

Fig. 18. Waveforms of the output voltage (1), Two dc-link voltages in one of inverter phases (2) and (3) and the output current (4) While changing the reference dc-link voltages in all H-Bridges from 120 V to 300 V(a), and from 300 to 120 V (b). The output power is 10 kW. Scale: 500 V/div(1), 200 V/div (2-3), 20.1 A/div (4), 40 ms/div.




(a)




(b)

Fig. 19. Waveforms of the output voltage (1), Two dc-link voltages in one of inverter phases (2) and (3) and the output current (4) While changing transmitted active power from 3.3 to 17 kW (a), and from 17 kW to 3.3 kW (b). The reference dc-link voltage is 120 V. Scale: 500 V/div (1), 100 V/div (2-3), 8.38 A/div (4), 40 ms/div.

Fig. 18 shows the waveform of the output voltages, load current, and the dc-link voltages of two H-bridges in the same inverter phase when changing the reference dc-link voltages from 120 to 300 V and from 300 to 120 V; the same reference dc voltage is in all dc-links. Increasing the reference dc-link voltage resulted in a decrease in the number of levels of output voltage. This is because a smaller number of H-bridges was enough to generate the same value of the output voltage; the remaining H-bridges were not used (were bypassed).

The waveforms shown in Fig. 19 concern changes of the active power transmitted by the converter from 3.3 to 17 kW and from 17 to 3.3 kW. During this test, the reference value of dc-link voltages was 120 V.

In both presented cases, changes in the reference value of the dc voltages and the converted power do not affect the imbalance of the voltages in the dc circuits.

## VI. Conclusion

Presented in this article is the SVPWM algorithm for CHB ML inverter with dc-links voltage balancing ability. The CHB ML inverter is treated as group of successively activated three-level inverters; depending on the length of the reference voltage vector. Each of the three-level inverters is controlled using one of three proposed SVPWM methods. The H-bridges used to form the three-level inverters are selected based on the proposed ordering algorithm. The proposed control approach enables the use of both H-bridges with highest and lowest dc-link voltages for a given direction of phase current flow. Simulation and experimental tests and results herein show the increased possibilities of balancing the inverter dc-link voltages as well as proper generation of the inverter output phase-leg voltages.

To compare the SVPWM algorithms (each of which has the ability to balance dc voltages), identical systems of CHB multilevel inverters were used. Also in the DABs, identical control algorithms with identical parameters of PI controllers were used. The obtained results [shown in Fig. 17(b) in the article] show that it is possible to increase the control over dc-link voltages compared to the previously presented method [Fig. 17(a)].

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