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Accurate electrothermal modelling of high frequency DC-DC converters with discrete IGBTs in PLECS software

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Abstract—In the paper, a novel, improved method of the IGBT junction temperature computations in the PLECS simulation software is presented. The developed method aims at accuracy of the junction temperature computations in PLECS by utilising a more sophisticated model of transistor losses, and by taking into account variability of transistor thermal resistance as a function of its temperature. A detailed description of the proposed method, as well as the parameter estimation procedure is given. The method is verified experimentally for the case of a DC-DC boost converter. Any discrepancies between simulations and measurements are discussed in detail. The proposed method is well suited for accurate electrothermal circuit-level simulations of power electronics converters.

Index Terms— Circuit simulation, DC-DC power converters, Insulated Gate Bipolar Transistors, Power semiconductor devices, Semiconductor device modeling, Thermal resistance

I. INTRODUCTION

IGBTs (Insulated Gate Bipolar Transistors) [1], [2] are still widely applied in power electronics converters. Discrete IGBTs are commonly used in converters of the rated power up to about 10 kVA [3].

The critical stage of converter design are software simulations. The software-of-choice for such simulations are: PLECS (Piecewise Linear Electrical Circuit Simulation) [4], PSIM [5] or SPICE (Simulation Program with Integrated Circuits Emphasis) [6].

The accuracy of simulations depends on the exactness of the applied model. To achieve the accurate results it is mandatory to use in the simulations such models of transistors which will be used in a converter. Such models are often provided by the transistor manufacturers. In [7] it was shown that although such PLECS models provide the acceptable accuracy for DC characteristics, they lead to relatively substantial errors for simulating switching losses, because of their simplified approach to this phenomenon.

From the viewpoint of a power converter design process it is

Manuscript received Month xx, 2xxx; revised Month xx, xxxx; accepted Month x, xxxx. This work was supported by the Ministry of Science and Higher Education through Program "Regionalna Inicjatywa Doskonalosci" in the years 2019–2022 under Project 006/RID/2018/19 and the sum of financing is 11 870 000 PLN.

equally important to precisely compute not only power losses, but also junction temperatures. This temperature is the key factor to estimate the lifespan of both the transistors and the whole converter [8], [9]. In case of the simulation software dedicated to power electronics, like PLECS or PSIM, the semiconductor temperatures are derived by using linear thermal models described with the Cauer or Foster networks [10]. Unfortunately, the precision of the junction temperature computations is restricted by not taking into account in thermal models the influence of this temperature on thermal conduction from the junction via the case and thermal grease to the heatsink, and thermal convection from both the heatsink surface and the transistor surface [11], [12]. As a consequence of the relations mentioned above, for discrete transistors mounted on the heatsink, the values of the Cauer network thermal resistances decrease with the junction temperature over 25% compared to the values valid for the ambient temperature [13].

In PLECS (and also in PSIM) there is no straightforward, internally implemented method to define parameters of the Cauer or Foster network as a function of the junction or ambient temperature. Therefore, it is necessary to implement a dedicated, additional algorithm to provide a better insight to heat transfer. Such an algorithm was proposed in [7] for a transistor operating for a resistive load. However, in the case of a DC-DC converter this algorithm is not sufficient, because the modifications implemented in the model of power losses are too simple.

On the other hand, the method proposed in [10] is based on the idea to perform the electro-thermal analysis in PLECS, and then to compute the temperatures in another program, which is not convenient. Moreover, the data required for these computations is not included in the regular power semiconductor datasheets.

In this paper a novel method of modelling IGBTs in PLECS that operate in power converters is proposed, which provides accurate computations of the junction temperature. In Section II the standard models of IGBTs and diodes in PLECS are described. Section III presents in detail the proposed, novel

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method of precise modelling of power semiconductors, whereas in IV the procedure of parameters estimation for the proposed model is discussed. Section V provides the experimental results which validate the exactness of the proposed model as well a discussion about its properties, pros and cons.

II. SEMICONDUCTOR DEVICES MODELS IN PLECS

In PLECS, electrical modelling is simplified. Computations of voltage or current transients of IGBTs or diodes are based on their simplified, piecewise linear characteristics defined by two parameters: forward voltage V_f , and on-resistance $R_{\rm on}$.

Transistor switching is modelled without taking into account its dynamics, with the assumption of zero switching time, and by omitting its parasitic capacitances and inductances. As a result, overvoltages and overcurrents do not occur in the computed waveforms in the PLECS software, which are important design parameters for power converters [14].

Thermal modelling in PLECS is more sophisticated, as it is based on its special "thermal library" models, and is realised in two stages. The first stage are power loss computations, and the other stage are temperatures computations based on the thermal impedance based model. The power loss calculations are based on both DC and switching characteristics of power semiconductors (IGBTs and diodes).

The conduction loss is derived on the basis of on piecewise linear interpolation of the output on-state characteristic derived from arbitrary points taken from the regular semiconductor datasheet.

As similar approach is implemented for switching loss computations. These losses, both turn-on and turn-off, are modelled as a piecewise linear interpolation of the appropriate datasheet characteristics, as a function of collector current $I_{\rm C}$, blocking voltage $V_{\rm CE}$, and junction temperature $T_{\rm j}$. PLECS allows the entry of additional, arbitrary characteristics to model losses as a function of any physical quantity, e.g.: switching loss as a function of gate resistance $R_{\rm G}$, which can be found in the datasheet. Extending the model with the influence of $R_{\rm G}$ resistance significantly reduces the computation error. In the case of the IGP06N60T transistor, within the range of resistance changes $R_{\rm G}$ specified by the manufacturer, energy losses $E_{\rm off}$ increase by 30% and energy losses $E_{\rm on}$ by 120%.

Unfortunately, this method of thermal modelling does not allow for the precise inclusion of overvoltages and overcurrents in thermal computations, related to the semiconductor switching. They cause that V_{CE} voltage turned off by the IGBT and I_{C} current turned on by this transistor can be even several dozen percent higher than it results from the computations made by the PLECS software. As a result, the values of the switch-off voltage V_{CE} and the switch-on current I_{C} computed in the PLECS software are underestimated, which causes that the computed values of E_{off} and E_{on} are also understated. This drawback, together with the impossibility to express thermal resistance as a function of the junction temperature is the main reason of a relatively low precision of the semiconductor temperature computations in PLECS [15].



To improve the exactness of the IGBT junction temperature computations in PLECS it is necessary to implement additional, dedicated algorithms. Such an algorithm was proposed in [7]. This algorithm is based on the modified method of separated iterations, the original version of which is presented in the paper [16]. However, its form is not enough to precisely compute the junction temperature of IGBTs operating in power converters with resistive-inductive loads, because it does not take into account the influence of switching-related overvoltages and overcurrents. Moreover, it does not take into account the influence of the IGBT switching frequency on the real duty cycle of the collector-emitter voltage, and in consequence it results in the underestimation of power losses in high frequency switched converters [17].

To address the shortcomings mentioned above in order to improve the exactness of the IGBT power loss computations and, at the same time, to take into account the influence of the junction and ambient temperatures on the value of $R_{\rm thj-a}$, this paper introduces and describes in detail a novel, modified algorithm (Fig. 1), which is derived on the basis of the one presented in [7]. This new method of modelling the IGBT power losses make it possible to take into account overvoltages and overcurrents, and also the influence of its switching dynamics on the real duty cycle of the collector-emitter voltage. In addition, this algorithm takes into account the load inductor series resistance, which is necessary to precisely compute the IGBT current. This resistance influences and limits the current switched by the IGBT especially for higher loads.

The first step of the proposed method is to measure the IGBT junction-ambient thermal impedance $Z_{\text{thi-a}}(t)$ for various, at least four values of its junction temperature T_i . These steady state measurements have to be repeated for the second, substantially different ambient temperature T_a . The other stage is to derive parameters of linear thermal model, based on the arbitrary characteristic $Z_{\text{thi-a}}(t)$, e.g. according to the method given in [18]. In order to simplify the computations needed for the proposed algorithm, it is advisable to use the $Z_{\text{thi-a}}(t)$ characteristic which is as close as possible to the expected the junction and ambient temperatures. In the next steps, parameters of the nonlinear thermal model have to be derived on the basis of the measured transient of $Z_{\text{thj-a}}(t)$, taking into account $R_{\text{thi-a}}$ as a nonlinear function of both junction and ambient temperatures [19]. For this purpose, in the proposed algorithm the model presented in [13] was used, which is defined by the following equation:

$$R_{thj-ai} = d_i \cdot R_{th1} \cdot (1 - a \cdot (T_a - T_0)) \cdot \exp\left(-\frac{T_j - T_a}{T_z}\right) + (1)$$

$$+ R_{th0} \cdot (1 - b \cdot (T_a - T_0))$$

In (1), d_i is the quotient of thermal resistance of i_{th} element of the heat flow path and the device thermal resistance R_{thj-a} . R_{th0} represents the minimum value of thermal resistance at the ambient temperature equal to the reference temperature T_0 . R_{th1} denotes the maximum change in the value of thermal resistance while changing the value of the device junction temperature and



 $T_a = T_0$. Coefficients a and b are the temperature rates of change in R_{th0} and R_{th1}, whereas T_z determines the slope of dependence $R_{th}(T_i)$.

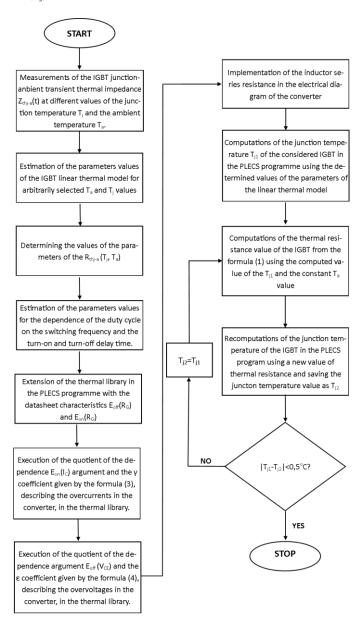


Fig. 1. Flow diagram of the developed method

Because of finite dynamics of the IGBT (different for turnon and turn-off) the duty cycle of transistor switching is not exactly equal to the duty cycle of its control signal. The difference of both quantities is a function of switching frequency, and in the range of higher switching frequencies this could lead to substantial errors in the transistor power loss computations [17]. Therefore, in the fourth step of the proposed method it is necessary to parametrise in PLECS the value of the signal duty cycle, and to make it dependent on both turn-on and turn-off delays, according to the following equation:

$$d_{equ} = d_{gen} + (t_{doff} - t_{don}) \cdot f$$
 (2)

where: d_{equ} denotes the equivalent duty cycle of transistor switching, d_{gen} – duty cycle of the control signal, t_{doff} – transistor

turn-off delay, t_{don} – transistor turn-on delay, and f – the IGBT switching frequency.

Thermal models of the IGBT in PLECS use in the default mode the switch loss function in the form of $E_{\rm on}(I_{\rm C},V_{\rm CE},T_{\rm j})$, and $E_{\rm off}(I_{\rm C},V_{\rm CE},T_{\rm j})$, whereas in the datasheet there is often additionally a dependence of $E_{\rm on}$ and $E_{\rm off}$ on the gate resistance $R_{\rm G}$. Omitting of these relations could lead to substantial computation errors [20]. For example, for a discrete IGBT of symbol IGP06N60T, for the presented in the datasheet range of $R_{\rm G}$, the value of $E_{\rm on}$ increases by 125%, and the value of $E_{\rm off}$ increases by 26% [21]. Therefore, in the fifth step it is necessary to add to the IGBT thermal model in PLECS the characteristics of $E_{\rm on}(R_{\rm G})$ i $E_{\rm off}(R_{\rm G})$ as a "Custom Tables".

In the case of an IGBT operating in a power converter there are overcurrents during a turn-off process. As a result, the equivalent switching current during this state is higher than the one expected for an ideal, lossless transistor [14], [22]. In the classic circuit simulation program - SPICE, overcurrents and overvoltages can be modelled by adding in the analyzed system L and C components representing parasitic capacitances and inductances of semiconductor devices as well as the inductances of cables and traces. Unfortunately, the time needed to perform such electrothermal simulations of the DC-DC converter is even 1 day. On the other hand, in the PLECS software it is impossible to take into account overvoltages and overcurrents in this manner, because the transistor voltage and current waveforms are discontinuous, therefore the introduction of L and C components representing the parasitic properties of the converter components makes it impossible to obtain the convergence of the computations.

A possible solution that enable taking into account this phenomenon and its influence on E_{on} in the PLECS software is to substitute in the thermal model the values of collector current I_C with the values of the quotient of this current and the factor γ , whose value is calculated according to the following equation:

$$\gamma = \frac{I_{Conreal}}{I_{Conideal}} \tag{3}$$

where: $I_{\rm Conreal}$ is a IGBT turn-on current for a half of the maximum converter load, and $I_{\rm Conideal}$ is the turn-on current derived for an ideal transistor and the same point of the converter operation. The appropriate equations for calculations of $I_{\rm Conideal}$ for various converter topologies are given e.g. in [22]. $I_{\rm Conreal}$ can be determined experimentally by measuring the maximum value of the switched on current or by performing computer simulations in the SPICE program using models of the semiconductor devices.

In the case of turning-off the transistor, the substantial influence on $E_{\rm off}$ have voltage overshoots, which increase the voltage that is blocked during the switching process. A possible solution that enables taking into account this phenomenon and its influence on $E_{\rm off}$ is to substitute in the thermal model the values of the voltage $V_{\rm CE}$ with the values of the quotient of this voltage and the factor ε , whose value is calculated according to the following equation:



$$\varepsilon = \frac{V_{CEoffreal}}{V_{CEoffideal}} \tag{4}$$

where: $V_{\text{CEoffreal}}$ is the IGBT turn-off voltage for a half of maximum converter load, and $V_{\text{CEoffideal}}$ is the a turn-off voltage derived for an ideal transistor and the same point of converter operation. As in the case of a turn-on process, the appropriate equations for various converter topologies are given e.g. in [22]. $V_{\text{CEoffreal}}$ can be determined experimentally by measuring the maximum value of the switched off voltage V_{CE} or by performing computer simulations in the SPICE program using models of the used semiconductor devices and taking into account parasitic inductances of cables and traces.

The last step of preparing the proposed model of the IGBT operating in a power converter is to take into account in this model series resistance of inductors.

In the next, ninth step it is necessary to perform the PLECS simulations with the linear model of parameters derived in the second step described above. The computed junction temperature is then denoted with T_{i1} .

In the tenth step it is necessary to compute once more the junction temperature, taking into account thermal resistances of the Cauer network derived on the basis of (1) for T_j equal to T_{j1} . The computed junction temperature is then denoted with T_{i2} .

The computations have to be repeated until the difference between T_{j1} and T_{j2} is within the assumed, allowed error, equal to e.g. 0.5° C.

IV. PARAMETERS ESTIMATION OF THERMAL MODELS

In order to use this model it is necessary to estimate its parameters. For the electrical part of the model the parameter estimation was carried out for a case of a DC-DC boost converter. It was decided to carry out an experimental verification of the developed method for the converter output voltages not exceeding 400 V and the switched currents with instantaneous values not exceeding 10 A. Therefore IGBTs were chosen to IGP06N60T, and diodes to IDP08E65D1. The transistor is of 600 V, 6 A class. The selected diode is characterised by the maximum voltage equal to 650 V, and the rated current equal to 8 A. Both semiconductors are packaged in the TO-220 case. The derived parameters of the electrical model in PLECS are given in Table I.

TABLE I
Parameters values of electrical models of the IGBT and the diode

diode							
	IGBT		Diode				
	$V_{\rm f}[V]$	$R_{on} [\Omega]$	$V_{\rm f}[V]$	$R_{on} [\Omega]$			
	0.89	0.106	1.01	0.05			

In order to compute the junction temperature of a power semiconductor in PLECS in is necessary to define its thermal model in a dedicated thermal library. Many semiconductor manufacturers provide such a PLECS model on their website. The thermal model of the selected IGBT has been downloaded from the website of its manufacturer – Infineon Technologies

[23]. The PLECS thermal models of any semiconductor can be also prepared based on the appropriate datasheet.

Computations of the semiconductor junction temperature require parameters of a lumped-element thermal model of heat distribution from junction to ambient. In order to derive parameters of such a model in the form of the Cauer net, measurements of the junction-ambient thermal impedance transients are performed for a transistor with finned heatsink of the following physical dimensions: 75 mm x 50 mm x 35 mm.

These measurements were mode with the use of the measuring system presented in [24]. This circuit enables the implementation of an indirect electrical method for measuring thermal impedance $Z_{thj-a}(t)$. In the next step, the parameters of a linear model are calculated for the junction temperature equal to 120°C, and by using all the measurements of $Z_{thj-a}(t)$ – the parameters of a nonlinear thermal model. The parameters of the linear thermal model are given in Table II, whereas parameters of the nonlinear model derived according to method given in [11] – in Table III. The measured transient thermal impedance $Z_{thj-a}(t)$, together with the results of calculations for both thermal models are shown in Fig. 2.

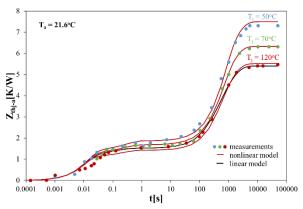


Fig. 2. Measured and computed waveforms of the transient thermal impedance $Z_{\text{thi-a}}\!(t)$

As shown in Fig. 2, the linear thermal model provides a good agreement between the results of computations and measurements for only one value of the junction temperature of the component, because this model does not take into account the dependence $R_{\text{thj-a}}(T_i)$. For the presented junction temperature range, the linear model causes an error of computations of thermal resistance $R_{\text{thj-a}}$, reaching as much as 25% for T_i =50°C. Such a big error value has a key impact on the accuracy of IGBT the junction temperature computations, which shows that it is necessary to use a nonlinear thermal model, for which the results are of much better accuracy – the relative error does not exceed 3%. For the considered nonlinear thermal model for one value of temperature T_i the value of thermal resistance $R_{\text{thj-a}}$ computed using this model is equal to the value computed using the linear model. In the considered case, this can be seen for $T_i = 120^{\circ}$ C and it is the reason why the red line and the black line overlap.

TABLE II

Parameters values of a linear thermal model of the discrete IGBT placed on the heatsink

	IGBT
R _{th1} [K/W]	1.282
R _{th2} [K/W]	0.239
R _{th3} [K/W]	3.047
R _{th4} [K/W]	0.8374
C _{th1} [mJ/K]	9.316
C _{th2} [mJ/K]	594.9
C _{th3} [J/K]	141
C _{th4} [J/K]	1086

TABLE III
Parameters values of nonlinear thermal model of the discrete IGBT placed on the heatsink

	IGBT
$R_{th1}[K/W]$	6.3
$R_{th0} [K/W]$	5.55
$T_{Z}[K]$	26
$T_0[K]$	300
a	0.0056
b	-0.0057
d_1	0.1372
d_2	0.0442
d_3	0.6637
d_4	0.1549
C _{th1} [mJ/K]	9.316
C_{th2} [mJ/K]	594.9
C_{th3} [J/K]	141
C_{th4} [J/K]	1086

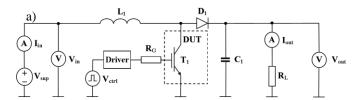
The values of factors γ and ϵ which are present in the equations (3) and (4) are strictly related to the construction of particular converter, because both overcurrents and ovevoltages are a result of parasitic capacitances and inductances of the circuit, in particular of its elements, wires and the PCB paths layout [22]. In order to precisely derive its values it is necessary to measure the maximum values of current during the semiconductor turn-on process, and the maximum voltage during turn-off process, and then to calculate the parameters according to (3) and (4). For the particular experimental model of a boost converter, for which the results are presented in the paper, the values of appropriate factor are equal to: $\gamma = 1.5$, and $\varepsilon = 1.25$. The values of these parameters can also be determined using the SPICE program. For this purpose, simulations of the analysed system should be carried out, taking into account the inductance of cables and trace of the designed converter [24] and using the models of semiconductor devices used in the designed converter.

V. EXPERIMENTAL VERIFICATION

In order to verify the correctness of the computations of the IGBT junction temperature in PLECS, measurements of this component are carried out using the measurement set-up whose diagram is shown in Fig. 3a, and its photo in Fig. 3b.

In the presented measurement set-up, source V_{sup} is used to power supply the converter. This voltage is provided by power supply PSB-2800L by GW Instek. The switching signal is

provided by the function generator $V_{\rm ctrl}$, which is connected through the driver IR2125 and resistor $R_{\rm G}$ to the gate of the transistor (DUT). Resistor $R_{\rm G}$ limits the maximum current of the transistor gate. As a source of the control signal the function generator NDN JC5603P is used. The temperature of the transistor case is measured by means of the infrared thermometer PT-3S by Optex. The driver IR2125 has the maximum output current equal to 1 A and the maximum output voltage of 18 V. As a voltmeters and ammeters Rigol DM3058E multimeters are used. Values of RLC components are presented in Table IV.



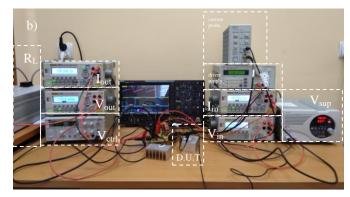


Fig. 3. Diagram of the measurement set-up dedicated to measure characteristics of the boost converter

TABLE IV
Values of RLC components occurring in the converter

,	Addes of NEC components occurring in the converter				
	$R_G[\Omega]$	L ₁ [μH]	C ₁ [μF]		
	100	460	330		

In order to measure the junction temperature without opening the IGBT cap, its cap temperature T_c is measured optically. Then the value of the junction temperature is calculated from the formula (5).

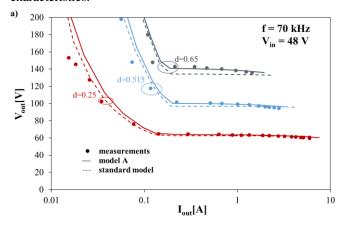
In order to calculate T_j , R_{thj-a} is measured using the method presented in [25]. On the other hand, R_{thj-c} is measured using measured T_j temperature using indirect electrical method and the optically measured T_c temperature in thermally steady state. The calculations of temperature T_j are made using the formula [7]:

$$T_{j} = T_{c} + \left(T_{c} - T_{a}\right) \cdot \frac{R_{thj-c}}{R_{thj-a} - R_{thj-c}} \tag{5}$$

In Fig. 4-6, the solid line marks the results of computations obtained using the model formulated using the new method (model A), the dashed line – the results of computations in PLECS obtained using the model from [23] (Standard Model), and the points - the results of measurements.



In Fig. 4a are shown the characteristics of the constructed DC-DC boost converter, and in Fig. 4b –junction temperatures as a function of the output current, which correspond to these characteristics



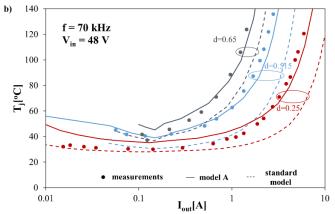


Fig. 4. The output characteristics of the DC-DC boost converter (a) and corresponding IGBT junction temperature (b) as a function of the converter output current.

As can been seen from Fig. 4a, the proposed model A, in the contrary to the standard model, provides the results which are almost identical to the measurements. The main reason of errors of standard model is neglecting in this model the influence of turn-on and turn-off dynamics on the real duty cycle of collector-emitter voltage. For model A, a slight inaccuracy is only for very low values of the output current.

It is clear from Fig. 4b, that only for the proposed, novel method of modelling an IGBT in PLECS it is possible to obtain high accuracy of the transistor junction temperature computation in a wide range of both the duty cycle and the output current. The standard model, because of its oversimplification, provides the substantially worse accuracy. For this model, the errors exceeds even 80°C.

In Fig. 5a, the output voltage of the DC-DC boost converter as a function of control signal duty cycle is shown, for two values of input voltage, whereas in Fig. 5b – corresponding IGBT junction temperature is shown.

As it can be seen from Fig. 5a, both the considered models make it possible to obtain the good accuracy of determining the dependence $V_{\rm out}(d)$. The difference between the computed values of the output voltage results from taking into account in

the new method influence of electrical inertia on duty cycle of the collector-emitter voltage and, consequently, the output voltage of the converter. In turn, the better accuracy of the junction temperature computations obtained with the use of the new method results from taking into account the influence of currents and voltages overshoots in this model and thanks to the correct determination of the duty cycle of the collector-emitter voltage.

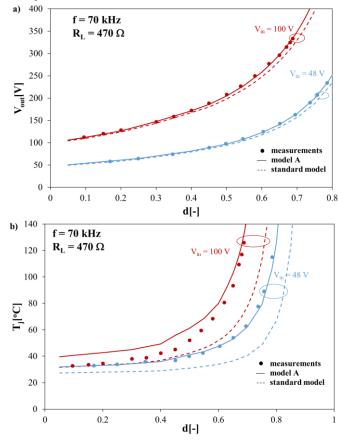


Fig. 5. The output voltage of the DC-DC boost converter (a) and corresponding IGBT junction temperature (b) as a function of the control signal duty cycle

Due to the above mentioned phenomena in the new method, the error in determining the junction temperature does not exceed 10°C. For comparison, for the model implemented in the PLECS program, it is even 50°C.

In Fig. 6a there is shown the DC-DC boost converter output voltage as a function of switching frequency, for a two values of the control signal duty cycle, and in Fig. 6b – the corresponding IGBT junction temperature.

Similarly to the measurements and the model based calculation results depicted in Fig. 4 and 5, also from the characteristics shown in Fig. 6 it is clear, that model A provides the considerably better accuracy than the standard model. The lower accuracy for the standard model for the characteristics from Fig. 6a is mainly the result of not taking into account the real duty cycle of IGBT collector-emitter voltage. For this model, the difference between the measurements and the results of computations increases with an increase of switching frequency. The similar trend can be observed from the junction

temperature characteristics, because of simplifications in the loss computation method in the standard model.

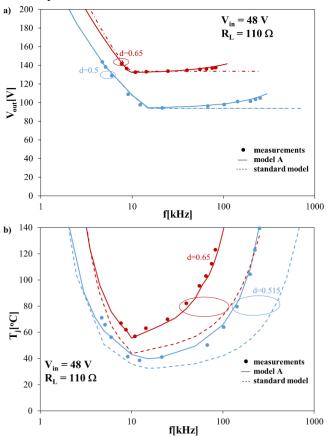


Fig. 6. The output voltage of the DC-DC boost converter (a) and corresponding IGBT junction temperature (b) as a function of switching frequency

The important, additional advantage of the proposed method of the IGBT thermal modelling in PLECS is a relatively short computation time.

For the considered converter and operating conditions, duration of such computations for manual changes of parameters of the thermal model in subsequent iterations of the developed algorithm in PLECS does not exceed 5 minutes for PCs with Intel i7 class processors. For the dedicated application, which does it automatically, the required time would be shortened to less than a minute.

VI. CONCLUSIONS

In the paper the analysis of an influence of selected factors on the accuracy of the IGBT junction temperature calculation in PLECS was presented, and the novel method of its thermal modelling in PLECS was proposed, described in detail and verified experimentally. Additionally, the proposed method was compared to the standard approach for a thermal model of an IGBT in PLECS. The results are discussed in detail.

The important advantage of the proposed method is the possibility to use the parameters from a standard IGBT datasheet as the input parameters for computations. The only data, which is required for computations, and is not present in

the datasheet is the one which is specific for a particular design of the power converter.

It was proved, that the simplified, standard modelling of the IGBT switching power loss, and the methods which do not take into account the dependence of thermal resistance on the semiconductor junction temperature lead to substantial errors in the computed thermal quantities. It is particularly important to take into account in the thermal model the influence of overvoltages and overcurrents, as well to derive the real duty cycle of the collector-emitter voltage based on the control signal. To maximise the exactness of the IGBT junction temperature, the separated iterations method was proposed and implemented.

The proposed method of the IGBT modelling in PLECS provides very substantial improvement of the computation exactness at the expense of a very slight increase of the required computation effort. This method provides the IGBT junction temperature computation exactness, for junction temperature above 40°C, with errors of computations of the junction temperature increase not greater in any case than 7%, and the results are computed even within 1 minute. The junction temperature increase computation error of the PLECS based IGBT thermal model from [23] for the same point of operation can be, in comparison, as high as 80%.

The proposed in the paper novel method of the IGBT modeling in PLECS can be useful for designers of power electronics converters, allowing them to substantially improve the thermal computations accuracy even at the early design stages, and thus shortening the whole converter design process. It can be useful in particular to design a converter cooling system and to estimate the exact power limits for its various operating conditions.

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