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A Simplified SVPWM Technique for Five-leg Inverter with Dual Three-phase Output

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***Abstract*—This article proposes a simplified space vector pulse-width modulation (SVPWM) technique five-leg i nverter with dual three-phase output. An idea to fed the dual tree-phase machine by the multiphase voltage source inverters (VSIs) is not new. Dual- and multi-motor drive systems are widely used in the industry applications. The most popular fields a re: electric vehicles (EVs) and traction systems. Moreover, the specific characteristic of the dual-drive systems allow to use them in the paper and textile production process. Mostly these solutions utilize carrier-based PWM (CBPWM) techniques for the output voltage generation, however the SVPWM techniques might be also used for this purpose. The main idea of this paper is to simplify the modulation process and obtain the similar algorithms complexity and execution times for the space-vector and carrier-based PWM techniques. The proposed SVPWM strategy allows to decrease the number of calculations at the initial stage of the algorithm. The output voltages for both loads/motors can be generated independently, with different frequencies and amplitudes. Simulation results were obtained using the PLECS software package. The experimental investigation with RL load were conducted as well. The carried tests proved the effectiveness of the proposed modulation strategy. All results are shown in this paper.**

***Index Terms*—space vector pulse width modulation, five-phase power converters, dual three-phase drives, machine control**

I. Introduction

Two decades back the multiphase drive systems have became a one of most popular research topic. Since that time several control schemes and modulation techniques were presented. In work [1] the possibility of the independent control of the dual three-phase drive was discussed and a novel control strategy was presented. Future works [2]–[8] were focused on the improving of the control schemes and PWM techniques. The paper [2] proposed the modified control technique to increase the voltage utility factor (VUF). Initially, the VUF value not exceed the half of the dc-link, or 50%, however, with modification authors o btain a n i mprovement to 86.6% [2]. Nevertheless, both motors should operate with the similar frequencies; this is a limitation of this control method. The papers [3] shown the research problems of the dual three-phase drives in terms of the dc-link voltage utilization and the common-phase current amplitude increasing. The SVPWM implementation issues were discussed in [4], where the standardized modulation blocks were proposed and the problem with algorithm implementation was partially solved. The modulation algorithm for five-leg VSI was proposed in [5], the switching pattern of this PWM is symmetrical for both motors, so the switching frequency is the same for each leg. The comparison between different topologies, where dual three-phase machines can be supplied by one inverter was done in [6]. The three main types of the topologies were depicted: with additional leg, with common neutral point, and with shared/common-leg. Analysis provided in [6] proves the superior of the common-leg inverter topology. The performance comparison of different PWM techniques was done in [7]. The dc-link voltage distribution between machines, tha harmonic content and the complexity of the implementation were the main topics in that research. Authors recommended double zero-sequence injection method as the best due to the comparison studies. The paper [8] proposed the general modulation technique to control n three-phase motors from VSI with the $(2n + 1)$ legs. The appropriate PWM strategy was proposed as well.

During the past decade, the different control system were presented, [9]–[11]. The simple direct torque control (DTC) was proposed in [9]. The work [10] shown the torque and flux ripples and proposed a solution – fuzzy stator resistance estimator, implemented to decrease these ripples. The complex sensorless control strategy with model reference adaptive control (MRAC) was introduced in [11]. Future investigation allowed authors to obtain the experimental results and shown the behavior of dual permanent magnet synchronous motor (PMSM) drive system, [12]. Not only control and modulation strategies were under investigation. The several topologies, where the idea of the common-phase utilization exists, were presented in [13], [14]. The model predictive control (MPC) methodology as well as hysteresis current control were used

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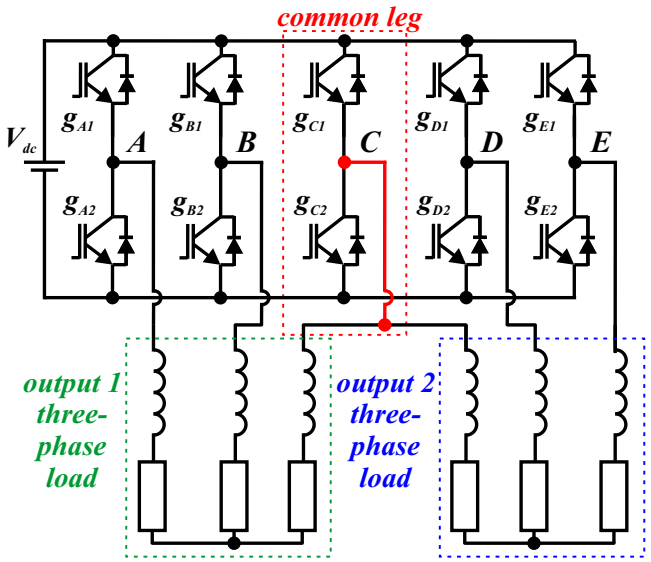

Fig. 1. The power circuit of the five-leg inverter with dual three-phase output.

for dual-motor drive system with five-leg VSI in [15] and [16], respectively.

The last years this research topic still actual and different papers were published, [17], [18]. The complex priority-based MPC technique was proposed in [17]. This technique allows to obtain a lower current ripples and shorter computation time compare to the conventional MPC methods. However, the complexity of the algorithm is still higher than for CBPWM and SVPWM. The modified SVPWM algorithm was proposed in [18]. The main advantage of this purpose is the speed range expending, when one motor operate with low speed. This effect can be achieved by the modification of the resulting switching pattern, when the duration of the active vectors increased. The idea of the switching pattern modification is not new, however, previously this approach was used for multiphase drive systems.

This paper presents the simplified SVPWM technique for a five-leg inverter with dual three-phase output. The main contribution is to shown the possibility of the switching pattern modification and the computation complexity reduction. This reduction can be obtain by the decreasing of the initial calculation. The similar approach was proposed for multiphase inverters in [19]. However, it is a first attempt to implement such simplification to the SVPWM strategy for the five-leg inverter with dual three-phase output.

This paper consist of the sections: the simplified SVPWM technique description in section II, the simulation and experimental results are shown in section III, and the conclusion is given in Section IV.

II. Proposed SVPWM technique

The five-leg inverter with one common-leg can be utilized for two three-phase loads, Fig 1. the conventional SVPWM techniques considered two three-phase space vector diagrams, Fig 2. These modulation strategies provide calculations for

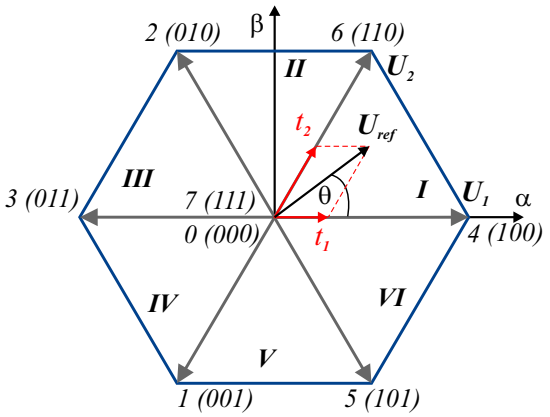

Fig. 2. The space-vector placement for three-phase load.

both motors independently at all steps of the algorithm execution. The proposed SVPWM technique propose simplification at the initial stage, when the whole modulation strategy can be described as below.

The initial calculations should be done only once, and their results will be stored in memory. First stage of the algorithm is to select two vectors and use both of them for each loads. Well known that active vectors duration t_1, t_2 should fulfill the condition:

$$U_{dc} \cdot U \cdot T = T_s \cdot U_{ref} \tag{1}$$

where U_{dc} is a dc-link voltage, T_s – switching period, U_{ref} is matrix containing the reference vector components, and U – matrix consisting normalized coefficients, [19]:

$$U = \begin{bmatrix} Ux_1 & Ux_2 \\ Uy_1 & Uy_2 \end{bmatrix} \tag{2}$$

$$T = \begin{bmatrix} t_1 \\ t_2 \end{bmatrix}; U_{ref} = \begin{bmatrix} Ux_{ref} \\ Uy_{ref} \end{bmatrix}; \tag{3}$$

Taking into account the presented dependencies, the active vectors duration t_1, t_2 can be calculated as follows:

$$T = \frac{U_{ref}}{U_{dc}} \cdot T_s \cdot U^{-1}. \tag{4}$$

In the proposed approach only the (3) are recalculated at each execution cycle. The other components from (4), T_s and U^{-1}, can be easily predefined and calculated once. This way, the sector identification procedure is redundant here. Moreover, for dual-drive systems all calculations need to be done twice, for both motors. This modulation method allows to use one set of the preselected values for both motors.

After the initialization, the next step is to consider five-phase inverter as two independent three-phase systems, and define the times for both outputs, as:

$$\begin{aligned} &if(g^i_{n1} == 1) \quad t^{up}_{ni} = t^i_1; \quad else: \quad t^{low}_{ni} = t^i_1; \\ &if(g^i_{n2} == 1) \quad t^{up}_{ni} += t^i_2; \quad else: \quad t^{low}_{ni} += t^i_2; \end{aligned} \tag{5}$$

where n is a phase/leg number (a,b,c), i is a output number (load 1 or 2), g^i_{n1}, g^i_{n1} – gates in each leg, Fig. 1, indexes up and low – ON and OFF states of the transistor. Than, those times should be combined. In five-phase inverter with one common-leg, to obtain the corresponding activation times zero component should be introduced to the switching sequence as:

$$\begin{aligned} t^{up}_x &= t^{up}_{n1} + t^{up}_{common\ 2}; \\ t^{low}_x &= t^{low}_{n1} + t^{low}_{common\ 2}; \\ t^{up}_{com} &= t^{up}_{common\ 1} + t^{up}_{common\ 2}; \\ t^{low}_{com} &= t^{low}_{common\ 1} + t^{low}_{common\ 2}; \\ t^{up}_y &= t^{low}_{n2} + t^{up}_{common\ 1}; \\ t^{low}_y &= t^{low}_{n2} + t^{low}_{common\ 1}; \end{aligned} \tag{6}$$

where x and y is a phase number dedicated to the firs and second load, respectively, com - is a number of the common leg. In fig. 1: x – "A" and "B", y – "D" and "E", com – "C".

To reduce the losses the optimization pattern was implemented. The activation times of the zero vectors (000 and 111) can be reduced by following procedure. The minimal duration of the ON and OFF state, should be found:

$$\begin{aligned} min^{up} = t^{up}_A \quad if(min^{up} > t^{up}_n) \quad min^{up} = t^{up}_n; \\ min^{low} = t^{low}_A \quad if(min^{low} > t^{low}_n) \quad min^{low} = t^{low}_n; \end{aligned} \tag{7}$$

The minimal values are exist in the each phase, so it we can provide the following modification:

$$t^{up}_n = t^{up}_n - min^{up};\ t^{low}_n = t^{low}_n - min^{low}; \tag{8}$$

Without the optimization procedure presented above proposed SVPWM technique can generate negative times, however, at this step all times are greater or equal to zero. Nevertheless, the duration of the obtained times should be verified in terms of the switching period T_s. These times should be shorter or equal T_s, for this the following calculation should be done:

$$\begin{aligned} max^{time} = t^{up}_A + t^{low}_A; \\ if(max^{time} > T_s);\ t^{up}_n = \tfrac{T_s}{max^{time}};\ t^{low}_n = \tfrac{T_s}{max^{time}}; \end{aligned} \tag{9}$$

From this stage modulation algorithm is ready to generate the output voltages correctly. Nevertheless, the additional part, with optimization procedure proposed in [19] was implemented here. By zero vectors introduction into the switching sequence the resulting pattern will activate only one gate at each leg in one switching cycle. The duration of this vectors is define as:

$$t_0 = 0.5 \cdot (T_s - max^{time}); \tag{10}$$

The (10) modify the previously calculated times, as:

$$t^{up}_n += t_0;\ t^{low}_n += t_0;; \tag{11}$$

After this final step, the resulting switching sequence is created.

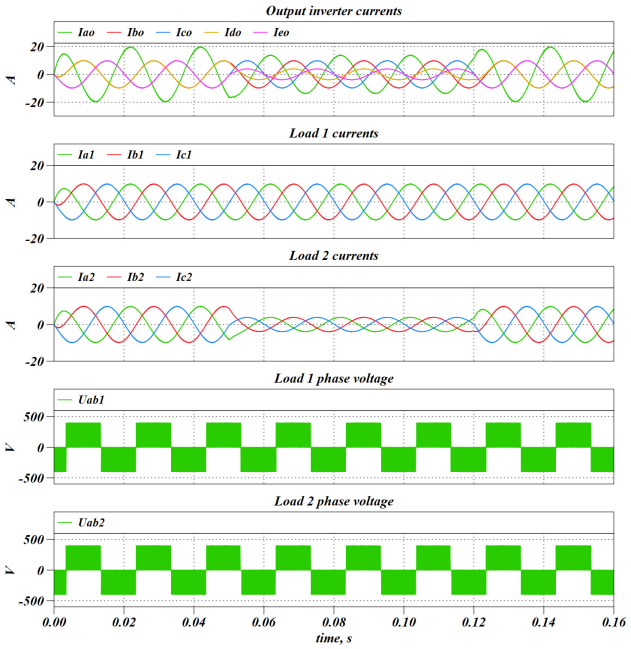

Fig. 3. The dynamic system response under the step change in the reference output voltage. Output inverter currents, loads currents and phase voltages.

III. Simulation and Experimental Studies

A. Simulation results

The simulation results were obtained utilizing the PLECS software package. The effectiveness of the proposed modulation algorithm was verified. The system behavior for different frequencies and length of the reference voltage vector was presented as well. During the simulation studies the parameters of the first and second RL loads were define: $R_1 = R_2 = 10\Omega$ and $L_1 = L_2 = 20mH$, the indexes 1 and 2 shown the 1^{st} and 2^{nd} loads, respectively. The dc-link voltage was set as $U_{dc} = 400V$. Obtained data were given in Fig. 3 and Fig. 4, where the output inverter currents, phase currents and voltage for the 1^{st} and 2^{nd} loads were shown.

At the moment $0.05s$, indicated in the Fig. 3, a step change on the reference voltage vector amplitude, U_{ref}, occurs for the load 2. As can be mentioned from figure, the amplitude of the output currents changed and all five-leg currents waveform can be easily analyzed. At the moment $0.12s$ the reference value was changed back.

Previously shown results was obtained for the same frequencies for both loads and without any delay in angle Θ between them. Fig. 4 shows the system dynamic response for the step change in angle Θ; at the moment $0.2s$ the angle difference was set as 180 degree. The current amplitude in the common-leg is equal to zero, when the $U^1_{ref} = U^2_{ref}$, and depends on the amplitudes difference. The general rule is the current amplitude in the common-leg is equal to the current for the 1^{st} and 2^{nd} loads.

Previously shown results was obtained for the same frequencies for both loads and without any delay in angle Θ between them. Fig. 4 shows the system dynamic response for

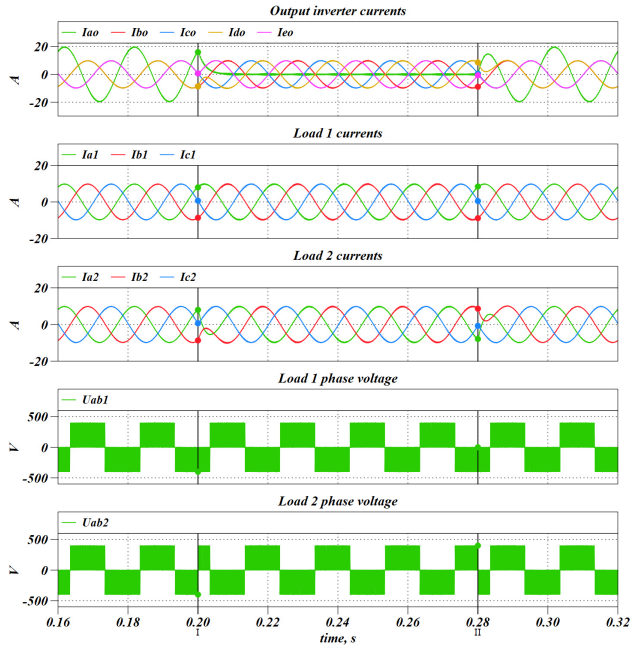

Fig. 4. The dynamic system response under the step change in the angle between two loads. Output inverter currents, loads currents and phase voltages.

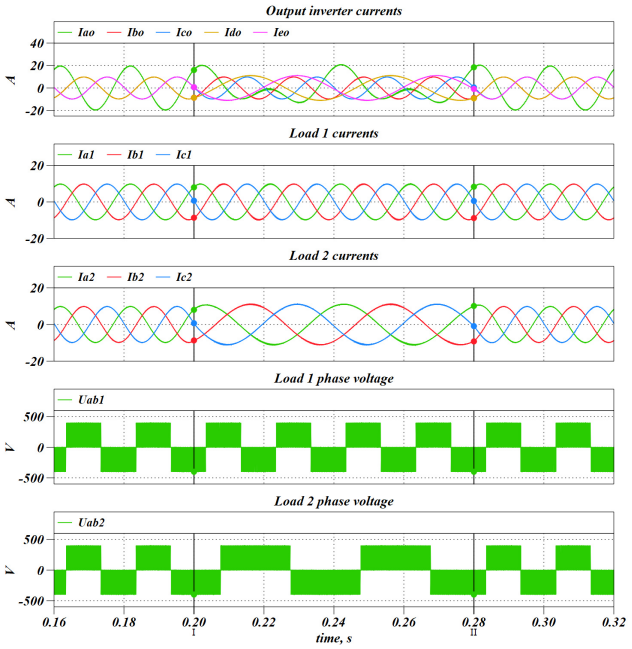

Fig. 5. The dynamic system response under the step change in the frequency of the second load. Output inverter currents, loads currents and phase voltages.

the step change in angle Θ; at the moment $0.2s$ the angle difference was set as 180 degree. The current amplitude in the common-leg is equal to zero, when the $U^1_{ref} = U^2_{ref}$, and depends on the amplitudes difference. The general rule is that the current amplitude in the common-leg is equal to the sum of the currents for the 1^{st} and 2^{nd} loads.

Fig. 5 shows the step change on the frequency value. With different frequencies the common phase current can not be easily reduced, and should be analyzed separately.

B. Experimental results

The experimental tests were conducted using the five-phase prototype inverter, Fig 6. This inverter uses the DSP processor (ADSP21263) for control and modulation algorithms execution, and the FPGA Altera Cyclone II board for control of the AC/DC converters and the other peripherals. The RL loads were used during the experimental studies. The loads parameters are $R_1 = R_2 = 10\Omega$ and $L_1 = L_2 = 20mH$, the indexes 1 and 2 shown the 1^{st} and 2^{nd} loads, respectively. The dc-link voltage was define as $U_{dc} = 400V$. All parameters were chosen so as to replicate the results of the simulation studies.

The improvement in the execution time of the SVPWM modulation strategy is shown in Table I. The calculation of the simplified algorithm initialization part takes $0.22\mu s$, this operation need to be only once. The modulation strategies require $1.95\mu s$ and $3.37\mu s$ of the processor time for the proposed and conventional SVPWMs, respectively. The proposed, simplified SVPWM allows to achieve a total improvement of 42% in the execution time.

Fig. 7 shows the system behaviors under step change of the reference voltage amplitude (a), the angle difference (b), and

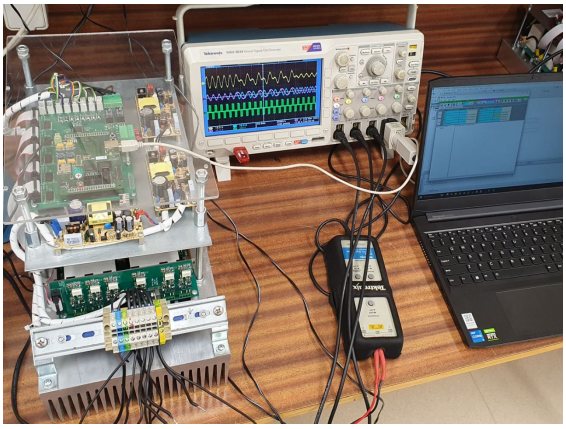

Fig. 6. Five-phase voltage source inverter, laboratory prototype.

the frequency value (c) for one of the load. During the studies same frequency value was set for both loads, and the amplitude of the current in the common-leg is sum of the loads phase currents. Fig. 7 (a) proves that modulation algorithm allows to operate with different reference voltage amplitudes. In Fig. 7 (b) the angle between loads was set to π, so the common-leg current decrease to zero. Such characteristic allows to decrease

TABLE I
SVPWMs Execution time

Modulation technique	Execution time	
	Modulation procedure	*Initialization*[a]
Proposed SVPWM	$1.95\mu s$	$0.22\mu s$
Conventional SVPWM	$3.37\mu s$	0

[a]Calculated only once.

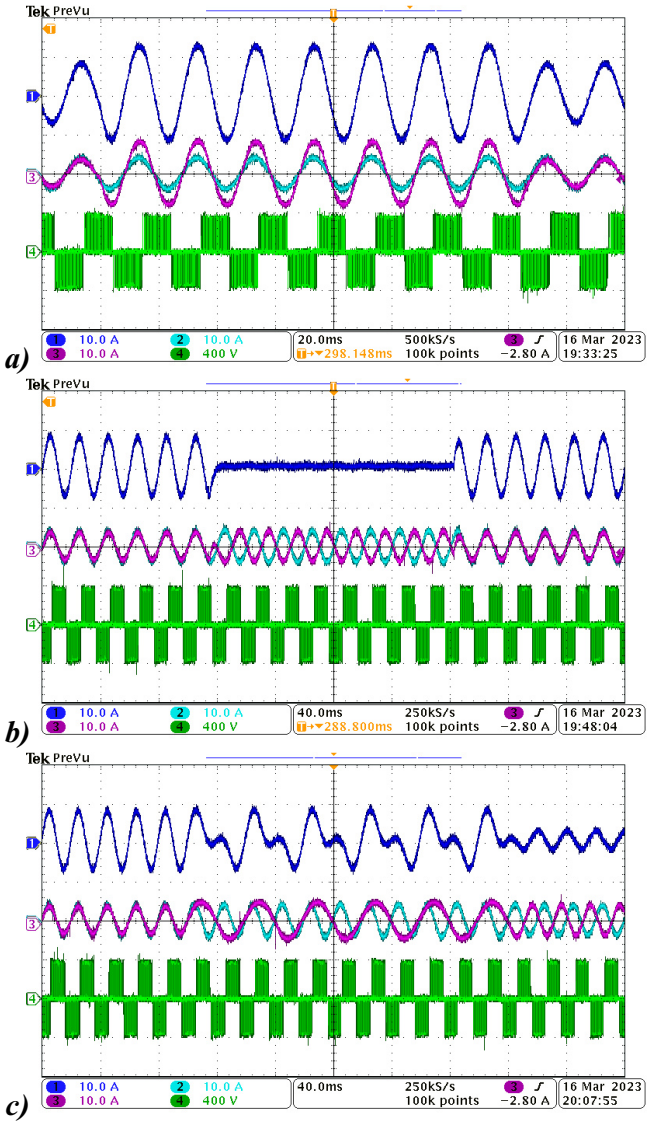

Fig. 7. The dynamic system response under the step change in: (a) the reference output voltage; (b) angle between two loads; (c) frequency of the second load. Output inverter currents, loads currents and phase voltage.

the inverter conduction losses up to 20%. Results of various frequencies operation are shown in Fig. 7 (c). The common-leg current waveform consists of harmonics for both loads, however, the shape of loads currents stayed unchanged. After the step back change of the load frequency, we can not control the angle difference, so the amplitude of the common-phase current will be uncontrolled.

The THD analysis are shown in Fig 8. For the same loads frequency the obtained THD values of common-leg current are 0.885% and 0.890% for the proposed and conventional SVPWM, respectively. At the same moment, the THD values of the loads phase current are 2.12% and 2.18%. Provided comparison tests shown that proposed SVPWM technique has the similar characteristics, THD and dc-link voltage utilization, as classical SVPWM techniques.

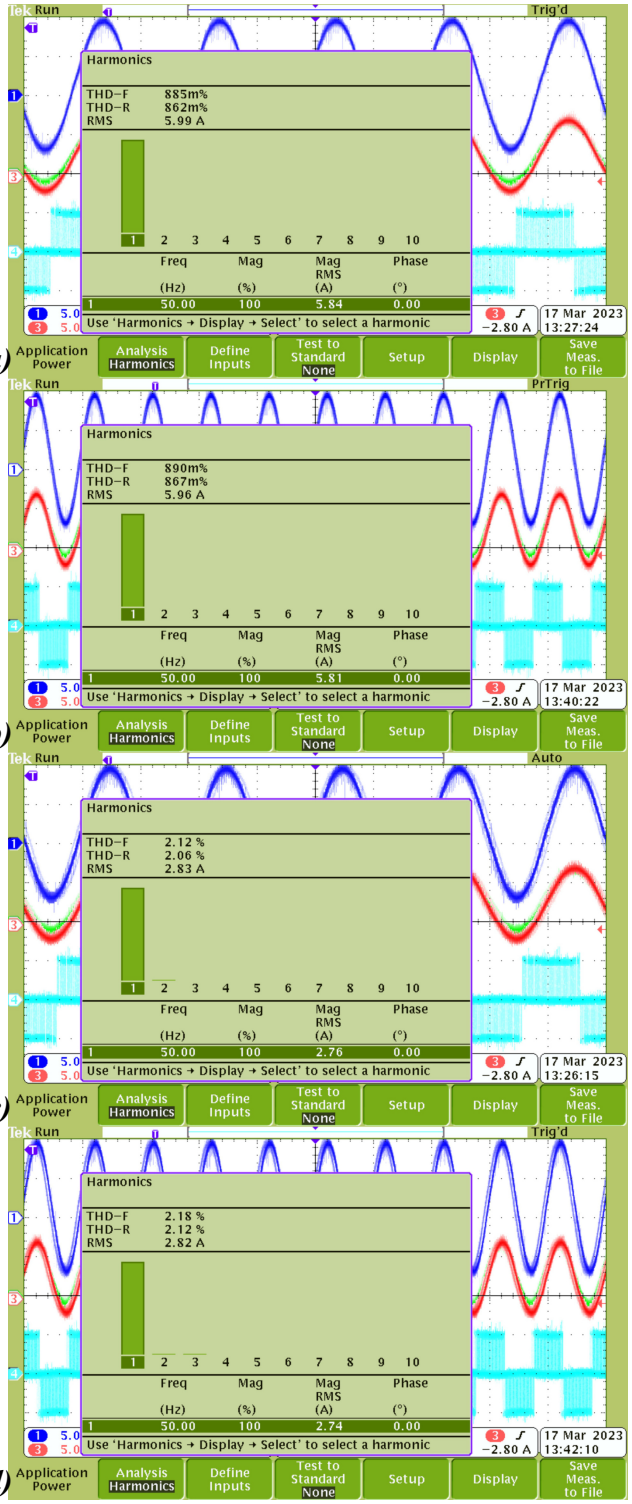

Fig. 8. The FFT analysis of: the common-phase current (a) proposed SVPWM; (b) classic SVPWM; and the output load currents (c) proposed; (d) classic modulation methods.

The main difference between the proposed and conventional techniques is a reduced execution time, as shown in Table I. The shorter time was achieved by the simplification at the initial part of the modulation algorithm. Simultaneously, the

currents across the switches are the same for each modulation technique and the THD values are relatively equal, as shown in Table II. These characteristics follow the nature of the proposed SVPWM, where the resulting switching patterns are the same for both methods.

TABLE II
SVPWMs THD COMPARISON

Modulation technique	THD value	
	Common-leg	*Individual output leg*
Proposed SVPWM	0.885%	2.12%
Conventional SVPWM	0.890%	2.18%

IV. CONCLUSION

The experimental studies proved the effectiveness of the proposed modulation strategy. Comparing with the conventional SVPWM method, shown that both approaches have the similar performance in THD and dc-link voltage utilization. The proposed SVPWM technique offers the large improvement, 42% in the processor usage time. The simplification of the initial stage, proposed here, make the simplified SVPWM much more attractive for usage in industry applications. The modulation method allows to remove the unnecessary part with the reference voltage vector position identification at the each execution of the modulation algorithm. The five-leg inverter, with dual three-phase output, offers a several possibilities in control, e.i. losses reducing, and control scheme complexity decreasing. All of these, make the dual drive systems interesting research topic for future investigations. The proposed SVPWM should be considered as main counterpart to the existing PWM methods.

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