

# A 0.5 V Nanowatt Biquadratic Low-Pass Filter with Tunable Quality Factor for Electronic Cochlea Applications

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**Abstract:** A novel implementation of an analogue low-power, second-order, low-pass filter with tunable quality factor ( $Q$ ) is presented and discussed. The filter feature is a relatively simple, buffer-based, circuit network consisting of eleven transistors operating in a subthreshold region.  $Q$  tuning is accomplished by injecting direct current into a network node, which changes the output resistance of the transistors and, as a result, modifies the filter network's loss, and thus its  $Q$ .  $Q$  tuning is independent of a filter cut-off frequency ( $\omega_0$ ). The filter, with a nominal  $\omega_0$  of 1 kHz, was fabricated using a 0.18  $\mu\text{m}$  CMOS technology, and features a  $Q$  range of 2–11, power consumption of up to 52 nW, and a 59 dB dynamic range when using a 0.5 V supply. The  $\omega_0$  can be tuned from 0.5 to 2.5 kHz using a traditional method by changing the transistor transconductances, but this process partially affects the quality factor.

**Keywords:** analogue filters; low frequency filters; audio filters; low power circuits; analogue integrated circuits; CMOS analogue circuits; electronic cochlea; energy efficient analogue filters



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## 1. Introduction

One important functional block that is a part of hearing aids [1–6] as well as devices for human voice recognition [7], are tunable filters [8–11] that emulate characteristics of a human cochlea. Such filters allow pre-processing of acoustic signals based on extracting components of the amplitude spectrum of the received sounds and enabling adaptive adjustment of the sensitivity of the signal path in individual frequency bands. Such properties of the filters enable high dynamics and the intelligibility of received sounds, especially human speech, in the presence of noise and external interference, which has a significant impact on the comfort of using a hearing aid and the correctness of human speech recognition. Nowadays, hearing aids are more often manufactured in the form of implants that are placed in the middle ear of hearing-impaired people. In such a case, the problem of reducing power consumption and the voltage supplying the implant becomes particularly important, as the implant itself contains a small store of electrical energy, and its long-term operation relies on the cyclic recharging of energy [6].

Analogue filter implementations (e.g., as in [12–18]) show that analogue filters are more advantageous than fully digital ones from a power reduction perspective. On the other hand, examples of analogue filters realized so far show that it is still difficult to achieve sufficient performance, especially regarding low power consumption, to allow cochlear implant operation without energy charging for many hours. As a result, new, more efficient filter implementations with more favourable parameters are still being researched. Experience from previous implementations of filters in CMOS technology has demonstrated that satisfactory results can be achieved using banks of parallel- [12–14] or cascade- [15–18] connected second-order low-pass filters with electronically tunable quality factor ( $Q$ ).

Cochlear filter banks typically cover the entire acoustic bandwidth, 20 Hz to 20 kHz, which can be limited to the range of 250 Hz–8 kHz when implementing only the speech

recognition function [19]. Coverage of the required bandwidth is achieved using the appropriate number of filters in a bank, with octave-distributed cut-off frequencies ( $\omega_0$ ). As the volume of the received sound changes, adaptive adjustment of the acoustic sensitivity is realized by means of changes in the quality factor ( $Q$ ) of individual filters, which is consistent with the physiology of human hearing [20].

The second-order filter presented in this paper was designed for use in cochlear filter banks. Thus, special attention was paid to voltage and power supply reduction and implementation of effective electronic tuning of the quality factor. MOS transistors operating in the subthreshold region with nano ampere bias currents were used to achieve a significant reduction in power consumption. The following sections of this paper describe the filter circuit, the theoretical analysis of the parameters, and measurement results obtained using a prototype filter fabricated using an X-FAB 180-nm CMOS process.

## 2. Materials and Methods

### 2.1. Principle of Operation

A detailed schematic of the proposed filter and its transconductance-C model are shown in Figure 1.

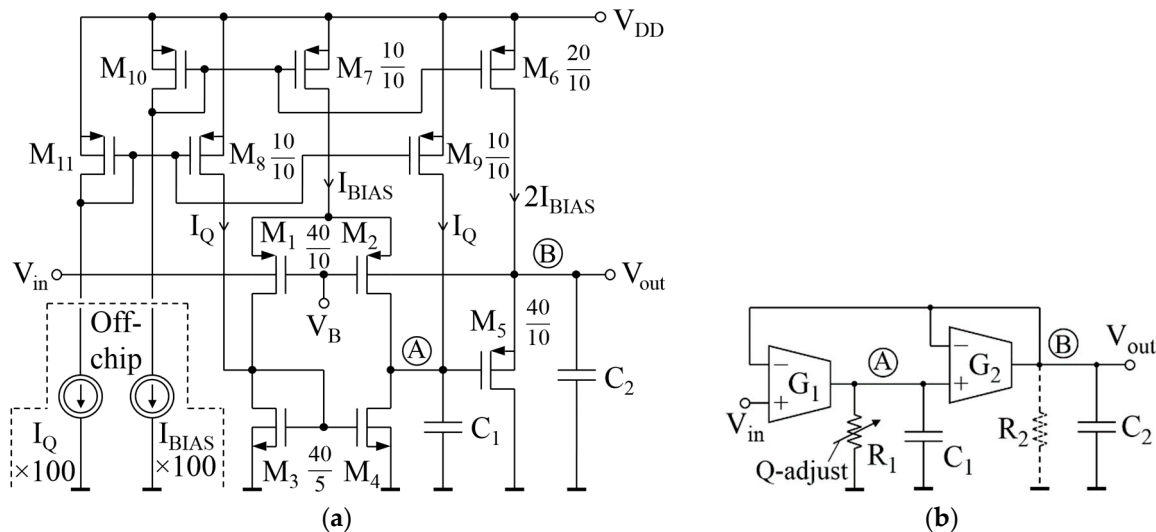


Figure 1. Proposed filter: (a) detailed schematic; and (b) equivalent small-signal, Gm-C network.

The filter consists of two transconductance stages. The first stage is a differential pair ( $M_1, M_2$ ) loaded using a current mirror ( $M_3, M_4$ ) and two extra current sources ( $M_8, M_9$ ). Due to the low supply voltage ( $V_{DD}$ ) of 0.5 V, the bulk-driven differential pair is used. The second stage is a source follower ( $M_5$ ) loaded using a current source ( $M_6$ ). The stages are modelled using the transconductors  $G_1$  and  $G_2$  in Figure 1b. Their transconductances,  $G_1$  and  $G_2$ , are determined by DC bias current  $I_{BIAS}$ . The extra DC current  $I_Q$ , generated by  $M_8$  and  $M_9$ , modifies the resistance seen at node A and, as a result, also modifies the filter quality factor. Nodal resistance is modelled using the adjustable resistor  $R_1$  in Figure 1b.

With  $I_{BIAS}$  and  $I_Q$  less than 50 nA, all transistors in Figure 1a operate in the subthreshold region. The transistors' gate transconductance ( $g_m$ ), back-gate transconductance ( $g_{mbs}$ ), and output conductance ( $g_{ds}$ ) are proportional to their drain current ( $I_D$ ) according to the following relationships

$$g_m \cong \frac{I_D}{nV_t}, g_{mbs} \cong \frac{n-1}{n}g_m = \frac{(n-1)I_D}{n^2V_t}, g_{ds} \cong I_D\lambda_{DS} \tag{1}$$

where  $V_t$  is the thermal voltage, and  $n$  and  $\lambda_{DS}$  are technology-dependent parameters [21,22].

Thus, the transconductances of the stages are

$$G_1 = g_{mbs1} \cong \frac{(n-1)I_{BIAS}}{2n^2V_t}, G_2 = g_{m5} \cong \frac{I_{BIAS}}{nV_t}, \tag{2}$$

and the nodal resistance is

$$R_1 = \frac{1}{g_{ds4} + g_{ds9} + g_{ds2}} \cong \frac{1}{\lambda_{DS}(I_{D4} + I_{D9} + I_{D2})} = \frac{1}{\lambda_{DS}(I_{BIAS} + 2I_Q)} \tag{3}$$

The resistance at node B,  $R_2$ , can be neglected because it is connected in parallel to the resistance  $1/G_2$ , which is much smaller than  $R_2$ ; i.e.,  $1/G_2 \ll R_2$ . With this, the filter transmittance is

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = A \cdot \frac{\omega_0^2}{s^2 + s\omega_0/Q + \omega_0^2} \tag{4}$$

where

$$A = 1 - \frac{1}{G_1R_1 + 1}, \omega_0 = \sqrt{\frac{(G_1 + 1/R_1)G_2}{C_1C_2}}, Q = \frac{\sqrt{(G_1 + 1/R_1)G_2} \cdot \sqrt{\frac{C_1}{C_2}} \cdot R_1}{1 + \frac{C_1}{C_2}G_2R_1} \tag{5}$$

To tune the quality factor effectively, the sensitivity of the  $Q$  parameter with respect to  $R_1$  must be greater than the sensitivity of the other filter parameters. This is satisfied if  $C_2$  is much greater than  $C_1$ , in details  $C_2 \gg C_1G_2R_1$  must be met, which is explained in the following section.

### 2.2. Q Tuning

Thus, assuming that  $C_2 \gg C_1G_2R_1$ , the quality factor Formula (5) becomes

$$Q \stackrel{C_2 \gg C_1G_2R_1}{\cong} \sqrt{(G_1 + 1/R_1)G_2} \cdot \sqrt{\frac{C_1}{C_2}} \cdot R_1 = \omega_0 \cdot C_1 \cdot R_1 \tag{6}$$

The relative sensitivities of the filter parameters with respect to  $R_1$  are

$$S_{R_1}^A = \frac{1}{G_1R_1 + 1}, S_{R_1}^{\omega_0} = -\frac{1}{2(G_1R_1 + 1)}, S_{R_1}^Q = 1 - \frac{1}{2(G_1R_1 + 1)} \tag{7}$$

where the relative sensitivity is defined as  $S_x^y = (dy/y)/(dx/x)$ .

As  $G_1R_1$  is much greater than one,  $G_1R_1 \gg 1$ , and the sensitivity of  $Q$  to  $R_1$  is several times greater than other sensitivities; i.e.,  $S_{R_1}^Q \gg |S_{R_1}^{\omega_0}|$  and  $S_{R_1}^Q \gg S_{R_1}^A$ . As a result, the quality factor adjustment only slightly disturbs the cut-off frequency and DC gain.

The condition  $C_2 \gg C_1G_2R_1$  at (6) is well satisfied in the developed filter, as  $C_2$  is 60 pF,  $C_1$  is 50 fF, and  $G_2R_1$  ranges from 22 to 150.

### 2.3. $\omega_0$ Tuning

The cut-off frequency  $\omega_0$  given by (5) is proportional to  $I_{BIAS}$ ,  $\omega_0 \sim I_{BIAS}$ , which results from the facts that conductances  $G_1$ ,  $G_2$ , and  $1/R_1$  are  $\sim I_{BIAS}$ . Using the same facts in (6), it can be deduced that  $Q$  should vary moderately when  $I_{BIAS}$  changes. The sensitivities of  $A$ ,  $\omega_0$ , and  $Q$  with respect to  $I_{BIAS}$  are as follows

$$S_{I_{BIAS}}^A = \frac{2I_Q}{I_{BIAS}(\eta + 1) + 2I_Q} \cong 0, S_{I_{BIAS}}^{\omega_0} = 1 - \frac{I_Q}{I_{BIAS}(\eta + 1) + 2I_Q} \cong 1, S_{I_{BIAS}}^Q = S_{I_{BIAS}}^{\omega_0} - \frac{I_{BIAS}}{I_{BIAS} + 2I_Q} \tag{8}$$

where  $\eta = (n-1)/(2n^2V_t\lambda_{DS})$ . When the typical parameters of the process are used (i.e.,  $n \approx 1.3$ ,  $\lambda_{DS} \approx 0.01 \text{ V}^{-1}$ , and  $V_t \approx 25 \text{ mV}$ ), the  $\eta$  is about 350. Therefore, the sensitivity of

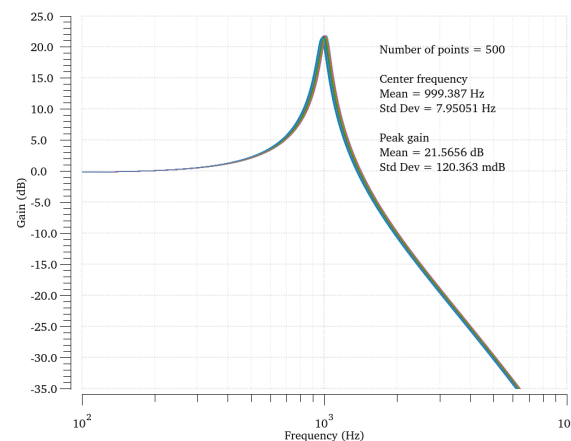
$\omega_0$  to  $I_{BIAS}$  is approximately equal to unity and is always greater than the sensitivity of  $Q$  to  $I_{BIAS}$ .

#### 2.4. Mismatch

Technological mismatch affects all filter components (and hence, filter parameters) according to general rules, and are not analysed in detail here. However, the mismatch related to components  $C_1$  and  $R_1$  requires some comment.

The small capacitor  $C_1$  is exposed to mismatch because of its small area (the Pelgrom rule) and the increased proportion of parasitic capacitances. Fortunately, the sensitivities of the filter parameters with respect to  $C_1$  do not depend on the value of  $C_1$ : these sensitivities are constant and less than one; i.e.,  $S_{C_1}^{\omega_0} = -0.5$ ,  $S_{C_1}^Q = 0.5$ , and  $S_{C_1}^A = 0$ . Thanks to this, the negative impact of a small  $C_1$  on the filter characteristic is reduced.

As  $S_{R_1}^Q \cong 1$ , deviations in  $R_1$  caused by mismatch directly translate into the spread of the quality factor. The mismatch in  $R_1$  may be relatively high, because  $R_1$  depends on many factors, such as transistor drain currents, channel lengths,  $\lambda_{DS}$  parameter, etc., which are sensitive to mismatch as well. However, detailed Monte Carlo simulations, taking into account all possible mismatch factors, show that  $\omega_0$  spreads from 971 to 1023 Hz and  $Q$  varies from 21.15 to 21.9 dB, which means that the 1-sigma deviations in  $\omega_0$  and  $Q$  are 7.95 Hz and 0.12 dB, respectively; i.e., only 0.8% and 0.5%, respectively, with respect to the mean values 0.99 kHz and 21.5 dB, as shown in Figure 2.



**Figure 2.** Monte Carlo simulation results (Cadence Spectre) of the 1 kHz filter in Figure 1a.

#### 2.5. Noise

Figure 3a depicts the noise model of the filter. Sources  $v_{n1}$  and  $v_{n2}$  represent the input-referred noise of the respective amplifiers. The thermal noise of resistor  $R_1$  is assumed to be included in  $v_{n1}$  because this resistor is a part of amplifier  $G_1$ ; i.e.,  $R_1$  is the output resistance of this amplifier.

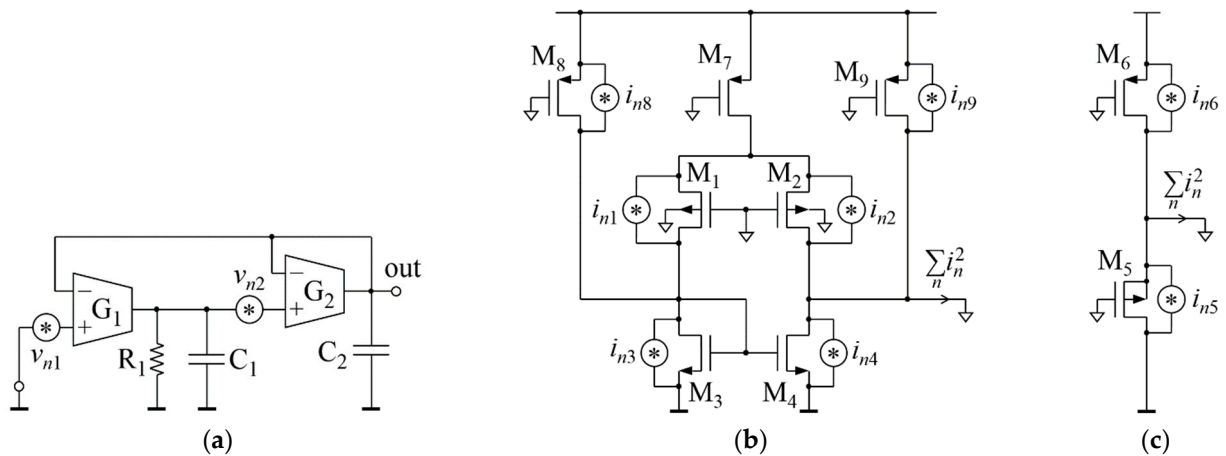


Figure 3. Noise schematics for: (a) the whole filter; (b) the amplifier G<sub>1</sub>; and (c) the amplifier G<sub>2</sub>.

Based on Figure 3a, the total filter noise (power spectral density) referred to the filter input is

$$v_{n,in}^2(\omega) = \frac{v_{n1}^2(\omega) \cdot |H(j\omega)|^2 + v_{n2}^2(\omega) \cdot |H(j\omega)|^2 \cdot \left| \frac{1/R_1 + j\omega C_1}{G_1} \right|^2}{|H(j\omega)|^2} = v_{n1}^2(\omega) + v_{n2}^2(\omega) \cdot \frac{\frac{1}{R_1^2} + \omega^2 C_1^2}{G_1^2} \tag{9}$$

where  $v_{n1}^2(\omega)$  and  $v_{n2}^2(\omega)$  denote the power spectral density of the respective noise sources.

Figure 3b,c show the amplifier schematics containing all relevant sources of transistor noise ( $i_{n7}$  noise has been neglected, as it is attenuated by a differential stage). Based on these schematics,  $v_{n1}^2(\omega)$  and  $v_{n2}^2(\omega)$  are

$$v_{n1}^2(\omega) = \frac{\sum i_n^2}{G_1^2} = \frac{i_{n1}^2(\omega) + i_{n2}^2(\omega) + i_{n3}^2(\omega) + i_{n4}^2(\omega) + i_{n8}^2(\omega) + i_{n9}^2(\omega)}{G_1^2}, \quad v_{n2}^2(\omega) = \frac{\sum i_n^2}{G_2^2} = \frac{i_{n5}^2(\omega) + i_{n6}^2(\omega)}{G_2^2} \tag{10}$$

The Q tuning mechanism introduces extra noise, which is related to the finite resistance  $R_1$  in (9) and the additional noise currents  $i_{n8}$  and  $i_{n9}$  in (10). The power density of this extra noise can be estimated by calculating the difference in the input-referred noise of the filter with Q tuning, (9), and without one; i.e.,

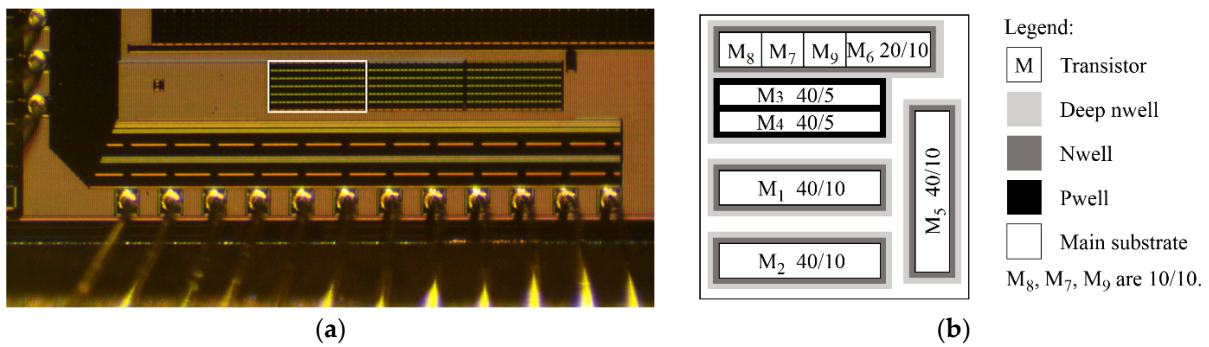
$$v_{n,in}^2(\omega) - v_{n,in,without\ Q\ tuning}^2(\omega) = \frac{i_{n8}^2(\omega) + i_{n9}^2(\omega)}{G_1^2} + \frac{i_{n5}^2(\omega) + i_{n6}^2(\omega)}{G_1^2 R_1^2 G_2^2} \cong \frac{i_{n8}^2(\omega) + i_{n9}^2(\omega)}{G_1^2} \tag{11}$$

Formula (11) shows that the additional noise related to the Q-tuning mechanism is mainly due to the noise generated by transistors M<sub>8</sub> and M<sub>9</sub>. As the noise of these transistors increases with their bias current  $I_Q$ , a filter variant with low Q has more noise compared to a high-Q variant. The simulated worst-case noise of the 1 kHz ( $I_{BIAS} = 3$  nA) filter in Figure 1a is with a maximal  $I_Q$  of 40 nA ( $Q = 1.9$ ), and is 60  $\mu V_{RMS}$  when referred to the filter input and integrated from 100 Hz to 1.5 kHz. Assuming no transistors M<sub>8</sub> and M<sub>9</sub>, the filter noise is 40  $\mu V_{RMS}$ , which means that the additional Q-tuning circuit increases the filter noise by 50%.

### 3. Experiments

#### 3.1. The Chip and Measurements

The filter was implemented in the integrated circuit shown in Figure 4a. A white rectangle indicates an area of the filter, which is 128  $\mu m$  by 258  $\mu m$ , including metal-insulator-metal (MIM) capacitors. MIM capacitors cover the entire filter; hence, no transistors are visible in the micro photo.

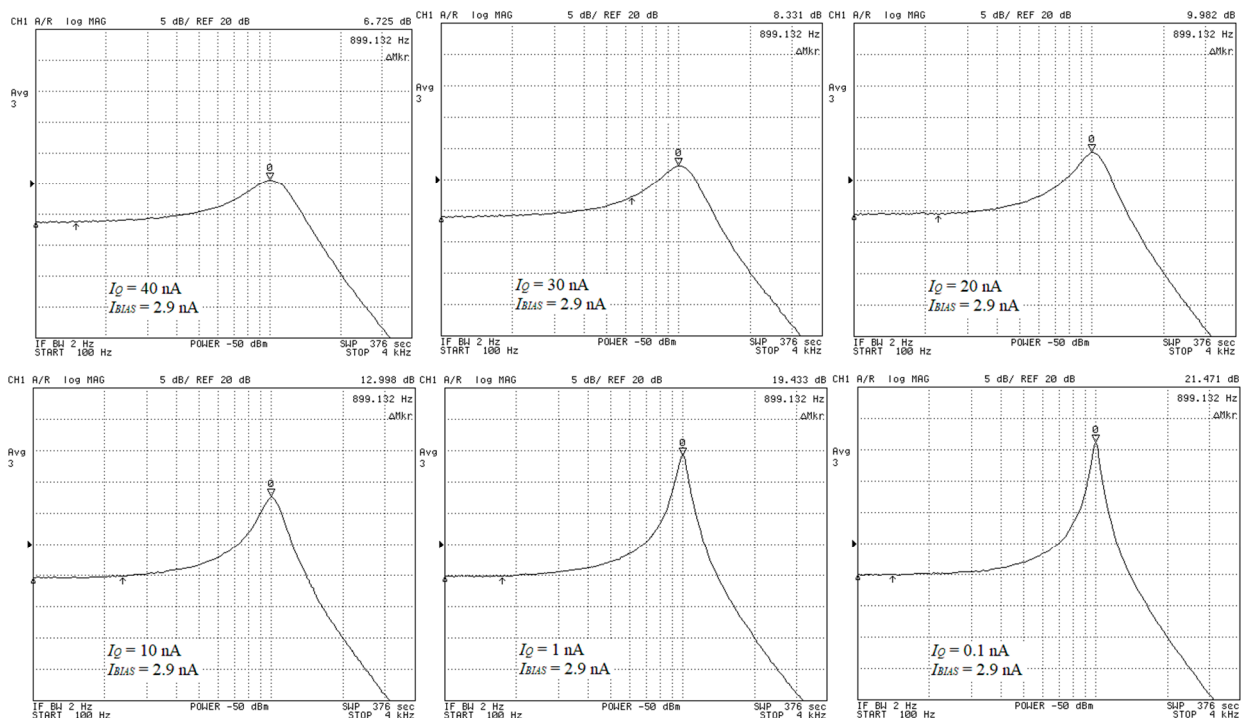


**Figure 4.** Fabricated filter: (a) micro photo; and (b) simplified view of a filter cell. Transistor dimensions,  $W/L$ , are in  $\mu\text{m}/\mu\text{m}$ .

The arrangement of transistors inside the filter cell is illustrated in Figure 4b. The filter cell contains transistors  $M_1$  to  $M_9$ ; their dimensions,  $W/L$  in  $\mu\text{m}/\mu\text{m}$ , are as follows:  $M_1$  and  $M_2$ , 40/10;  $M_3$  and  $M_4$ , 40/5;  $M_5$ , 40/10;  $M_6$ , 20/10; and  $M_7$ ,  $M_8$ , and  $M_9$ , 10/10. Transistors  $M_{10}$  and  $M_{11}$  are outside the cell because they are wide (one hundred parallel-connected 10/10 devices each) to conduct off-chip bias currents. All transistors are thin-oxide low- $V_T$  devices with threshold voltages ( $V_T$ ) of 0.34 V and  $-0.39$  V for  $n$  and  $p$  type devices, respectively. Low threshold voltages are necessary due to the 0.5 V supply voltage. As low- $V_T$  transistors have relatively high channel leakage, long 10  $\mu\text{m}$  channels are used, which reduce leakage to much below 0.1 nA at temperatures up to 50 °C.

In the following, measurement results for the filter operating using the supply voltage  $V_{DD} = 0.5$  V, a gate bias voltage  $V_B = 150$  mV, and input DC level of 360 mV are reported.

Figure 5 illustrates the  $Q$  tuning process, along with an  $I_Q$  ranging from 40 to 0.1 nA. On successive screens from the analyser, it is seen that  $Q$  increases from 6.7 dB (2.16) to 21.4 dB (11.74), and there is no deviation in  $\omega_0$  (1 kHz). Thus, this observation addresses (7), and confirms that the sensitivity of  $Q$  to  $R_1$  is much greater than that of  $\omega_0$  to  $R_1$ .



**Figure 5.** Tuning of  $Q$  measured at  $\omega_0$  of 1 kHz.  $I_Q$  is 40, 30, 20, 10, 1, and 0.1 nA.  $I_{BIAS}$  is 2.9 nA.

The frequency tuning range was also examined. The consecutive screens in Figure 6 present the measured filter amplitude responses, in which  $\omega_0$  increases from 500 Hz to 2.5 kHz, with  $I_{BIAS}$  from 1.4 to 7.7 nA. In this case, the quality factor varies due to changes in transistor conductances: the  $Q$  deviation is  $\pm 12\%$  or  $\pm 2\%$ , assuming a tuning range of 0.5–2.5 kHz or 1–1.5 kHz, respectively. Quality factor deviations can be compensated by appropriate corrections of  $I_Q$ . For example,  $\omega_0$  and  $Q$  are 1 kHz and 21 dB, respectively, at an  $I_{BIAS}$  of 2.9 nA and an  $I_Q$  of 0.1 nA. If  $\omega_0$  is set to 1.5 kHz using an  $I_{BIAS}$  of 4.5 nA, then  $I_Q$  must be corrected to 0.3 nA to maintain the quality factor at the same level.

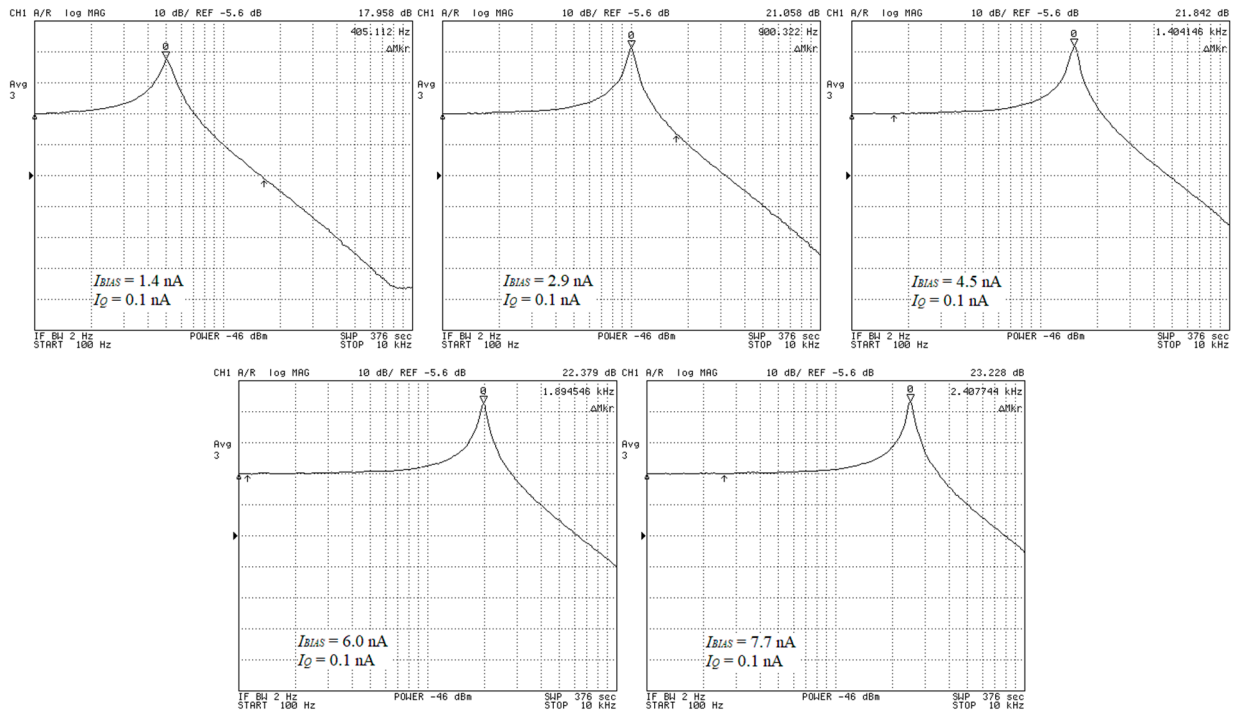


Figure 6. Tuning of  $\omega_0$  at  $Q$  of 21dB.  $I_{BIAS}$  is 1.4, 2.9, 4.5, 6, and 7.7 nA.  $I_Q$  is 0.1 nA.

Figure 7a,b show the filter noise density and total-harmonic-distortion (THD) parameter measured at the filter output, respectively. The total noise, referred to the filter input and integrated from 100 Hz to 2 kHz, is  $70 \mu V_{RMS}$ . The 1% output THD occurs with an input 200 Hz sine wave with an amplitude of  $67 mV_{RMS}$ , which results in a signal-to-noise (S/N) ratio of 59.7 dB.

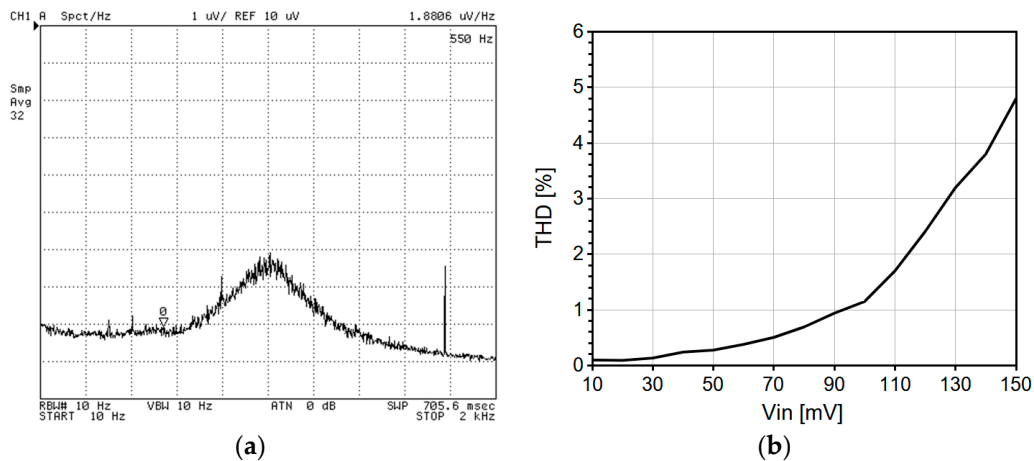


Figure 7. Measured (a) output noise of the 1 kHz filter with  $Q = 2$ ; and (b) output THD vs. input amplitude.

Measured filter parameters are summarized in Table 1. Power consumption ranges from 2.2 to 52 nW, depending on the  $Q$  and  $\omega_0$  values. The power and noise performance of the filter presented in this work are better compared to other solutions, except that of [23]. In terms of quality factor range, the realization of this work meets the minimum requirements for cochlear applications (a  $Q$  range of 2–11). The best  $Q$  range, 1.3–39, was reported in [14].

**Table 1.** Performance comparison of low-frequency filters with tunable  $Q$ .

Parameter	This Work	[23] Simulated	[18]	[12]	[13]	[14]
Process	0.18 $\mu\text{m}$	0.18 $\mu\text{m}$	0.35 $\mu\text{m}$	0.35 $\mu\text{m}$	1.5 $\mu\text{m}$	0.18 $\mu\text{m}$
Supply	0.5 V	0.5 V	3.3 V	3.3 V	2.8 V	0.5 V
Power	2.2–52 nW	8.25–10.75 nW	NA	13–20 $\mu\text{W}$ <sup>1</sup>	0.1–5.4 $\mu\text{W}$	0.1–100 nW <sup>2</sup>
$\omega_0$	0.5–2.5 kHz	1.28 kHz	0.1–20 kHz bank	0.31–8 kHz bank	0.2–6 kHz bank	0.08–20 kHz bank
$Q$	2–11	2–40	NA	2–19	1–10	1.3–39
S/N	59 dB	68 dB	36–52 <sup>3</sup> dB	17–32 dB	57 dB	40–55 dB

<sup>1</sup> Estimated. <sup>2</sup> Estimated assuming no PGA. <sup>3</sup> With PGA.

The frequency tuning range of this work’s filter, 0.5–2.5 kHz, cannot be meaningfully compared, because other references report only the frequency range of an entire bank of filters (e.g., 0.1–20 kHz), and not those of individual filters.

The next section discusses the frequency range of a filter bank assuming use of the filter presented in Figure 1a.

### 3.2. Filter Bank Design Example (Simulations)

A filter bank is a cascade of filters with different nominal cut-off frequencies. To change the nominal cut-off frequency of the filter in Figure 1a, the circuit must be redesigned by appropriately scaling the bias current, capacitance, and transistor dimensions. Taking into account practical design limits, such as a minimum transistor bias current of 0.5 nA (which implies that  $I_{BIAS} \geq 1$  nA) and the upper capacitance limit of 100 pF, the cut-off frequency can be scaled down to 500 Hz, according to Table 2.

**Table 2.** Scaling a filter bank—simulations<sup>1</sup>.

$\omega_0$ (kHz)	$C_2$ (pF)	$I_{BIAS}$ (nA)	$M^2$	$I_Q$ (nA)		$P$ (nW)	
				$Q = 11.22$ (21 dB)	$Q = 5.01$ (14 dB)	$Q = 11.22$ (21 dB)	$Q = 5.01$ (14 dB)
0.5	60	1.42	1	0.025	1.54	2.155	3.67
1	60	2.93	1	0.136	3.1	4.531	7.495
2	30	6.01	2	0.453	6.2	9.468	15.215
4	15	9.12	2	0.198	5.83	13.878	19.51
8	7.5	9.4	2	0.055	5.95	14.155	20.05

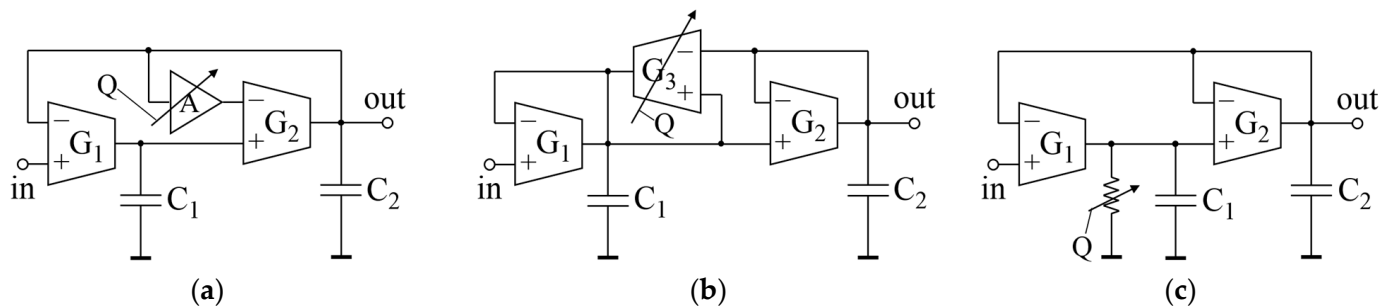
<sup>1</sup> Process: X-FAB 180-nm (xh018). Transistors: thin oxide 1.8 V, low VT. <sup>2</sup> Transistor multiplication factor (the number of parallel connected transistors).

On the other side, the upper range of the cut-off frequency is limited by two factors: a minimum value of filter capacitance allowed due to mismatch, and a maximum value of  $I_{BIAS}$  related to a power limit. So, based on the worst power case selected from Table 1 (which is [12]), the practical limit of 20  $\mu\text{W}$  per single filter in a bank can be assumed, which is well above the 52 nW achieved in this work. Nevertheless, scaling up  $I_{BIAS}$  involves upscaling the transistors’ widths (according to scaling factor  $M$  in Table 2), which results in a larger parasitic capacitance at node A. This parasite limits the cut-off frequency to 8 kHz, which is quite sufficient for speech recognition systems.



#### 4. Discussion

Selecting an appropriate filter structure to build a filter bank is related to the method for tuning the filter quality factor. Depending on the filter structure, the quality factor is adjusted by changing a specific circuit parameter, e.g., the amplifier gain, transconductance, resistance, etc. However, changes in circuit parameters always affect the filter cut-off frequency to a greater or lesser extent. Figure 8 schematically illustrates three different methods of  $Q$  tuning: the one proposed in this paper and two others that are applicable to transconductance-C (Gm-C) filter structures. These three methods are briefly discussed and compared.



**Figure 8.** Methods used to tune a quality factor using: (a) a voltage attenuator; (b) an additional transconductor; and (c) a transconductor's output resistance.

The filter shown in Figure 8a uses a loop-in voltage attenuator (A) to tune the quality factor [23]. This method is the only one among those illustrated that allows for fully independent control of the quality factor and cut-off frequency. The disadvantage of this scheme is a certain difficulty in implementing the attenuator, which must attenuate only AC signals, not DC signals.

In the classic method illustrated in Figure 8b, the quality factor is tuned independently by means of the additional transconductance  $G_3$  [16–18,24]. Independent tuning of the cut-off frequency is possible, but  $G_1/G_2$  and  $G_3/G_2$  ratios must be kept constant. Therefore, the robustness of this filter to the transconductance mismatch is weaker compared to that of the other solutions.

The technique proposed in this paper (Figure 8c) uses the adjustable output resistance of a transconductance amplifier to tune the filter quality factor. This is a compromised solution, because the quality factor can be controlled independently, while frequency tuning causes some deviations in the  $Q$  factor. The robustness of filter characteristics to technological mismatch is at a satisfactory level despite the capacitance disparity ( $C_1 \ll C_2$ ), as previously mentioned. The proposed quality factor tuning technique's advantages include relatively simple implementation, because it does not require additional amplifiers, transconductors, etc., but only requires simple DC current sources.

#### 5. Conclusions

The filter presented in this paper can be used to implement low-cost filter banks that emulate the characteristics of the cochlea over the speech frequency range. The proposed filter belongs to the class of buffer-based filters [25] characterized by a DC voltage gain close to unity and an insensitivity to mismatch in the filter passband. Therefore, the proposed filter is suitable for both parallel and cascade banks.

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