

Experimental test results of an automatic voltage regulator with independent phase voltage controllers

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Abstract. The growing number of distributed renewable energy sources and dynamic constant-power loads (e.g. electric vehicle charging stations) pose new challenges for network operators. These changes result in alterations to network load profiles and load flows, leading to greater voltage volatility. One effective solution to these problems can be the use of automatic voltage regulators (AVRs), which stabilize and symmetrize voltage output, whether at distribution transformers (DTs) or elsewhere in the distribution network. The device developed by the authors consists of two bidirectional power converters and three single-phase transformers connected in series to the low-voltage grid as a stabilizer. The proposed control system provides accurate and fast regulation of the AVR's output voltage (within the range of $\pm 10\%$ of the nominal grid voltage), with each phase being independently adjusted, regardless of the type of power load. The article includes test results demonstrating selected functionalities of the developed AVR. The physical model of the device discussed in the article is a research component of the LINTE² laboratory of the Gdańsk University of Technology.

Key words: automatic voltage regulator, grid voltage control, distribution transformer, hybrid transformer, power electronics converter, smart grids

1. INTRODUCTION

The operating conditions of the power distribution grid have changed in recent years. The number of loads with constant power demand has increased [1, 2]. For such electrical equipment, a decrease in the supply voltage causes an increase in current consumption, exacerbating voltage drop in the power line. On the other hand, the growing number of renewable generation systems connected to distribution grids can cause problems with excessively high voltage in the power grid. Additionally, renewable energy is characterized by high variability of energy generation depending on weather conditions [3, 4]. As a result, the power flow in distribution grids becomes more complicated, making it more difficult to maintain supply voltage within acceptable limits [5, 6].

A common method of maintaining an appropriate voltage level in the distribution grid is through on-load tap changing of the transformers [6]. This is typically achieved using electromechanical tap changers, which have drawbacks such as poor dynamics, arcing and high operation costs [7, 8, 9]. Thyristor tap changers can improve the dynamic of voltage control, but at the cost of additional conduction losses and the output voltage can still be changed discretely [5, 9].

Smooth and fast regulation of voltage and current in the distribution network is enabled by power electronics transformers (or solid-state transformers (SST)) [10, 11, 12]. However, their significantly higher price and lower reliability mean that they have not been widely used in distribution networks [8, 13].

In recent years, alongside SST, various types of power electronic systems have been developed to compensate and im-

prove voltage quality in AC transmission networks (Flexible AC Transmission Systems (FACTS)) and distribution grids (Custom Power Devices (CPD)) [14]. The AVR presented in the article is the most similar in terms of topology and functional features to the Unified Power Flow Controller (UPFC) [14, 15, 16], Unified Power Quality Conditioner (UPQC) [17, 18, 19], and particularly the Hybrid Distribution Transformer (HDT) [5, 7, 8, 20, 21, 22].

The UPFC can independently control voltage, phase angle and impedance in the transmission line. This tasks are usually carried out in the fundamental harmonic domain [14]. The UPQC is used in the distribution grid mainly to provide sinusoidal balanced voltage to the load and simultaneously to ensure the flow of sinusoidal and symmetrical currents from the source, irrespective of distortion or unbalance on the load or source side [17].

The power electronic system of HDT combines the functionalities of the aforementioned devices, with characteristic features including close integration with DT and low rated power, typically between 10% and 20% of the distribution transformer. Therefore, the losses of the converter slightly deteriorate the HDT efficiency [5, 7, 8].

This paper presents an automatic voltage regulator based on a back-to-back converter system and a series transformers. It was designed to symmetrize and regulate voltages in distribution network feeding station, but it is feasible to install it at any point in the distribution grid, e.g. at sensitive loads or at places of line cross-section change.

The literature describes many different control methods for systems such as AVR; a brief overview is contained in [17]. The two most common control techniques are the instant-

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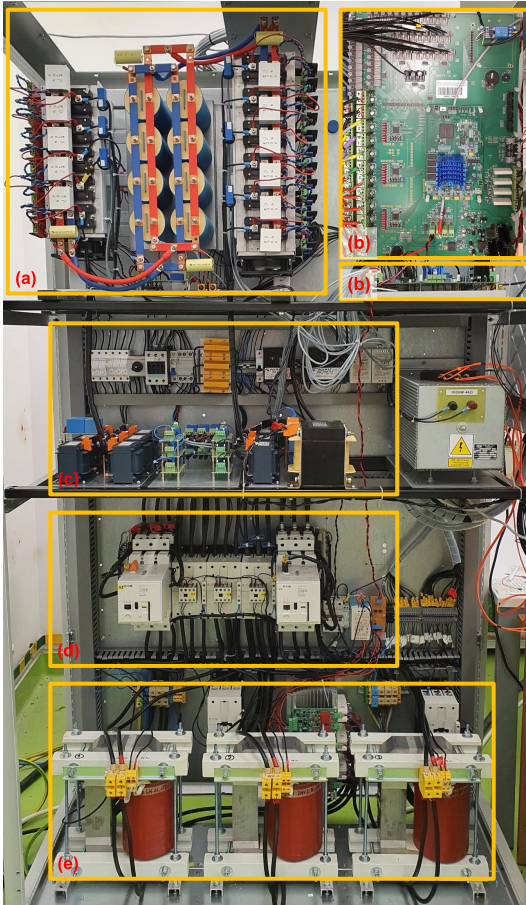


Fig. 2. Laboratory model of the automatic voltage regulator: a) AC/DC/AC converter b) AVR controller c) converters passive filters d) electrical switching devices e) series transformers.

(K_e) was constructed using bidirectional thyristor switches to safeguard the AVR against excessive currents in the converter circuits, such as during external short circuits at the AVR output. The shunt circuit (K_m), based on electromechanical contactors, facilitates the shutdown of the AVR, for example, during failure or AVR maintenance work.

3. CONTROL SYSTEM OF AUTOMATIC VOLTAGE REGULATOR

The AVR control system can be divided into two parts: the control system of the AC/DC converter, which provides a DC voltage of the required value, and the DC/AC inverters that are powered by it. On the other hand, the main task of the DC/AC converter control system is to regulate the phase voltages (fundamental harmonic) at the AVR output within $\pm 10\%$ of the nominal grid voltage.

A. AC/DC converter control system

A classical cascade control system shown in Figure 3 has been implemented in order to control the DC-link voltage. The DC voltage PI controller settings (K_{Pdc} , K_{Idc}) were determined for the 60 Hz control band. The grid currents are regulated in the dq coordinate system rotating synchronously with the angular frequency of the supply voltage. The parameters of the PI con-

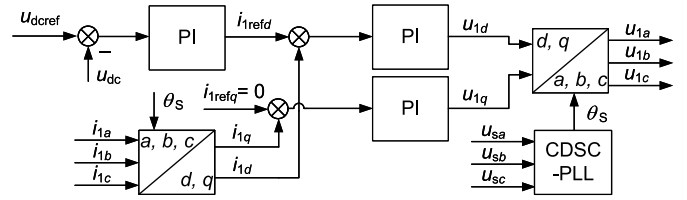


Fig. 3. Block diagram of the AC/DC converter control system.

trollers (K_{Pdq} , K_{Idq}) were calculated for a control bandwidth of 320 Hz.

The Cascaded Delayed Signal Cancellation - Phase Locked Loop (CDSC-PLL) algorithm [23] was used to determine the phase angle of the fundamental harmonic of the grid voltage. The PI controller settings used in this algorithm were selected for the 50 Hz control band.

B. DC/AC converter control system

The DC/AC converter allows the generation of appropriate series voltages, which are added to the secondary side voltages of the distribution transformer Tr_S through the transformers Tr_{SE} . Three independent series voltage regulators were proposed, one for each phase. They allow independent and fast adjustment of individual phase voltages on the AVR output. The block diagram of the load voltage controller for one phase is shown in Figure 4.

Using the recursive discrete Fourier transform (RDFT) algorithm, the amplitude of the fundamental harmonic (U_{S1x}) of the input phase voltage (u_{Sx}) is calculated and subtracted from the amplitude of the reference load voltage (U_{Lref}). In this way, the amplitude of the series voltage (U_{SEx}) to be obtained at the secondary side of the transformer Tr_{SE} is calculated. This amplitude is limited to the maximum value that can be generated (U_{SEmax}). The value of U_{SEmax} is determined by the parameters of the series transformer used, the value was assumed to be equal to the amplitude of the rated voltage of the secondary side of the transformer Tr_{SE} . Similarly, the amplitude (U_{Lrefx}) of the reference phase voltage at the AVR output (u_{Lrefx}) is equal to U_{Lref} if it is less than the maximum achievable voltage, otherwise it is limited to $U_{Lrefx,min} = U_{S1x} - U_{SEmax}$ or $U_{Lrefx,max} = U_{S1x} + U_{SEmax}$.

The reference values u_{SErefx} and u_{Lrefx} are cosine signals, scaled by the Tr_{SE} transformer ratio N_{SE} , whose argument is equal to the sum of the instantaneous phase Θ_S of the supply voltage, estimated by the CDSC-PLL algorithm and a fixed phase shift ($\phi_a = 0, \phi_b = -2\pi/3, \phi_c = 2\pi/3$). The voltage u_{SErefx} is one of the components of the reference output voltage (u_{fx}) of the voltage source inverter. Its value depends directly on the difference between the referenced and estimated amplitude of the input phase voltage.

The difference of u_{Lrefx} and the measured load voltage u_{Lx} , is the voltage regulation error e_{ux} , which is fed to the input of a resonant controller (R_{res}) with transfer function:

$$R_{res}(z) = K_{IL} \frac{\sin(\omega_1 T_s)}{2\omega_1} \frac{1 - z^{-2}}{1 - 2\cos(\omega_1 T_s)z^{-1} + z} \quad (1)$$

where: ω_1 is the mains angular frequency and K_{IL} - integral

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$1.08U_n$, $0.92U_n$, $1.1U_n$, $0.9U_n$, $1.15U_n$, $0.85U_n$, $1.0U_n$. In Figures 6-8, the signals in phases a, b, c are marked with red, green and blue, respectively, and the reference output voltage U_{Lref} - in magenta.

The RMS values presented in the figures were calculated in a moving window of fixed length (N), based on the general formula:

$$X[k] = \sqrt{\frac{1}{N} \sum_{n=k-N+1}^k x^2[n]}, N = f_s/f_n \quad (3)$$

where: x is a signal registered by the AVR controller and f_s - sampling frequency. The RMS values of the series voltages (U_{SEx}) have been calculated as the differences between the RMS values of the output and input voltages of the AVR ($U_{SEx} = U_{Lx} - U_{Sx}$).

Figures 6f-8f show the RMS waveforms of load currents (I_{Lx}) that contain information about the value and symmetry of the load connected to the AVR output.

In the case shown in Figure 6, the AVR was loaded with a three-phase symmetrical resistor providing currents of approximately $1.05I_n$ (Figure 6f) at the rated output voltage.

Figure 7 shows a test in which the AVR was loaded with a symmetrical resistive load of about $0.26S_n$ and a three-phase six-pulse diode rectifier loaded with resistance, the rectifier was connected to the AVR output through chokes of an inductance of 3 mH. The total apparent power of the load was $0.77S_n$.

Figure 8 concerns the AVR operation with an unbalanced single-phase resistive load in phase c . The RMS value of the current in the loaded phase is about $0.8I_n$ (Figure 8f) at the rated output voltage.

Figures 6a-8a show the RMS waveforms of the referenced and measured phase voltages at the AVR output. For the first two types of loads (Figures 6a-7a), the setpoints $1.08U_n$, $1.1U_n$, $1.15U_n$ and $0.85U_n$ have not been reached due to the applied limitation of the series voltages U_{SEx} to $\pm 0.1U_n$ (cf. Figures 6d-7d). For the other setpoints, the differences in the RMS values of the referenced and measured voltages are within the tolerance band of $\pm 0.2\%U_n$ (Figures 6b-7b). Since the reference voltage is the same for each phase, thus the output voltages are balanced. The spiky behavior of the signals presented in Figures 6b-8b is a result of transients related to step changes in the reference voltage and the limited dynamics of the AVR control system. Due to the very high magnification of the waveforms near zero, the vanishing transients are visible for a long time. Additionally, because of the relatively small range of the y-axis, $U_{Lref} - U_{Lx}$ differences outside this range are not visible in a few of the time intervals in Figures 6b-8b.

The situation for the single-phase load (Figures 8a,b) is slightly different than for the previously discussed cases. In the unloaded phases (a and b) the RMS values of load voltages do not reach the setpoint values when U_{Lref} is equal to $0.9U_n$, $1.15U_n$, $0.85U_n$ (Figures 8a,b), while in the phase c - when U_{Lref} is equal to $1.1U_n$, $1.15U_n$, $0.85U_n$. In case of $U_{Lref} = 1.08U_n$, the maximum series voltage is generated in phase c (Figure 8d). Despite this, the output voltage is not

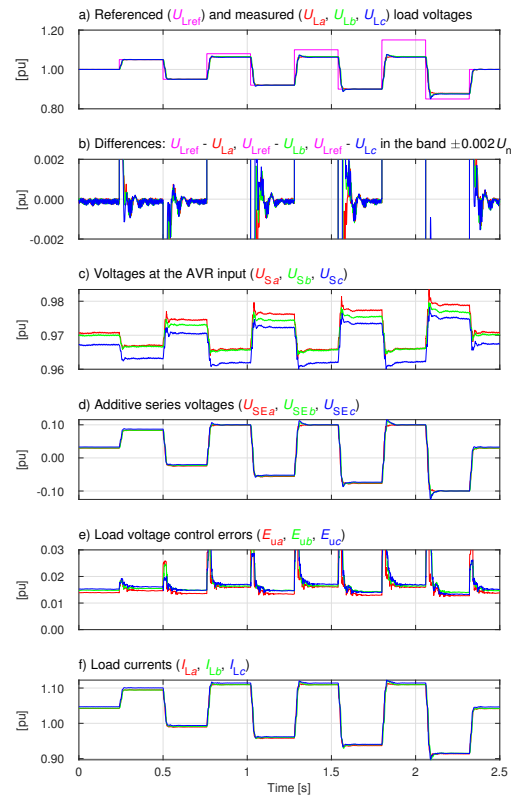


Fig. 6. RMS waveforms during the step changes of the load voltages with three-phase symmetrical resistive load.

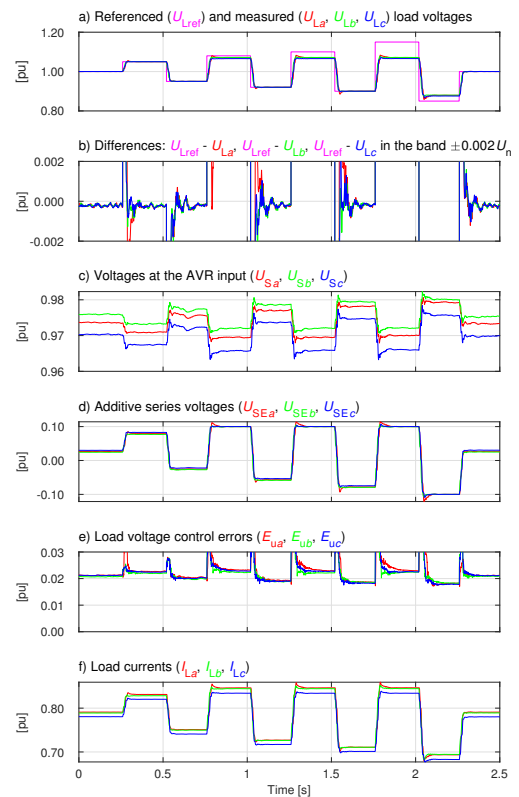


Fig. 7. RMS waveforms during the step changes of the load voltages with three-phase symmetrical nonlinear load.

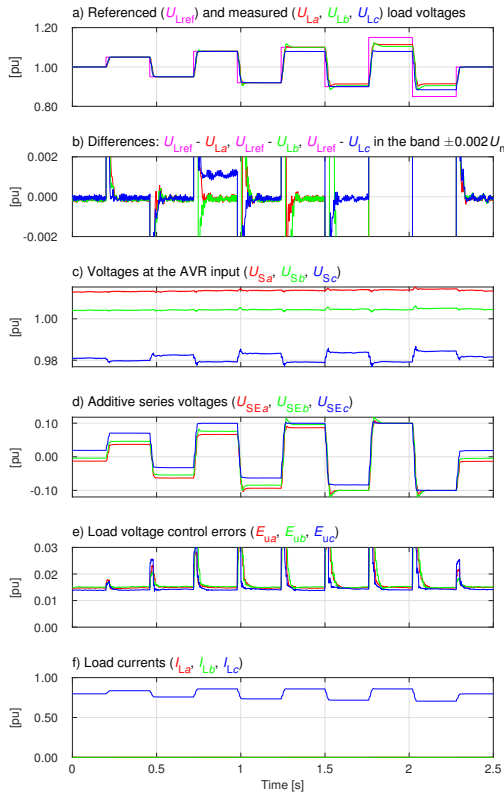


Fig. 8. RMS waveforms during the step changes of the load voltages with single-phase unsymmetrical resistive load.

able to reach the referenced value and a small error (approx. $0.1\%U_n$) is clearly visible within the assumed tolerance band of $\pm 0.2\%U_n$.

A slight unbalance, visible in the AVR input voltages for all types of loads (Figures 6c-8c), is not present in the AVR output voltages (Figures 6a,b-8a,b), when the additive series voltages are not limited. If the series voltage is limited in at least one phase, the AVR output voltages may be unbalanced. In such a situation, the voltages in the other two phases are not regulated in order to balance the AVR output voltages. This is due to the fully independent operation of the voltage controller in each phase. The described operating state of the AVR system can be seen clearly in Figure 8 when $U_{Lref} = 1.1U_n$ (period: 1.25 - 1.5s). Additive series voltage in phase *c* is limited while in the other phases are still below the limit (Fig. 8d). Consequently, the output voltages in phases *a* and *b* reach the referenced values, while the voltage in phase *c* is noticeably lower. An analogous situation is apparent when $U_{Lref} = 0.9U_n$ (period: 1.5s - 1.75s), where only the output voltage in phase *c* reaches the reference value and the voltages in the other phases are higher than it due to limitations.

Load voltage control error e_{ux} is the difference between a reference voltage u_{Lrefx} and a measured voltage u_{Lx} at the AVR output phase, where u_{Lrefx} is the reference value after passing through the amplitude limiting algorithm. Therefore the RMS value of the load voltage control error (Figures 6e-8e) is a measure of the imperfection between referenced and measured voltage at the AVR output. In a situation where the fundamental harmonics of the output voltages are generated pre-

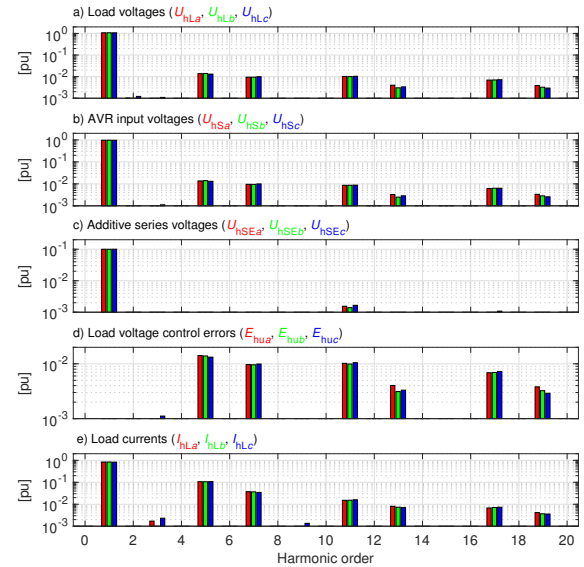


Fig. 9. Amplitude spectra of selected signals at $U_{Lref} = 1.15U_n$ and three-phase symmetrical non-linear load.

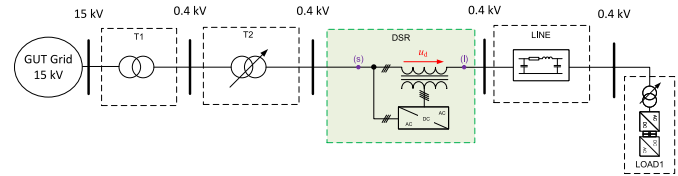


Fig. 10. Test system topology - case 2.

cisely (as in our case, cf. Fig 9d), the E_{ux} signals indirectly characterize the level of distortion of the load voltages. It is significantly higher for a nonlinear load (Figure 7e), despite its lowest power.

Similar conclusions about the operation of the system can be obtained by analyzing the spectra of the signals presented in Figures 6-8. For example, Figure 9 shows amplitude spectra of u_{Lx} , u_{Sx} , u_{SEx} , control errors e_{ux} , and currents i_{Lx} for a nonlinear load at $U_{Lref} = 1.15U_n$ (cf. Figure 7).

The fundamental harmonics in the spectra of load voltage control errors E_{hux} (Figure 9d) reach values below $0.1U_n$, which proves that the resonant controller R_{rez} precisely regulates the value of the fundamental harmonic in steady state. However, due to the relatively narrow frequency band, it does not allow to reduce the higher harmonics of the load voltages. Nevertheless, with precise regulation of the fundamental harmonics of the load voltages and its relatively small distortions, the RMS values are also stabilized with high accuracy. The content of higher harmonics in the AVR output (Figure 9a) and input voltages (Figure 9b) is very similar. The load voltage control system does not significantly modify the voltage spectrum of the distribution transformer, the additive series voltages (Figure 9c) are approximately sinusoidal.

B. Case 2 - variation of the AVR input voltages

The tests were carried out in the arrangement shown in Figure 10.

The AVR input voltages are varied by changing the taps of

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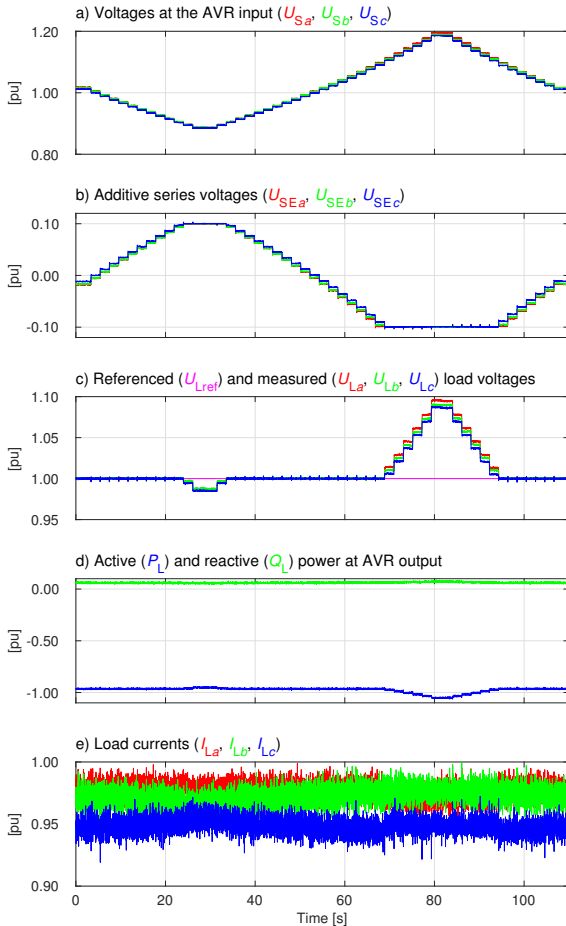


Fig. 11. RMS waveforms during the changes in AVR input voltages while transferring energy to the mains.

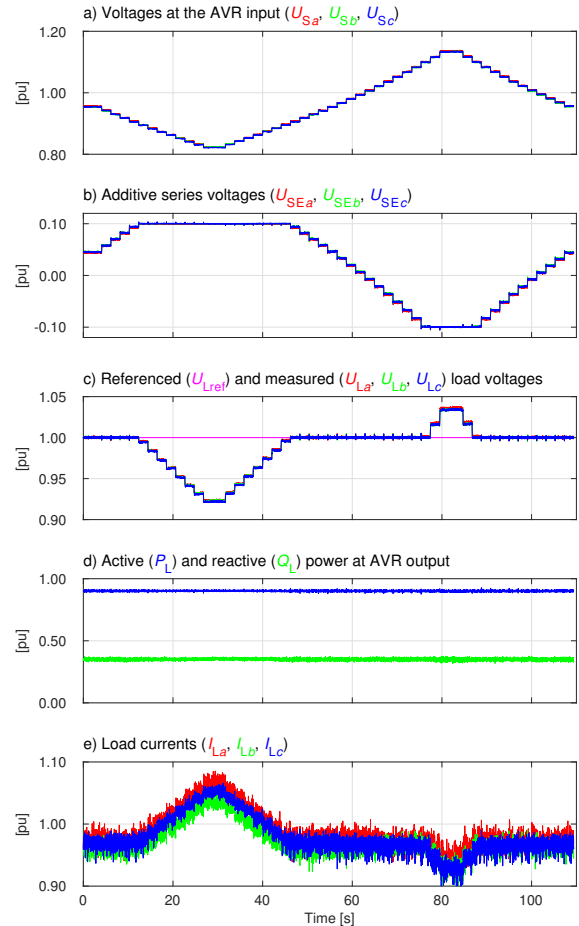


Fig. 12. RMS waveforms during the changes in AVR input voltages while constant power load with $Q_L/P_L = 0.4$

transformer T2. This transformer is equipped with a thyristor on-load tap changer. In this case, a bidirectional AC/DC/AC converter was connected to the AVR output, which allowed:

- transfer of energy to the power grid in constant current mode with power factor (PF) close to -1 (Figure 11)
- energy consumption in constant power mode with $Q_L/P_L = 0.4$ (Figure 12).

In both cases the AVR operates with a load close to its rated capacity, the RMS current waveforms are shown in Figures 11e, 12e and the waveforms of the active and reactive power - in Figures 11d and 12d. Changes of supply voltages are shown in Figures 11a, 12a. In either case, AVR correctly maintains the reference output voltage (Figs 11c, 12c) until the additive series voltages are within $\pm 0.1U_n$ (Figs 11b, 12b). When the differences between output and input voltages exceed the regulating capacity of the AVR, it generates its maximum additive voltage. The obtained results encourage the authors to develop an algorithm enabling the implementation of the physical model of Distribution Transformer with Multi-Zone Voltage Regulation described in paper [24]. The obtained results will be presented in subsequent publications.

C. Case 3 - transient states

The chapter presents selected transients related to:

- changes in the reference value of the load voltage (Figures 13 and 14)
- switching on and off different types of loads (Figures 15-19).

Figures 13 and 14 show the selected transients associated with step changes in load voltages, whose RMS waveforms are shown in Figures 6a and 7a, respectively, the time axis is the same in the corresponding figures. In both cases, the additive series voltages with maximum amplitude must change phase by 180 degrees. Despite the largest possible setpoint changes, the control system reduces the errors almost completely during one period of the mains voltage.

Figure 15 shows the transient state caused by switching on, at nominal AVR output voltage, a three-phase resistive load with a power slightly above rated. Figure 16 shows, at nominal load voltage, the switching on of a symmetrical inductive load of about $0.8S_n$. The control system ensures stable operation of the AVR and reduces the voltage error significantly during one period of the supply voltage.

Figure 17 illustrates the operation of a three-phase load in the form of the three-phase resistor (ca. $0.26S_n$) and a six-pulse diode rectifier with an output resistance (ca. $0.75S_n$) at a load voltage of $1.05U_n$. At time $t = 36ms$, phase *b* of the rectifier supply was disconnected causing a load asymmetry. The change in the value and type of the load causes a slight tran-

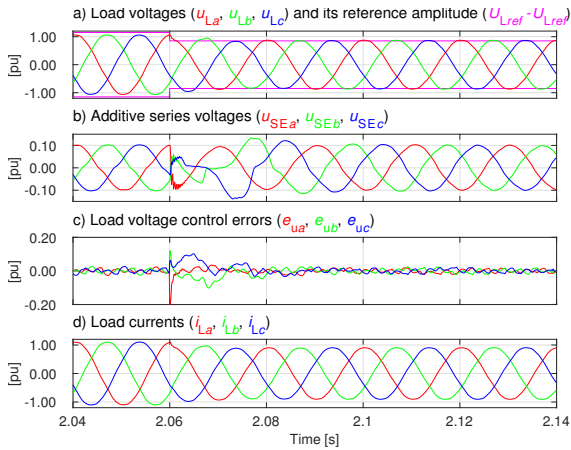


Fig. 13. Step change of the reference load voltage from $1.15U_n$ to $0.85U_n$ under symmetrical three-phase resistive load

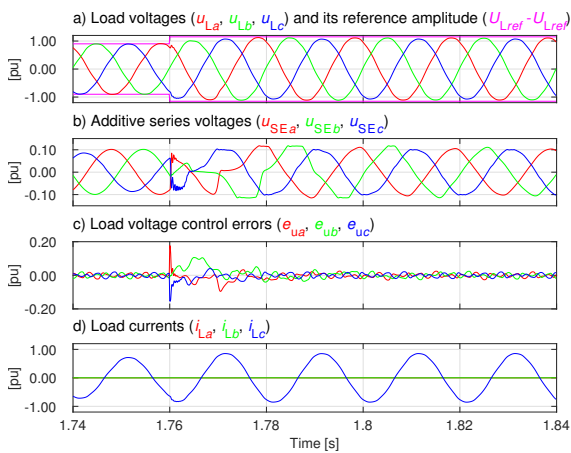


Fig. 14. Step change of the reference load voltage from $0.9U_n$ to $1.15U_n$ under unsymmetrical single-phase resistive load

sient, the output voltage adjustment time is about one period of the mains voltage.

Figures 18 and 19 show the transients related to the soft loading of the AVR output using the power electronic converter systems. Figure 18 presents the termination of energy transfer to the distribution grid and Figure 19 - the beginning of capacitive reactive power generation. In case of gradual change in load on the AVR output the voltage control errors are almost unchanged.

5. CONCLUSIONS

Experimental tests have confirmed correct operation of the AVR for resistive, inductive, capacitive, constant-current, constant-power, nonlinear and asymmetrical loads, as well as in cooperation with generating units transmitting energy to the mains. The AVR described in this paper exhibits appropriate dynamics. The control system significantly reduces the voltage error during half of the period of the supply voltage, regardless of the type of load. The error of the output voltage regulation in the steady state does not exceed 0.2% of U_n . The accuracy of the control is independent of the type of disturbance—whether it's a load change or a generation change. Further development of the AVR is planned in the near future, particularly the imple-

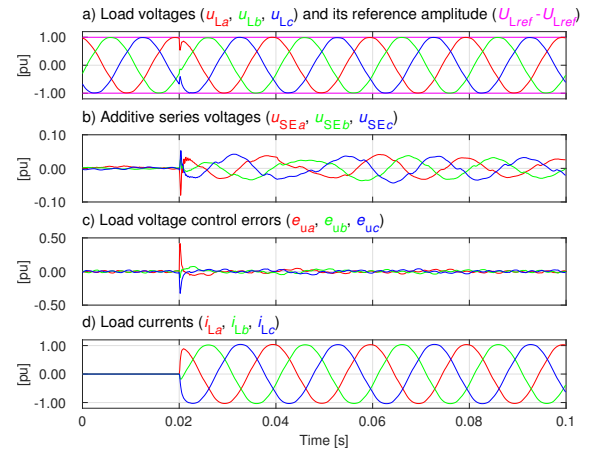


Fig. 15. Switching on a symmetrical three-phase resistive load of about $1.05S_n$ at $U_{Lref} = 1.0U_n$

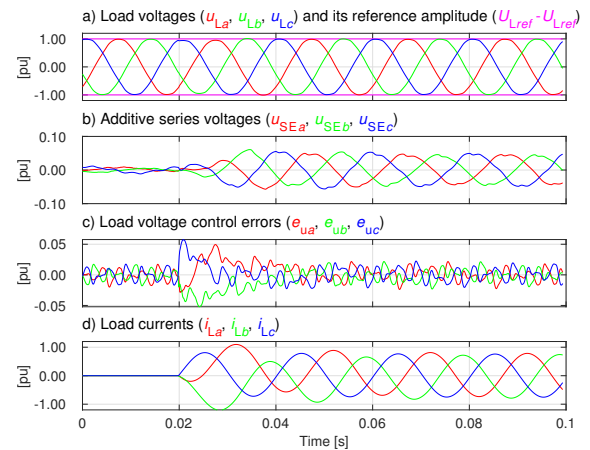


Fig. 16. Switching on a symmetrical three-phase inductive load of about $0.85S_n$ at $U_{Lref} = 1.0U_n$

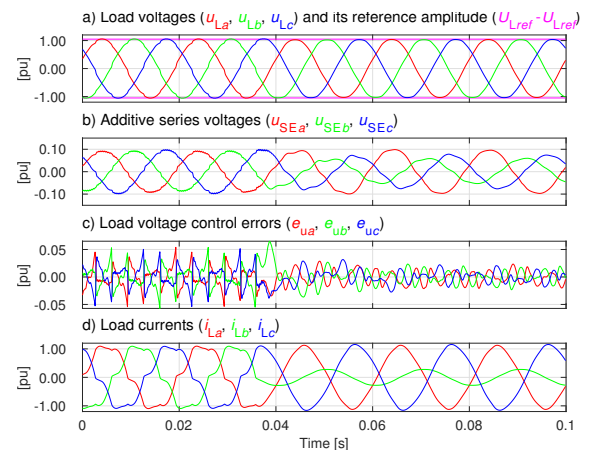


Fig. 17. Disconnection of phase b of the power supply of the six-pulse diode rectifier (ca. $0.75U_n$) during operation of the symmetrical three-phase resistor (ca. $0.26U_n$), $U_{Lref} = 1.05U_n$.

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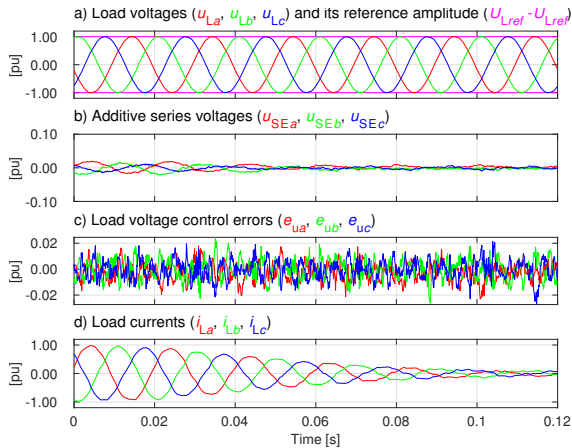


Fig. 18. Switching off the power electronic converter system transmitting energy to the supply network.

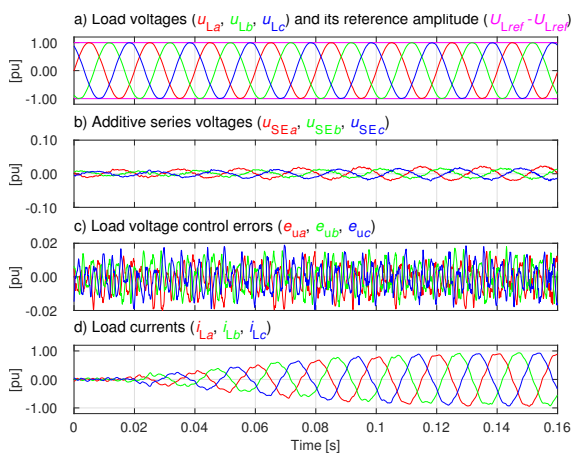


Fig. 19. Switching on the power electronic converter system generating the capacitive reactive power.

mentation of control that will provide compensation for higher harmonics of the output voltage and input current of the AVR, as well as the capability of reactive power compensation.

Research is planned using the AVR as part of a smart grid, which will be supported by the IEC61850 communication protocol implemented in the device.

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