IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 30 August 2024, accepted 26 September 2024, date of publication 1 October 2024, date of current version 10 October 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3471691

APPLIED RESEARCH

Concept of Wireless Low-Voltage DC Socket for the Residential House Application

VIKTOR SHEVCHENKO[1], (Student Member, IEEE),
OLEKSANDR HUSEV[1], (Senior Member, IEEE),
BOHDAN PAKHALIUK[2], (Student Member, IEEE),
DMITRI VINNIKOV[1], (Fellow, IEEE),
AND RYSZARD STRZELECKI[3], (Senior Member, IEEE)

[1]Department of Electrical Power Engineering and Mechatronics, Tallinn University of Technology, 19086 Tallinn, Estonia
[2]Department of Radiotechnic and Embedded Systems, Chernihiv Polytechnic National University, 14027 Chernihiv, Ukraine
[3]Department of Power Electronics and Electrical Machines, Gdansk University of Technology, 80-233 Gdańsk, Poland

Corresponding author: Oleksandr Husev (oleksandr.husev@taltech.ee)

This work was supported by the Estonian Research Council, Postdoctoral Research, under Grant SJD27.

ABSTRACT The proposed research is devoted to the comprehensive theoretical and experimental study of the concept of the wireless low power dc socket for residential applications. The main goal of this work is to provide safe dc source for residential customers at power level which is enough in order to supply all typical appliances without power factor correctors. Such types of devices can be already connected to the dc grid and decoupled from ac grid. This paper considers several typical solutions that can be used for realization. The comparative analysis of an LLC converter with a series-parallel compensation circuit is one of the outputs of this paper. Eventually, simulation and experimental verification is given. The main advantages and constraints are discussed in the conclusions.

INDEX TERMS Wireless power transfer, dc microgrid, series-parallel compensation, LLC converter.

I. INTRODUCTION

One of the greatest problems the world is facing today is environmental pollution and depletion of natural resources [1]. These two problems are interconnected. The use of gas and oil as the main energy sources leads to their complete exhaustion along with environmental pollution with CO2 emissions. The constant growing energy demand of humanity intensifies the problem. At the same time, there is evidence of positive aspects. Humankind is trying to shift the situation. Efforts are made to develop cheaper and more sustainable energy such as solar power, wind power and other forms of Renewable Energy Sources (RESs) that can replace oil and fossil fuels [2].

The political situation exacerbates the problem and push to speed up the transition to the sustainable green energy resources.

Another aspect lies in the direction of pollution reduction by means of using new green technologies in the massive industry. At the same time, a high penetration level of RESs evokes energy system stability and power quality problems.

The solution is to shift the responsibility to the local prosumer. Due to that, in many countries' governments have set strict regulations to the grid energy injection. It consists of the limitation of the injected power to the grid produced by RES in the local households. In particular, the feed-in energy cost of solar systems is declining and is expected to be close to zero in the current decade.

Low Voltage dc (LVdc) distribution grid is seemingly the most obvious solution. Relevance of LVdc distribution is demonstrated by the dc nature of most of RESs, Battery Energy Storage Systems (BESSs), home appliances, and electric vehicles. There are several possible scenarios under consideration.

The first and very simple case when the future house which is equipped by solar panels on the roof, battery, conventional ac sockets and new dc sockets. The dc supply

The associate editor coordinating the review of this manuscript and approving it for publication was Arturo Conde.

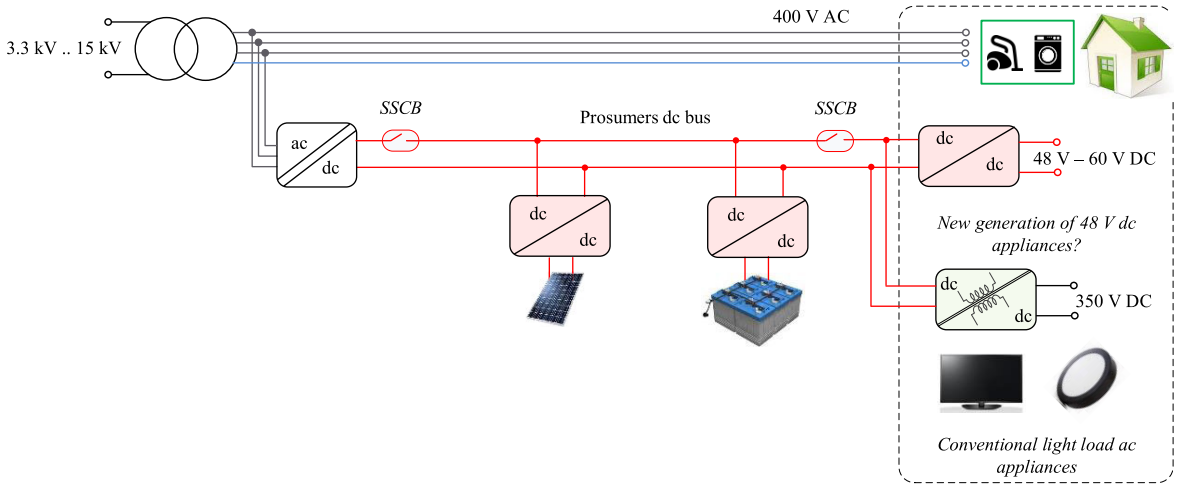

FIGURE 1. Concept of dc nano/micro grid for residential application.

voltage will be provided by using Energy Router that is an internal power electronic device [3], [4], [5], [6]. This device can be considered like low power interlink converter between ac and dc grids. At the same time, in the best case it can cover house consumption, but cannot make global impact on energy generation. The second approach in dc grid realization consists in the external dc microgrid [7], [8], [9], [10], [11].

In this case all power electronics equipment supposed to be connected directly to dc grid including renewable generation and battery storages. This could lead to reduced power electronics stages, higher efficiency, cost reduction, space and weight savings, and flexible placement of electrical equipment [10]. Furthermore, systems will no longer operate at a specific frequency, facilitating control and definition of standards. Also, the dc power experiences lower transmission and distribution losses compared to ac power. This is especially advantageous for transmitting renewable energy over long distances from remote locations to urban centers, as it minimizes energy losses during transport. Figure 1 shows the concept of dc nano/micro grid for residential application.

Both approaches are under the development and have many white spots such as protection, power quality requirements, grounding and overall standardization. But the first one does not require global investment and is more feasible for practical application.

Several scenarios are considering for house application. Despite on that, taking into account developing reference documents for residential dc microgrids do not accept 350 V and higher voltage levels available in the buildings due to the safety reason. Only low dc voltage (up to 60 V) with Type-C socket can be usable inside the building for light loads like led lighting, laptop or cellphone chargers, while for heavy load only ac grid will be available [12], [13]. Such scenario does not consider any higher output voltage levels in the house due to the safety reasons, which limits possible benefits of dc grid implementation. Also, it creates uncertainties for appliances manufactures as the same devices have to be updated to 48 V dc voltage and conventional ac [14].

II. CONCEPT OF WIRELESS DC SOCKET FOR RESIDENTIAL HOUSE

The Wireless Power Transfer (WPT) technique popularity is gradually increasing due to several reasons. First of all, breakthrough technologies in material science and power electronics, such as Wide Band-Gap (WBG) transistors, litz wires or core materials allow reaching high switching frequency operation with low losses. Secondly, the increasing number of electrical appliances with batteries used nowadays motivates to find alternative ways of energy transfer. This type of a charging systems has a number of advantages such as no sparking, no short circuits, no contact resistances, no wear and tear on the electrical contact, and they are unaffected by dirt, dust and water. It makes it attractable for residential application. In this case, all power electronics for low power dc facilities will be realized based on wireless power transfer technology. Isolation of the conduction materials creates the safest way of energy transfer. At the same time, it allows realizing operating at relatively high voltage (350 V) with low conduction losses.

One of the main restrictions of WPT mass implementation is a high cost in comparison to the conventional power supply solutions and relatively narrow range of efficient operation. The first reason is particular important for high power application where price difference becomes a significant obstacle. It is caused by technological issues.

The second reason is caused by low or changeable magnetic coupling coefficient between the receiving and transmitting coils and the quality factor (Q) of the WPT coils [15], [16]. Magnetic coupling is mainly determined by the ratio between the air gap and the size of the WPT coils, in addition, the magnetic coupling coefficient decreases rapidly with misaligned WPT coils. Therefore, large coils

or multiple coils are needed to deal with the variation of the magnetic coupling and to achieve a sufficient misalignment tolerance. Low magnetic coupling leads to significant reactive power oscillation in the primary side. Despite the many different compensation circuits and novel ideas [17], [18], [19], [20], [21], [22], [23], [24] it is not possible to provide distance independent efficient power transfer with single transmitting coil.

For example, in [21] the auto-resonant detection method that continuously ensures optimized soft switching is proposed, but there are no solutions for distance changing issue. In [22] it shown that in practical systems, a load-independent operation point is only an approximation. The output voltage is still affected by the load, obtaining minimum and maximum values under rated load and no-load operation, respectively, which in turns deteriorates performance. Some improvement for distance tolerance can be achieved by extra circuits [24].

Other approaches that have better distance tolerance are reported in [25], [26], [27], [28]. However, all of them has extra coils or at least additional components, that cannot be considered as cost-effective solution.

The alternative way of realization of the dc supply for low power devices using fixed wireless contact terminals. This research work is devoted to the concept of the wireless dc socket that can be implemented in any building. Figure 2 shows possible external look of wireless dc socket for residential house (a) and simplified schematics of possible internal structure (b).

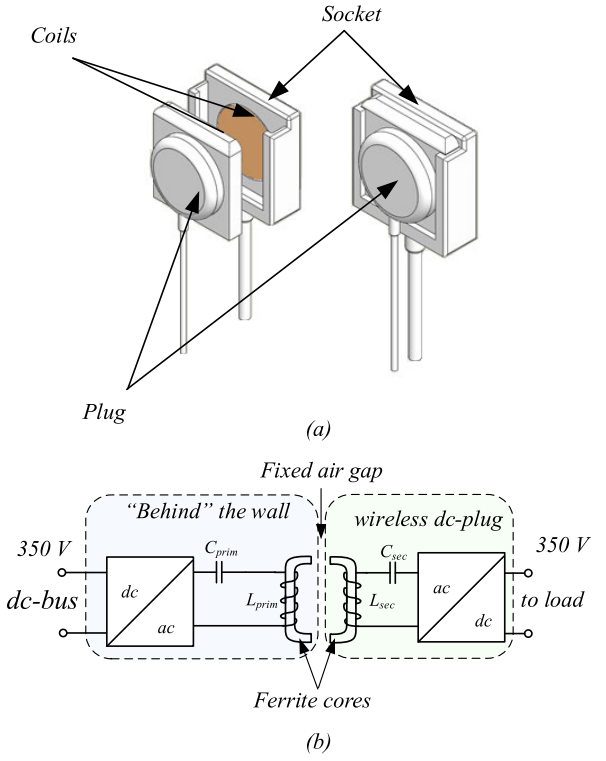

FIGURE 2. Possible external look of wireless dc socket for residential house (a) and simplified schematics of internal structure (b).

This solution will provide safe wireless connection but with fixed distance and position between primary and secondary coils. It will allow utilization of the conventional small ferrite coils on the primary and secondary sides which in turn will help to reduce size, number of turns and increase efficiency. This is especially important in terms of size of the socket. Other requirements that have to be addressed consist of cost minimization and secondary side simplicity. Presence of any active auxiliary components on the secondary side requires extra space and will significantly contribute to the cost.

III. COMPARATIVE EVALUATION OF ISOLATED DC-DC STAGES

In our opinion, different solutions can be used for this concept realization. First of all, even conventional Dual-Active-Bridge (DAB) can be considered for realization [28], [29], [30]. At the same time, due to the low power and minimization of the secondary side size, this solution is omitted for this application. The requirements of active control on the secondary side, which leads to synchronization and presence of auxiliary components makes it not feasible.

Figure 3 shows main solutions that are under consideration. First of all, as we have a fixed air gap, conventional LLC configuration can be considered as competitive solution [33], [34]. Two types of LLC converters are illustrated in Figure 3a and b. Both are classical solutions. The difference is that in case of the full bridge solution, that current is lower as well as voltage stress across resonant capacitor. In the half-bride, the number of semiconductors decreased, but effectiveness of transformer utilization is lower (higher current and higher secondary side turns numbers). Due to this, the full-bridge solution has priory to consider as a possible solution for the dc socket.

CLLC is another resonant solution which is depicted in Figure 3c. From one side can utilize leakage inductance compensation approach like, which means that relatively large magnetizing inductance is required.

| From another side, this circuit can be interpreted conventional inductive power transfer approach with Series-Series (SS) compensation. This approach provides very low value of inductances and Zero Current Switching (ZCS) at nominal power [18], [19].

Another WPT solution is Series-Parallel (SP) compensation approach depicted in Figure 3d. Both SS and SP compensation circuits can be considered. From one side, it was clearly shown that conventional SS is the optimal solution in case of equal voltage level from primary and secondary side [18]. From another side, the SP topology is recommended to be used applications, where a constant voltage transfer ratio without the necessity for feedback control is desired [31], [32].

Despite obvious decision of using inductive power transfer with SS compensation as a basic solution it has some critical

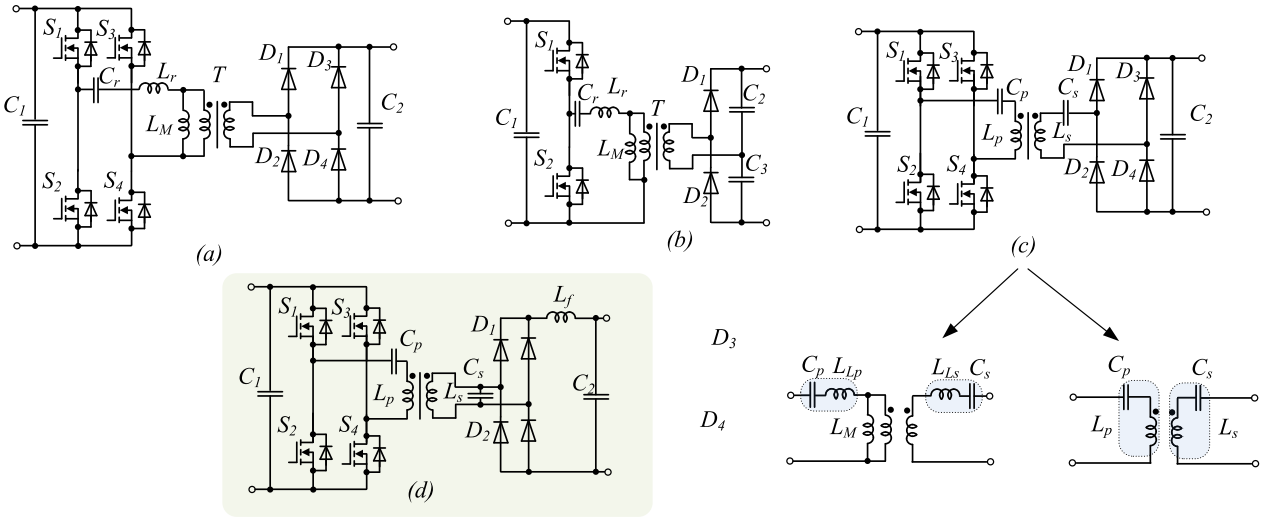

FIGURE 3. Main possible solutions for isolated dc-dc stage: and LLC configuration (a and b), CLLC configurations (c and d).

limitations. SS compensation is independent of the coupling coefficient, and the output current does not depend on the load on the resonance frequency [18], [35] which means that it can be optimized only for very specific operation point. Also, this solution can be quite sensitive to bifurcation problem [36], [37].

As a result, SP compensation is considered as main CLLC option due to the option of keeping constant output voltage without feedback. This section is devoted to the design of the selected CLLC and LLC solutions and its comparative analysis for wireless dc socket realization. Despite on two well-known solutions there are only few attempts to make a direct comparative analysis [38], [39], however, without sophisticated approach and direct conclusion.

A. METHODOLOGY OF COMPARISON

First, the fundamental waveforms of a converter are independent of the selection of components and electric parameters (e.g., switching frequency, selected semiconductors) and result from the basic modulation scheme, yielding some general requirements for the dimensioning of the components.

The fundamental waveforms of both converters along with their simplified equivalent circuits are illustrated in Figure 4.

General requirements include passive components estimation considering the same power level, input and output voltage and the input current ripple and the same voltage ripple.

Assuming the same technology for the same types of components, we can analyze the accumulated energy stored in the transformer and capacitors. In both solutions, the core is going to be utilized in order to increase coupling and reduce the size of magnetics. The volume of the capacitor can be estimated based on its maximum accumulated energy:

$$Vol_C \cong \sum_{i=1}^{N_C} C_i \cdot \hat{v}_{Ci}^2, \tag{1}$$

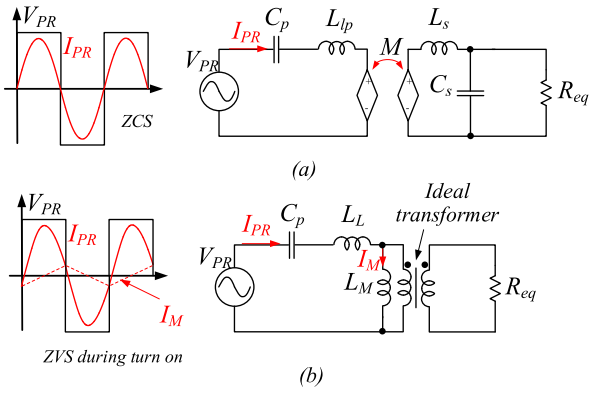

FIGURE 4. Fundamental waveforms and equivalent circuits of CLLC with full compensation (a) and LLC (b) converters.

where Ci is values of i capacitor, is the number of capacitors. v_{Ci} is a peak of capacitor voltage.

The volume of transformer can be estimated based on its maximum accumulated energy as well:

$$Vol_L \cong \sum_{i=1}^{N_L} L_i \cdot \hat{i}_{Li}^2. \tag{2}$$

This approach is used in several research papers and shows good accuracy [40], [41], [42], [43]. At the same time, this approach does not take into account the size of the wires. Which may take significant space in this application taking into account limited space for core and relatively large air gap. This approach provides volume in relative units and is appropriate when the size of wires can be neglected compared to the size of the core, where the energy is accumulated. In this condition, direct calculation and volume comparison of the transformer will be given.

In order to evaluate efficiency, the relative switching and conduction losses that are independent of the selection of

semiconductors will be calculated. First, the relative conduction losses are proportional to the square of the switch current. As a result, total conduction losses can be scaled to:

$$CL \cong \sum_{i=1}^{N_S} \tilde{i}_{Si}^2, \tag{3}$$

where i_{Si} is RMS switch current, N_S is the number of switches. The average value of the product v_{Si} and i_{Si} over a fundamental period T is good measure to indicate the switching losses:

$$SL \cong \sum_{i=1}^{N_S} \left\langle \hat{i}_{Si} \cdot \hat{v}_{Si} \right\rangle_T . \tag{4}$$

In a very general case, we can estimate the total voltage stress across the semiconductors:

$$V_T \cong \sum_{i=1}^{N_S} \hat{v}_{Si}, \tag{5}$$

where v_{Si} is a peak voltage across semiconductor. This parameter is very important and in contrast to the simple number of semiconductors, it may indicate the overall cost of required semiconductors. In this case, this parameter is the same for both solutions and will not be considered.

In a very general case, the voltage ripple factor can be defined for each capacitor:

$$K_C = \frac{v_{C\sim}}{< v_C >}, \tag{6}$$

where $v_C \sim$ is a variable component of the voltage across the capacitor, while $<v_C>$ is the average voltage across the capacitor. Similar statements are applied for the input current ripple factor:

$$K_L = \frac{i_{L\sim}}{< i_L >}. \tag{7}$$

B. CONVERTER DESIGN

Considering the size and efficiency optimization, it is necessary to calculate the minimal values of passive components that are able to provide acceptable input and output power quality. Table 1 summarizes the parameters of the dc wireless socket, including target demands for passive components.

TABLE 1. Parameters of the converter.

Symbol	Parameter	Value
V_{IN}	Input voltage	350 V
V_{OUT}	Output voltage	350 V
P	Maximum input power	100 W
F_{SW}	Nominal switching frequency	85 kHz
ΔI	Maximum input current ripple	20, %
$\mathcal{E}$	Target efficiency at nominal power	95%

Despite on converter similarities, the design approach completely different. In case of CLLC with SP compensation the capacitor belongs to the leakage inductance value, while mutual inductance is defined by coupling and is related with equivalent output resistance and maximum power transfer capability. In case of LLC converter, the resonance capacitor is calculated to compensate leakage inductance, but magnetizing inductance represents transformer and should be maximized.

The LLC converter is initially considered as the frequency-controlled topology. The frequency operating range is selected such that input impedance of the converter always stays inductive, and the current lags behind the voltage. This enables Zero-Voltage Switching (ZVS) on the primary side and Zero-Current Switching (ZCS) on the secondary side, which practically eliminates turn-on losses and minimizes turn-off losses. Using the LLC converter in the correct operating modes is key to realizing these benefits. However, it may not required in this particular application as it will not have feedback loop.

Harmonic analysis shows that the first harmonic represents LLC current very well. The design procedure of the LLC converter is well known. However, different approaches can be used. In our case, we proceed from the fact that coupling coefficient k in our case will be around 0.8, which in turn does not allow to minimize leakage inductance and gives less flexibility in converter design [44]. In particular, quality factor Q can be quite high and is defined as following:

$$Q = \frac{\sqrt{L_R/C_R}}{R_{AC}}, \tag{8}$$

where R_{AC} is equivalent ac load:

$$R_{AC} = \frac{8}{\pi^2} \cdot \frac{V_{SEC}^2}{P}. \tag{9}$$

It should be noted that relatively low coupling $k = 0.8$ is expected due to the gap introduced between secondary and primary side ferrites cores. It prevents operation with a very high quality factor and with high gain factor correspondently. In our case, when the nominal switching frequency and coupling are predefined, the magnetizing inductance should be selected to limit current ripple:

$$L_M \geq N \cdot \frac{4 \cdot V_{pr}^2}{P \cdot \omega_{SW}}, \tag{10}$$

After this, the leakage inductance can be calculated:

$$L_{Leakage} = L_R = k \cdot L_M . \tag{11}$$

It corresponds to the equivalent nominal power P. and the assumption that ripple introduced by magnetizing inductance is at least N times smaller compared to nominal current. The switching frequency is selected according to the typical range of switching frequency for wireless application. The resonance capacitor C_R is selected according to the expected leakage inductance:

$$C_R = \frac{1}{L_R \cdot \omega_{SW}^2}, \tag{12}$$

In order to calculate the output capacitor C_2, the simple methodology for full wave rectifier capacitance calculation can be used [45]:

$$C_2 = \frac{P \cdot \pi}{V_{OUT}^2 \cdot K_C \cdot \omega_{SW}}. \tag{13}$$

In case of CLLC with SP compensation, the calculation takes into account the following parameters. It is mentioned [18] that Load Matching Factor (LMF) for SP topology should be selected according to the nominal coupling k:

$$\gamma = \frac{1}{k} \cdot \sqrt{1 + k^2}, \tag{14}$$

and defined as:

$$\gamma = \frac{R_L}{\omega_{res} \cdot L_S}, \tag{15}$$

where γ – LMF, ω_{res}– resonance frequency, L_S– secondary side self-inductance, R_L – equivalent load, which in turn calculated as:

$$R_L = \frac{\pi^2}{8} \cdot \frac{V_{SEC}^2}{P}, \tag{16}$$

From (15), the secondary side self-inductance can be expressed:

$$L_S = \frac{R_L}{\omega_{res} \cdot \gamma}. \tag{17}$$

The next stage is calculation of the primary-side inductance which can be found from the condition of the gain factor:

$$Gain = \frac{V_{SEC}}{V_{pr}} = \frac{1}{k}\sqrt{\frac{L_S}{L_P}}. \tag{18}$$

Compensation elements should be tuned to the resonance frequency that can be found by the equations:

$$C_S = \frac{1}{\omega_{res}^2 \cdot L_S}. \tag{19}$$

Finally, the primary resonant capacitance is obtained:

$$C_P = \frac{1}{L_P(1-k) \cdot \omega_{res}^2}. \tag{20}$$

In this case with parallel compensation, the output filter is represented by inductor L_f and capacitor C_2. The simple methodology can be used to estimate ripple reduction factor K_r [45]:

$$K_r = \frac{1}{\omega_{res}^2 \cdot L_f \cdot C_2 - 1}, \tag{21}$$

where reduction factor is a ratio between output voltage ripple and voltage ripple before filter. However, with high accuracy the value of inductor L_f can be neglected and capacitor C_2 calculated according to (13).

The calculation results for both cases are summarized in the Table 2. 100 W output power with 1% output ripple is considered for calculation. Taking into account that, simplicity of the concept of dc socket is very important, the load characteristic is very important as well. Figure 5 shows the Bode diagram of both competitive solutions along with output characteristic that correspond to the parameters shown in the Table 2. Figure 5a shows a gain dependance over frequency while Figure 5b shows phase of input current over frequency. Gain dependance shows that output voltage can be regulated

TABLE 2. Values of the passive components.

Symbol	Value	
	LLC	CLLC with SP
C_R	0.94 nF	
L_R	3.6 mH	
L_M	18 mH	1.7 mH
L_P		2.7 mH
L_S		1.7 mH
C_P		6 nF
C_S		2 nF
C_2	0.5 µF	0.5 µF
L_f		0.1 µH

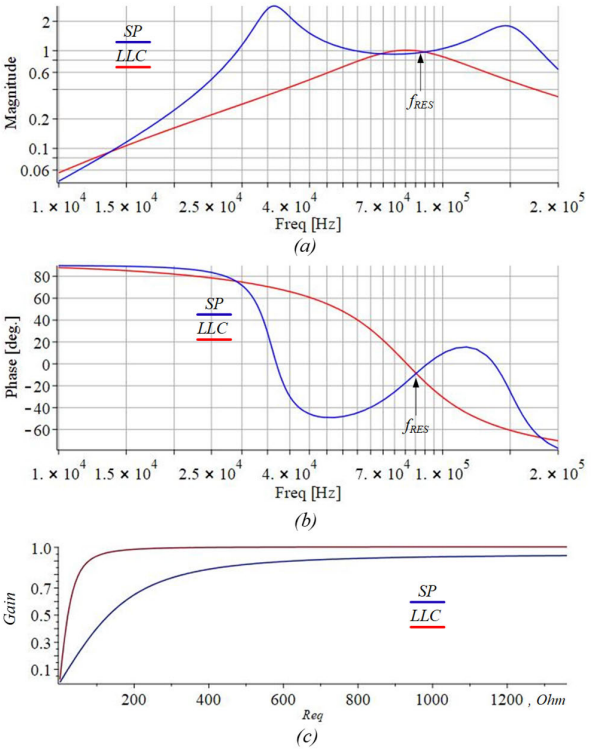

FIGURE 5. Bode diagram of LLC and CLLC converters: gain factor (a), phase of input current (b) and gain dependences over output load (c).

by slight changing of the switching frequency, but what is the most important that in case of CLLC with SP compensation solution that gain can be increased by switching frequency increasing.

From Figure 5b it can be seen that both solutions allow to regulate phase shift of input current. It can be useful for ZVS tuning over ZCS. Eventually, Figure 5c shows the output voltage dependance versus load. It confirms that both solutions provide load independent characteristic.

In order to verify calculation of passive elements, the simulation results are shown in Figure 6. Figure 6a shows the current and voltage waveforms at nominal power and voltage in steady-state mode of LLC converter, while Figure 5b shows steady-state mode of CLLC converter in idle operation mode and reduced switching frequency to 80 kHz. The voltage is slightly higher than nominal 350 V, but still in acceptable range.

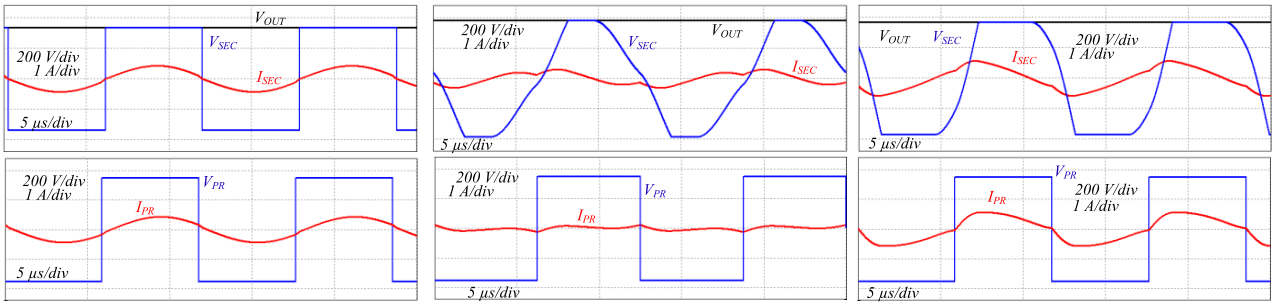

FIGURE 6. Simulation verification: steady state of LLC converter (a) and CLLC converter with SP compensation in idle load operation (b) and minimal load operation (c).

In case of nominal current, the switching frequency increased to 85 kHz, output voltage is 350 V. The current and voltage waveforms are very similar to LLC converter. In both cases, almost ideal ZCS of primary and secondary switches is achieved.

The main conclusion from comparative analysis is that solution based on CLLC configuration with SP compensation is significantly better than LLC solution. However, it should be noted that attempt to provide similar functionality with constant air gap was noticed in [43] and was based on LLC topology.

Despite on similar output filter, current and voltage waveforms, that result in similar semiconductor losses, in our opinion this is not a best solution for dc socket concept realization. LLC topology requires significantly larger magnetizing inductance which may be difficult to realize in case of significant air gap.

At the same time, SP compensation in CLLC configuration provides the same functionality with significantly smaller values of inductances and fixed air gap.

IV. "INDIRECT" CLOSED LOOP CONTROL AND PROTECTION ISSUES

Figure 7 shows the structure of the developed experimental prototype of the dc socket. The cost and feasibility of the concept was a priority in design procedure.

The cost and feasibility of the concept was a priority in design procedure. First of all, there is not any direct closed system control and correspondent feedback signal. It simplifies the secondary side PCB which intended to be integrated in the plug and must be as simple as possible. Presence of output capacitor and diodes that do not require any active control makes this PCB very simple.

At the same time, indirect output voltage control is still needed, and it is realized by input current and voltage measurement. These measurements are realized by simple resistor divider for voltage and shunt resistor R_{SH} and are used for output power control. In case of idle operation (consumption is minimal) the switching frequency is reduced in order to avoid output overvoltage, while it can be increased in case of maximum output power. This concept is implemented in the look up table. Also, the switching is stopped if significant overload detected. In advance, for idle mode operation, the

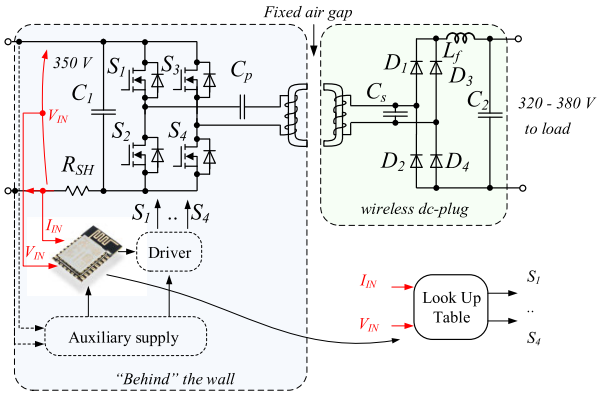

FIGURE 7. Structure of experimentally realized dc socket.

duty cycle of applied primary voltage can be reduced as well and set to maximum when load is detected.

The control itself is realized based on ESP-WROOM-32 unit which provides measurement sensing, switching of semiconductors and communication with external control source by wi-fi. The last component provides smart house functionality. It should be noticed that, as light load devices are considered as the main types of load, such as laptop or cellphone chargers, the direct grounding is not possible. At the same time, it will not create any safety issues. The first reason is that there is no any non-isolated open terminals. Secondly, if even isolation will be destroyed and open contact touched, there is not any risk of high current due to the very high impedance between input dc and output terminals.

Above mentioned overcurrent protection is needed only for shirt circuit case of the output terminals. It is not dangerous for customer, but theoretically can destroy this circuit. However, it is not the case as well, due to the limited value of the output capacitor, and high impedance between input and output terminals. Any shirt circuit on the secondary side will lead to the smooth primary current increasing and overcurrent detection.

V. EXPERIMENTAL VERIFICATION

Table 3 shows the components specification, while Figure 8 shows experimental prototype itself. The primary side PCB (transceiver) has control unit, cheap non-isolated multichannel driver and Si transistors.

TABLE 3. Components of the dc socket.

Parameter	Value
Primary transistors	IPL65R160CFD7
Driver	PG-DSO-28-1
Diode rectifier	IDL02G65C5
Control unit	ESP-WROOM-32
Auxiliary supply	MP9488
L_P, L_S, k	1.1 mH, 0.6 mH, 0.77
C_P, C_S	14 nF, 6 nF
Output filter L_f, C_2	0.1 µH, 0.5 µF

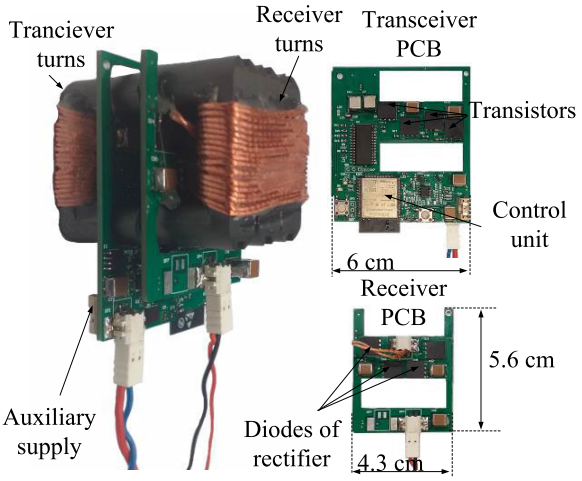

FIGURE 8. Experimental setup of dc socket.

Also, there are ceramic capacitors that play a role of resonance capacitor and input dc-link. Auxiliary supply is realized on simple non-isolated cheap chip and external inductor.

This configuration provides cost effective solution which can be integrated in the wall and been connected to residential distributed dc voltage level at 350 V. Transceiver PCB has a holes for magnetic element which has U-form. When the plug is inserted in the socket, the receiver coils are located opposite to transceiver coils and create a closed path for magnetic flux (left side of the Figure 8). The secondary side PCB (transceiver) has correspondent holes for the second half of U-shape transformer.

It should be noticed, that values of inductances were even lower compare to initially recommended by theoretical calculations and are shown in Table 3. The theoretical guidelines gives the best values to provide the best efficiency, in our particular case, size and number of turns has higher priority.

All the measurement results were obtained by voltage probes Tektronix TPA-BNC, current probes Tektronix TCP0150 and by the digital oscilloscope Tektronix MDO4034B-3. For testing different voltage levels and operating points, Chroma 62150H-1000S power supply was used.

Figure 9 is devoted to the experimental waveform of the presented solution of primary and secondary side with 87 kHz (a) and 83 kHz (b) switching frequency. It shows that experimental waveforms correspond to theoretical expectation. Some nonideality of waveforms is explained by tolerance of real components in resonant circuits.

Figure 9c shows the experimental demonstration of the shirt circuit response. It can be seen, that peak output current exist in this case, and in fact defines by the wire impedance, but overall dissipated energy is very low due to the small output ceramic capacitor. Also, due to the indirect control the transistors keeps switching until input current reaching some maximum value that is predefined in the code. After that, the switching is blocked, and error message can be sent to external control unit.

Figure 10 shows summary of experimental results which includes efficiency and thermal study. It can be seen that the hottest temperature corresponds to the primary side PCB and transistors in particular (Figure 10a). At the same time, the transformer coils are the coldest elements in power path (Figure 10b). Secondary side stage has low losses due to the SiC diodes and ZCS feature (Figure 10c). It means that this solution has significant reserve in terms of possible maximum power increasing.

The main limitation of this experimental setup consists in simplest transistors utilization which is caused by cost-effective solution. Best overall efficiency is about 93 % which includes losses in auxiliary supply (2-3%). Figure 10d shows output characteristics that depend on the load but can be indirectly regulated by switching frequency. Despite that the nominal voltage is equal to 350 V, the acceptable voltage level that is considered as a standard level is between 320 V to 380 V. It means that all dc appliances have to be adopted to this voltage range and our solution matches this expectation.

The switching frequency was also different for different power level where 83 kHz corresponded to idle mode and 87 kHz to maximum load. Finally, losses breakdown analysis is demonstrated in Figure 10e that corresponds to the nominal mode and was obtained by thermal camera with theoretical calculations.

Taking into account the parameters of semiconductors, the theoretical calculations is performed. The MOSFETs with fast body diodes. This is conventional Si CoolMos MOSFETs IPL65R160CFD7 with a fast body diode are utilized. The switching losses are defined as following [46], [47]:

$$P_{SW} = f\left(\left(\frac{t_{DON} + t_r + t_{DOFF} + t_f}{2}\right) \cdot I_D \cdot V_{DS} + \frac{5}{4} \cdot Q_{rr} \cdot V_{DS}\right), \quad (22)$$

where I_D is a peak current of the transistor, V_{DS} is an averaged peak drain-source voltage at the moment of switching, t_{DON} is a turn-on delay time, t_r –rise time, t_{DOFF} – turn-off time delay, t_f - fall time. However, due to the ZCS condition in the nominal mode, these losses are negligible. At the same time, in case of transistors utilizing in ZCS condition power losses are defined by E_{OSS} and E_{QOSS} losses where the E_{OSS} loss is introduced by the capacitance self-discharging current of the switch device itself and E_{QOSS} loss is introduced by the capacitance charging current from the opposite switch

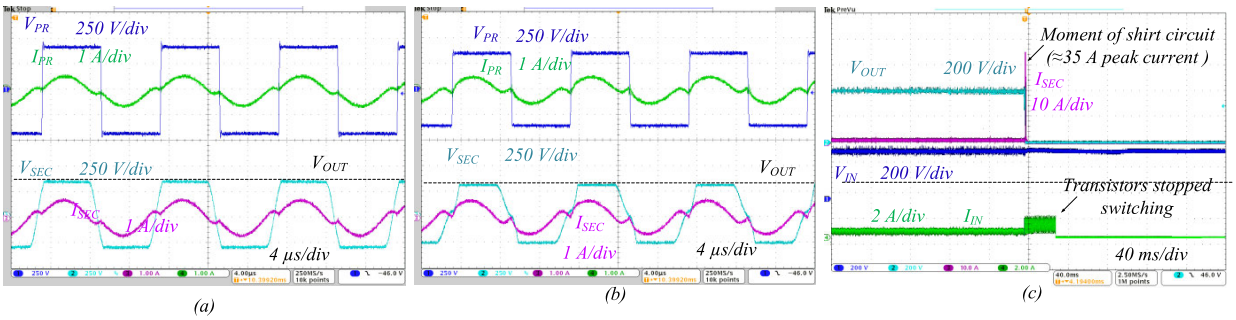

FIGURE 9. Experimental waveforms of primary and secondary side with 87 kHz (a) and 83 kHz (b) switching frequency in case of steady state operation, shirt circuit test (c).

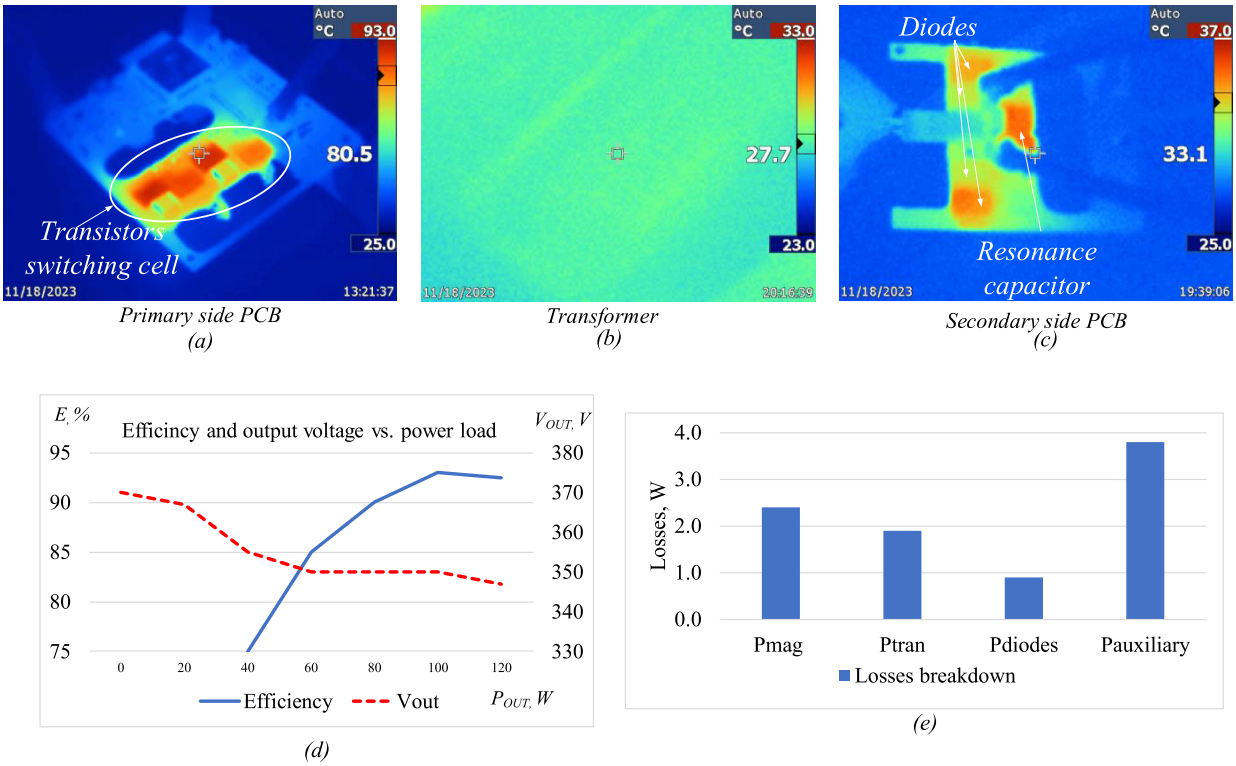

FIGURE 10. Experimental tests of the dc socket: thermal pictures of primary (a), transformer (a) and secondary (c) side PCBs along with efficiency and output voltage dependance versus power (d) and losses breakdown at 100 W (e).

device [48]:

$$P_{OSS} = 4f\left(E_{OSS} + E_{QOSS}\right). \tag{23}$$

Drain-source resistance R_{DS} and primary RMS current I_{RMS} define the conduction losses of the MOSFETs:

$$P_{con} = 2R_{DS}I_{RMS}^2, \tag{24}$$

where 2 means that two transistors are conducting at any moment of time.

Taking into account datasheet parameters of the transistor, the conduction losses are around 0.015 W while P_{OSS} losses are around 1.8 W.

Also, taking into account that secondary side diodes have only conduction losses around 0.8 W, it is possible to conclude that losses distribution shown in Figure 10e corresponds to the overall efficiency and is precisely estimated by thermal camera.

VI. CONCLUSION

This work proposes concept of the wireless low power dc socket for residential application. For this purpose, the comparative analysis of LLC converter with CLLC configuration and SP compensation circuit demonstrated that the approach with SP compensation has smaller size of coils which is critical advantage. Also, approach with SP compensation becomes feasible due to the constant air gap and flat output characteristics. Simulation and experimental verification confirmed all theoretical expectations.

As a result, it provides absolutely safe dc source for residential customers at power level which is enough in order to supply all typical appliances without power factor correctors.

The safety for customer is based on terminals isolation. Even conventional ac appliances without internal power factor corrector can be connected to this type of socket and decoupled from ac grid. Also, this approach can be easily adopted in case of 48 V appliances. In this case, terminals isolation will not an issue anymore.

There are lots of space for further tuning and optimization, in particular in terms of size and shape of the coils and indirect control technique along with utilization of more advanced semiconductors (like SiC or GaN). Further work can be devoted to the readiness level increasing and trade-off analysis between efficiency and cost.

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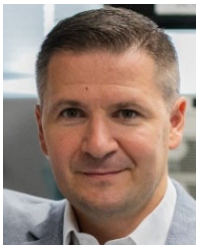
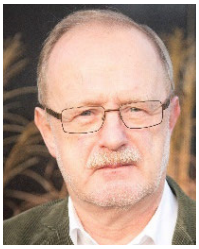
VIKTOR SHEVCHENKO (Student Member, IEEE) was born in Ukraine, in 1990. He received the B.Sc. and M.Sc. degrees in industrial electronics from Chernihiv National University of Technology, Chernihiv, Ukraine, in 2015 and 2017 respectively. He defended the Ph.D. thesis with Chernihiv National University of Technology, in 2021. Currently, he is a Postdoctoral Researcher with Tallinn University of Technology. He has several publications and patents. His area of research interests includes power electronics systems, wireless power transfer, and photovoltaic systems.

OLEKSANDR HUSEV (Senior Member, IEEE) was born in Chernihiv, Ukraine, in 1986. He received the B.Sc. and M.Sc. degrees in industrial electronics from Chernihiv State Technological University, Chernihiv, in 2007 and 2008, respectively. He defended the Ph.D. thesis with the Institute of Electrodynamics of the National Academy of Science of Ukraine, in 2012. He is a Senior Researcher and a Project Leader with the Department of Electrical Power Engineering and Mechatronics, TalTech University. He has over 200 publications and the holder of several patents. His research interests include power electronics systems; design of novel topologies; control systems based on a wide range of algorithms, including modeling, design, and simulation; applied design of power converters and control systems and application; and stability investigation.

BOHDAN PAKHALIUK (Student Member, IEEE) received the B.Sc. and M.Sc. degrees in industrial electronics from Chernihiv National University of Technology, Chernihiv, Ukraine, in 2016 and 2018, respectively. He is currently pursuing the Ph.D. degree (double postgraduate study) with Gdansk University of Technology and Chernihiv National University of Technology. He is a Junior Researcher with the Department of Biomedical Radioelectronics Apparatus and Systems, Chernihiv National University of Technology. His research interest includes design and control converters for wireless power transfer applications.



DMITRI VINNIKOV (Fellow, IEEE) received the Dipl.-Eng., M.Sc., and Dr.Sc.techn. degrees in electrical engineering from Tallinn University of Technology, Tallinn, Estonia, in 1999, 2001, and 2005, respectively. He is currently the Head of the Power Electronics Group, Department of Electrical Power Engineering and Mechatronics, Tallinn University of Technology. He is the Head of research and development and a Co-Founder of Ubik Solutions LLC, Estonian, a start-up company dedicated to innovative and smart power electronics for renewable energy systems. Moreover, he is one of the founders and leading researchers of ZEBE–Estonian Centre of Excellence for zero energy and resource efficient smart buildings and districts. He has authored or co-authored two books, five monographs, and one book chapter; and more than 400 published papers on power converter design and development. He is the holder of numerous patents and utility models in this field. His research interests include applied design of power electronic converters and control systems, renewable energy conversion systems (photovoltaic and wind), impedance-source power converters, and the implementation of wide bandgap power semiconductors. He is the Chair of the IEEE Estonia Section.



RYSZARD STRZELECKI (Senior Member, IEEE) received the Graduate and Ph.D. degrees in industrial electronics from Kyiv University of Technology, in 1981 and 1984, respectively, and the Habilitation (D.Sc.) degree from the Institute of Electrodynamics of the Academy of Sciences of the Ukraine, Kiev, in 1991. His D.Sc. theme was on "Prediction Control of the Self Commutation Power Electronics Converters."

In 1999, he was awarded the title of Professor of technical sciences. Currently, he is a Full Professor with the Faculty of Electrical and Control Engineering, Gdansk University of Technology; and also a Scientific Consultant of power electronics with AREX Ltd. He is the author of over 200 journals and conferences papers and six monographs and 13 patents. His interests focus on topologies and control methods and industrial application of power electronic systems, in particular to improve power quality and power flow control. He was an Elected and Reelected Member of the Committee on Electrical Engineering Polish Academy of Sciences, from 2019 to 2023.