POLITECHNIKA GDAŃSKA

The author of the doctoral dissertation: M.Eng. Dmytro Kondratenko
Scientific discipline: automation, electronics, electrical engineering and space technologies

DOCTORAL DISSERTATION

Title of doctoral dissertation: The pulse width modulation strategy for a five-phase three-level NPC voltage source inverter with DC-link voltage balancing ability.

Title of doctoral dissertation (in Polish): Strategia modulacji szerokości impulsów dla trójpoziomowego pięciofazowego falownika napięcia z diodami poziomującymi z możliwością balansowania napięcia obwodu pośredniczącego.

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Gdańsk, year 2024

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DESCRIPTION OF DOCTORAL DISSERTATION

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Language of doctoral dissertation: English

Supervisor: Arkadiusz Lewicki

Date of doctoral defense:

Keywords of doctoral dissertation in Polish: modulacja szerokości impulsów, PWM, falownik wielopoziomowy, falownik wielofazowy, falownik napięcia.

Keywords of doctoral dissertation in English: pulse width modulation technique, SVPWM, SPWM, multilevel inverter, multiphase inverter, voltage source invertor.

Summary of doctoral dissertation in Polish: Rozprawa doktorska obejmuje opracowanie metody modulacji opartej o założenia modulacji wektorowej, umożliwiającej niezależne formowanie dwóch wektorów napięcia wyjściowego w trójpoziomowym, pięciofazowym falowniku napięcia z diodami poziomującymi. Rozwiązanie znajdzie zastosowanie przy zasilaniu silników pięciofazowych, gdzie powinna być zapewniona możliwość zwiększenia momentu elektrycznego poprzez odpowiednie ‘wstrzykiwanie’ prądu 3ciej harmonicznej. Otwiera też możliwości niezależnego sterowania dwoma silnikami zasilanymi z pojedynczego falownika. Głównymi problemami, które należało rozwiązać tworząc algorytmy modulacji dla wielofazowych falowników trójpoziomowych są: konieczność równoważenia napięć kondensatorów obwodu pośredniczącego oraz zapewnienie możliwości poprawnego generowania wielu niezależnych wektorów napięcia również w przypadku, gdy napięcia obwodu pośredniczącego nie są jednakowe. Proponowane rozwiązanie pozwala na niezależne formowanie napięć wyjściowych przy minimalnej ilości przełączeń tranzystorów, jednocześnie umożliwia sterowanie rozkładem napięcia na kondensatorach obwodu pośredniczącego.

Summary of doctoral dissertation in English: The doctoral dissertation is all about the development of the space vector modulation algorithm for controlling the generation of output voltage vectors in a three-level, five-phase NPC inverter. The developed algorithm can be used to control five-phase motors, where it will be possible to increase the motor torque by 15%; by appropriate injection of 3rd harmonic current. The proposed control approach also opens up the possibility of independent control of two electric motors, supplied from a single inverter. The critical issues that need to be solved when creating pulse-width modulation algorithms for multiphase, three-level inverters are the need to simultaneously balance the input splitting DC-link capacitor voltages and ensure correct generation of many independent voltage vectors. This scenario is also applicable to the case when the DC-link voltages are of different values. The proposed solution paves way for independent syntheses of output voltages with minimum number of active switches’ transitions; while allowing for appropriate voltage distribution on the DC-link capacitors.

ACKNOWLEDGEMENTS

I wish to extend my sincerest gratitude to my supervisor, Professor Arkadiusz Lewicki, for his unwavering dedication, patience, and encouragement throughout my doctoral studies. His invaluable guidance and willingness to share his expertise significantly contributed to the completion of this thesis.

In addition to my supervisor, I am indebted to Professor Marcin Morawiec, Professor Jarosław Guziński, Professor Charles Odeh, and colleagues Mariusz Rutkowski, Robert Dobieglewski, and all other members of the Department of Electric Drives and Energy Conversion for their stimulating discussions and exceptional teamwork during my Ph.D. journey.

I am grateful to the National Science Center for their financial support through the project "Universal vector modulation algorithm for three-level, three- and multi-phase NPC inverters with DC voltage balancing," which facilitated my research endeavors. I also extend my appreciation to the entire staff of the Faculty of Electrical and Control Engineering at the Gdańsk University of Technology, whose assistance was instrumental in the realization of my research project and the completion of my doctoral thesis.

Lastly, but most importantly, I wish to express my deepest appreciation to my parents, Alla and Anatolii, and to Hanna, for their unwavering support, understanding, and belief in me. This work is dedicated to them.

This work was supported by the National Science Centre, Poland, grant 2021/41/N/ST7/01968.

List of abbreviations

AC	–	Alternating Current
ANPC	–	Active Neutral-Point Clamped
APOD	–	Alternate Phase Opposition Disposition
CBPWM	–	Carrier-Based Pulse-Width Modulation
CHB	–	Cascaded H-Bridge
CM	–	Common-Mode
CMV	–	Common-Mode Voltage
CMV-R PWM	–	Common-Mode Voltage Reduction PWM
CSI	–	Current Source Inverter
DC	–	Direct Current
DSP	–	Digital Signal Processor
DTC	–	Direct Torque Control
EMF	–	Electromagnetic Force
EV	–	Electric Vehicle
FC	–	Flying Capacitors
FFT	–	Fast Fourier Transform
FOC	–	Field-Oriented Control
FPGA	–	Field-Programmable Gate Array
GaN	–	Gallium Nitride
IGBT	–	Insulated Gate Bipolar Transistor
IVSVPWM	–	Improved Virtual Space Vector PWM
LS-PWM	–	Level-Shifted Pulse-Width Modulation
MEA	–	More Electric Aircraft
MMDS	–	Multilevel Multiphase Drive Systems
MOSFET	–	Metal Oxide Semiconductor Field-Effect Transistor
MPC	–	Model Predictive Control
NP	–	Neutral-Point
NPC	–	Neutral-Point Clamped
PD	–	Phase Disposition
PI	–	Proportional Integral
POD	–	Phase Opposition Disposition
PR	–	Proportional Resonant
PS-PWM	–	Phase-Shifted Pulse-Width Modulation
PWM	–	Pulse-Width Modulation
RFOC	–	Rotor-Field-Oriented Control
SHEPWM	–	Selective Harmonic Elimination Pulse-Width Modulation
SiC	–	Silicon Carbide
SPWM	–	Sinusoidal Pulse-Width Modulation
SVD	–	Space Vector Diagram
SVPWM	–	Space Vector Pulse-Width Modulation
THD	–	Total Harmonic Distortion
VMW	–	Virtual Modulation Wave
VSI	–	Voltage Source Inverter
VSVPWM	–	Virtual Space Vector PWM

List of symbols

A	–	Clark transformation matrix
C	–	Capacitance of the capacitor in DC-link
$i_{sdq}{}^{I}$, $i_{sdq}{}^{II}$	–	Stator current components in d_1-q_1 and d_3-q_3 coordinates
$i_{s\alpha}$, $i_{s\beta}$	–	Stator current components in α-β coordinates
J	–	Moment of inertia
L_m	–	Mutual inductance
L_r	–	Rotor inductance
L_s	–	Stator inductance
m	–	Modulation index
Q_{actual}	–	Charge delivered to the neutral-point
$Q_{all(max)}$	–	Maximum value of the available charge that can be delivered to the NP
$Q_{x(max)}$	–	Charge, which might be used to balancing the DC-link capacitor voltages and can be delivered to the NP by each of inverter phases
R_r	–	Rotor resistance
R_s	–	Stator resistance
$\boldsymbol{T}$	–	Matrix containing durations of the selected active vectors
T_e, T_L	–	Electrical and load torque
T_s	–	Sample time
$T_{x(N)}, T_{x(O)}, T_{x(P)}$	–	Durations of the 'N', 'O', and 'P' state
$u_{s\alpha}$, $u_{s\beta}$	–	Stator voltage components in α-β coordinates
$\boldsymbol{V}$	–	Coefficients matrix of the utilized active vectors
V_{DC}	–	DC-link voltage
V_{DC1}, V_{DC2}	–	DC-link capacitor voltages
V_{lx}, V_{sx}	–	Long and short virtual vectors
V_{ref}	–	Magnitude of the reference voltage vector
$\boldsymbol{V_{ref}}$	–	Matrix containing reference voltage components
$V_{sdq}{}^{I}$, $V_{sdq}{}^{II}$	–	Stator voltage components in d_1-q_1 and d_3-q_3 coordinates
θ	–	Angle of the reference voltage vector
$\theta_{\Psi sdq}{}^{I}$, $\theta_{\Psi sdq}{}^{II}$	–	Stator flux linkage angles in d_1-q_1 and d_3-q_3 coordinates
$\Psi_{r\alpha}$, $\Psi_{r\beta}$	–	Rotor flux components in α-β coordinates
$\Psi_{sdq}{}^{I}$, $\Psi_{sdq}{}^{II}$	–	Stator flux components in d_1-q_1 and d_3-q_3 coordinates
ω_r	–	Rotor speed

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1. Introduction

1.1. Preliminary discussion

DC and AC electric machines have been integral part that drive our world endeavors; playing prominent roles in the development of the industry. DC motors were originally used in variety of industrial applications due to ease of speed control. In the absence of appropriate control system, AC machines were limited to fixed speed operations. This restricted their deployment in certain applications, despite their several design advantages: absence of brushes, the possibility of working in an explosive or dusty environment, and higher reliability due to the simplicity of the design compared to DC machines. The advent and development of power electronics concepts made it possible to use variable-speed AC machines in industrial applications where operations at variable speed is required. In 1982, DC motors accounted for 8% of all electrical power drives used for variable speed applications, [1]. In recent decades, AC motors have also become widely used in such applications where traditional solutions were based on DC motors. As emphasized in [2], further development of technology will lead to full superiority of AC motors; at least in low- and medium-power industrial applications. In addition to the reliability and simplicity of the design, an important factor is the increase in the efficiency of such drives, [2].

The modern vision of drive systems considers them in terms of cost, size and efficiency of both the inverter and the AC motor. That is why the development of semiconductor switching devices (MOSFETs, IGBTs, SiCs and GaNs) has opened up new opportunities for the industry. MOSFETs and IGBTs introduced in 1963, [3], and 1980, [4], respectively, have become ubiquitous power switches and new models of these switches are designed up to the present day. Two decades ago, advanced technologies in the fabrication of power switches were conceptualized; leading to introduction of SiC and GaN switches. These switching devices offer several advantages: lower resistance and switching losses, the ability to operate at higher frequencies and temperatures, and the potential for reducing the size of designed inverters, [5]. These technologies are still evolving to reduce device costs and address requirements for driver circuits. For example, gate capacitance and inductance must be minimized to achieve faster rise and fall times of the gate voltage, [5].

Presently, several industrial solutions based on SiC and GaN technologies are available on the market. Such inverters can be optimized for any application, and the AC machines themselves are no longer limited by the supply. The supply (the inverter) can be adapted to

specific conditions, for example addition of additional phases. Moreover, in this reigning era of advanced computational system with digital signal processor (DSP) and the likes, complex control systems that could not be implemented before have become widely deployed. These control systems are used to control output voltages and currents generated in voltage source inverters (VSI) and current source inverters (CSI). However, the VSIs are most often used in industrial applications. Typically, these are in applications with three-phase AC motors. However, solutions using increased number of phases (multiphase) are known and widely described in the literature.

The concept of multiphase machines is an interesting solution, especially for high-power systems. First of all, in high-power applications, the limitations in the rated current of semiconductors limit the power that can be delivered. These limitations can be circumvented using multiphase solutions; where voltage remains on the same level, but current (or rather power) can be divided not into 3 but into 5, 6, … phases.

Depending on the stator winding design, multiphase machines have different features. A single multiphase voltage source inverter can be used to supply a single multiphase motor with concentrated windings and quasi-rectangular electromagnetic force (EMF); where the electromagnetic torque can be enhanced by utilizing higher current harmonics, [6], [7], [8], [9]. However, this feature is valid when the phase number is odd. The only known even phase number machine where the torque enhancement is applicable is in an asymmetrical six-phase machine, with a single neutral point, [10]. The electromagnetic torque of a five-phase induction motor can be increased by 15% compared to a three-phase motor. Induction motors with higher number of phases for torque enhancement can use the injection of additional harmonics with order lower than the motor phase number. The 3^{rd} and 5^{th} harmonics can be used for a seven-phase motor; 3^{rd}, 5^{th} and 7^{th} harmonics for a nine-phase motor; and 3^{rd}, 5^{th}, …,13^{th} harmonics for a fifteen-phase motor. The torque increase in 15-phase motor is 20% higher than in three-phase motors, [11]. However, the multiphase motors have problem in the control algorithm complexity. Several independently controlled planes exist (3 planes for 7-phase, and 7 for 15-phase motors) and the number of space vectors which should be considered are high (128 vector for 7-phase, and 32768 for 15-phase two-level inverters). The overall complexity of the control and relatively low improvement in torque enhancement make the five-phase motors the most attractive solution for industrial applications.

Multiphase drives with distributed windings result in sinusoidal electromagnetic force (EMF), and provide the possibility of designing a multi-motor drive system. The same inverter

can independently control several multiphase motors with sinusoidal rotor field distribution and appropriate phase transposition. In the case of a multi-motor drives system, it is possible to control independently, $s=(n-1)/2$ multiphase motors, using an n-phase voltage source inverter; where s is the number of motors and n is an odd number, as mentioned in [10]. Additionally, the torque ripples are lower compared to the three-phase counterparts. The lowest torque ripple component frequency is proportional to $2n$, where n is the number of phases, [10]. Multiphase drives system, where a single VSI is used to supply several motors, can be built using a smaller number of power switches compared to the same number of motors supplied by single three-phase counterparts. The two-level five-phase inverter is made of 10 switches and allows the independent control of two motors; while in the case of three-phase drives, two separate inverters are involved, with a total of 12 power switches. This benefit increases as the number of VSI levels and the number of phases increase. The three-level, five-phase NPC inverter, Fig. 1.1., is made of 20 switches and allows to control independently 2 motors. But in the case of three-phase drives, two three-level inverters with a total of 24 switches have to be used. In the case of seven-phase NPC inverters, a single VSI with 28 switches can replace three inverters with 36 switches. As a result, such drives can be cheaper to produce (the cost of an inverter is reduced, the cost of motors will be the same). This means that such drives have a chance to be popularized in industrial applications. However, the development of the pulse width modulation algorithm for the multiphase VSIs is a complex task and is widely studied [12], [13]. The special motor connection for an independent control is shown in Fig. 1.2. and described in [6].

The multiphase machines with all the stator windings similar have better fault tolerance, compared to the three-phase machines. The multiphase machine remains in operation till more than $(n-3)$ phases become open-circuited; n is the number of phases, [10]. Applications where such machines have much prospectives are in electric cars, railway traction and ships propulsion systems, high-power industrial applications, and 'more electric' aircraft, due to greater reliability offered by multiphase systems, [6], [10]. The use of 5 VSI phases is not limited only to powering AC motors with the same number of phases. They can be used for independent control of dual tree-phase motor drives, where one leg of the inverter is common for both motors, [14].

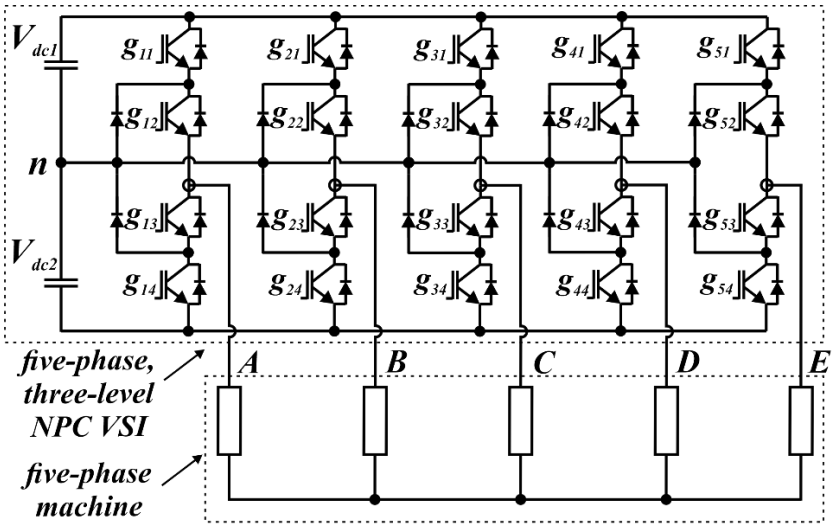
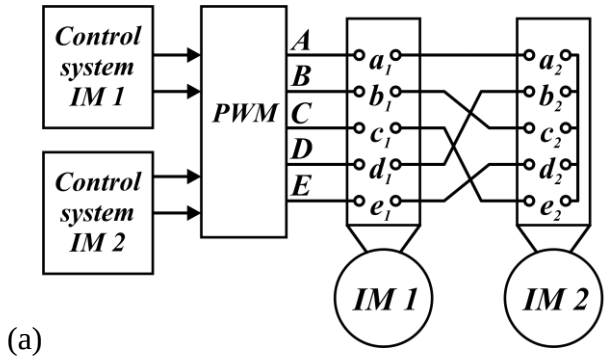
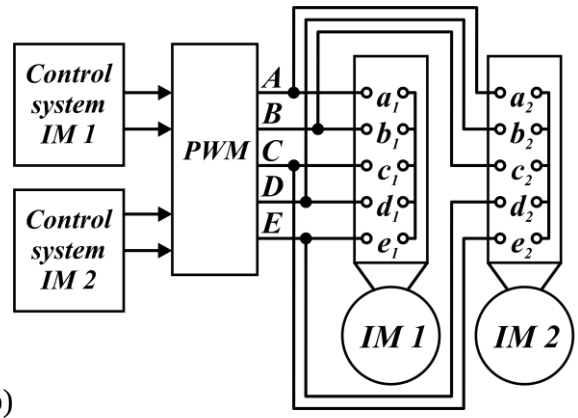


Fig 1.1. Five-phase, three-level NPC inverter power circuit.



(a)



(b)

Fig 1.2. The motors connection of the five-phase dual drive system: (a) serial, (b) parallel.

In VSIs, the output voltage is generated using Pulse-Width Modulation, PWM, techniques. In these modulation methods, two techniques are dominant: the sinusoidal PWM (SPWM), also known as carrier-based (CBPWM), and Space Vector PWM (SVPWM). The concept of SPWM is to compare reference modulating signals with high-frequency triangular carrier signals to obtain the gating signals. Power switches are activated when the modulation signal is higher than the carrier signal. In the conventional SPWM technique, the maximum linear output voltage is equal to $0.5V_{DC}$. In other words, 78.5% of the maximum output voltage of $2V_{DC}/\pi$

is available in the six-step inverter, [15]. The SVPWM method is able to get the maximum linear output voltage of $V_{DC}/\sqrt{3}$; that is, 90.7% of the maximum output voltage, Fig. 1.3.(a), [15]. In order to increase the DC-link voltage utilization in SPWM, appropriate modification can be made in this modulation approach. The most popular are the min-max injection, [16], and the additional harmonic injection, [17]. The harmonic order should be equal to the motor phase number; as an instance, for three-phase motors, 3rd harmonic component should be injected, 5th harmonic for 5-phase, etc. The gate signals generation principles under SPWM technique with 3rd harmonic injection are shown in Fig 1.3.(b). Fig. 1.4. shows the only fundamental frequency component, the fundamental modulation signal after 3rd harmonic component injection and after min-max component injection. Such injection allows the increase to maximum modulation index, from 1 to 1.1547, achieved under SVPWM control for three-phase drive system. Moreover, such injection will not affect the phase currents.

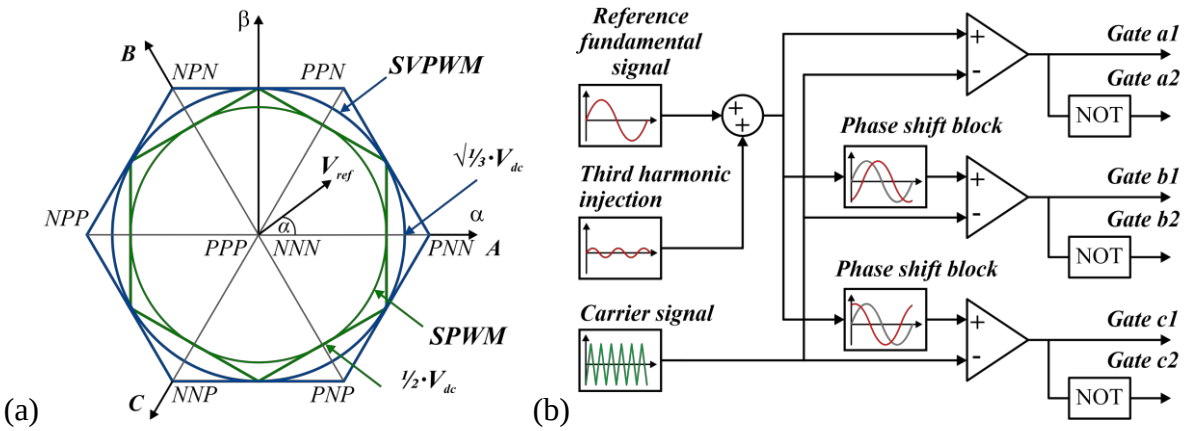


Fig. 1.3. Three-phase two-level inverter: (a) the linear modulation region under SPWM and SVPWM; (b) a gate signal generation under SPWM technique

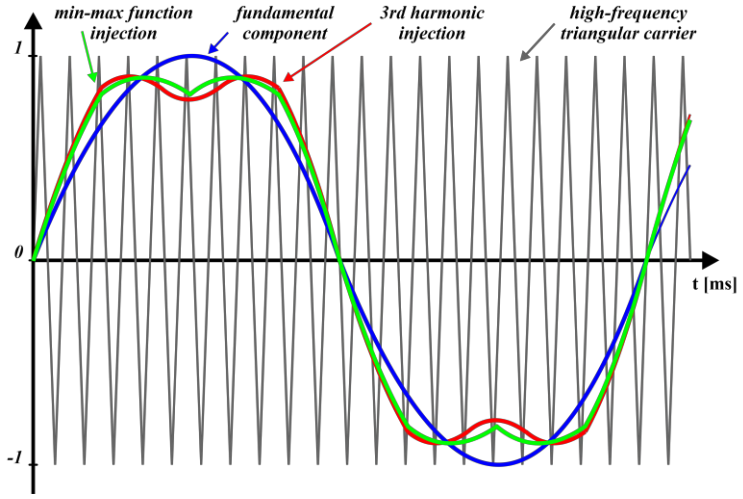


Fig 1.4. The reference and carrier signals in SPWM technique: fundamental harmonic only, with 3rd harmonic and with min-max component injection.

The SVPWM is a natural extension of vector control algorithms. It is deemed superior to SPWM, but considered more complex and therefore less frequently used in industrial applications than SPWM. The problem of implementing SVPWM algorithms is particularly visible in the case of three-phase VSIs with the number of levels greater than 2, as well as in the case of multiphase two level VSIs. In both cases, the problem is the appropriate selection of active vectors. In multiphase inverters, the active vectors defined in many coordinate systems are interdependent. In multilevel VSIs, the selection of active vectors usually bases on the subsector of space vector diagram (SVD), where the reference vector is located. The shape and position of subsectors in the SVD change as the DC-link voltages change. This causes problems with the selection of active vectors. The SVPWM algorithms for multiphase and multilevel inverters combine the above-mentioned problems.

On the other hand, the SVPWM algorithms provide higher maximum modulation index than conventional SPWM schemes. The maximum modulation index of three-phase inverter controlled using SVPWM is 1.1547, that is 15% higher than in conventional SPWM schemes. The SVD for a two-level three-phase inverter is given in Fig. 1.5.

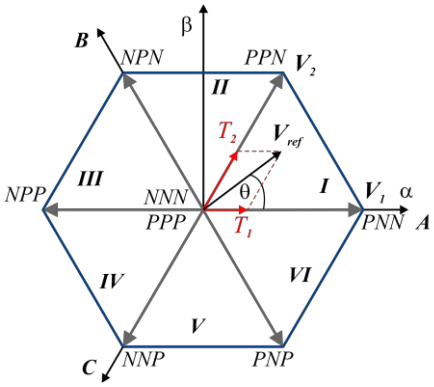


Fig 1.5. Space vector diagram for a two-level three-phase inverter.

In case of three-phase drive system, the voltage vectors form a hexagon that can be divided into six symmetrical sectors, Fig. 1.5. Each sector is associated with a specific combination of voltage vectors. To generate the desired output voltage, SVPWM algorithm calculates the durations of the active vectors. The upper control algorithm (FOC, DTC, etc) delivers the position, θ, and magnitude, V_{ref}, of the reference space vector to be generated. In the case of SPWM algorithms, this reference space vector should be converted to the phase voltages using inverse Clarke transformation.

The SVPWM modulation algorithm can be realized with the following steps:

- The first step is to determine the sector where the reference vector is located.

- Once the sector is located, the durations of the two adjacent voltage vectors are calculated. The activation times are proportional to the magnitudes of the voltage vectors. These are determined based on the volt-second balancing principle associated with the three vectors; two active (**V1** and **V2**) and one zero (**V0**) vectors, and their corresponding times (T_1, T_2, and T_0). When the reference voltage vector is located in first sector, Fig. 1.5., and the DC-link voltage remains unchanged during the duty cycle, the following relationship (volt-second principle) is satisfied:

$$T_s \cdot \boldsymbol{V}_{ref} = T_1 \cdot \boldsymbol{V}_1 + T_2 \cdot \boldsymbol{V}_2 + T_0 \cdot \boldsymbol{V}_0 = T_1 \cdot \boldsymbol{V}_1 + T_2 \cdot \boldsymbol{V}_2; \tag{1.1}$$

where T_s is a sample time, T_1, T_2, and T_0 are the times of the two active (**V1** and **V2**) and one zero vectors, respectively. Sample time T_s can be define as: $T_s=T_1+T_2+T_0$. Such dependencies can be defined in matrix form as follows:

$$V_{DC} \cdot \boldsymbol{V} \cdot \boldsymbol{T} = T_s \cdot \boldsymbol{V}_{ref}, \tag{1.2}$$

$$\text{where: } \boldsymbol{V} = \begin{bmatrix} V_{\alpha 1} V_{\alpha 2} \\ V_{\beta 1} V_{\beta 2} \end{bmatrix}, T = \begin{bmatrix} T_1 \\ T_2 \end{bmatrix}, V_{ref} = \begin{bmatrix} V_\alpha^{ref} \\ V_\beta^{ref} \end{bmatrix} \tag{1.3}$$

So the durations of the active vector can be define in matrix form as follows:

$$\boldsymbol{T} = \frac{T_s}{V_{DC}} \cdot \boldsymbol{V}^{-1} \cdot \boldsymbol{V}_{ref} \tag{1.4}$$

- Next, the switching sequence should be arranged to realize the selected space vector with the determined durations. The sequence with a minimum number of switching in a single sampling period should be chosen to reduce the switching losses. Example of switching sequence for a two-level three-phase inverter is shown in Fig. 1.6.
- Finally, the modulation algorithm utilizes previously obtained switching sequence to calculate the durations of gating signal and to generate the required output voltage.

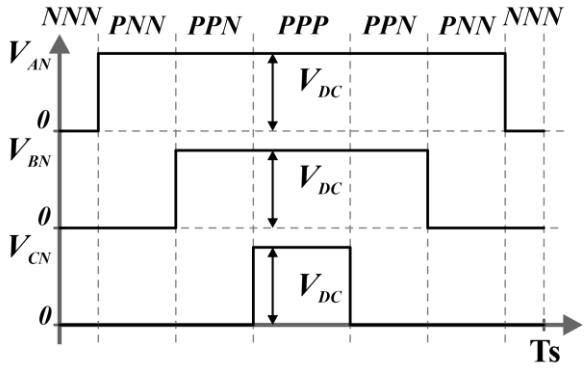


Fig 1.6. The switching sequence for a two-level three-phase inverter.

One of limitations in high power applications is related to the maximum value of the output voltage, as an effect of maximum blocking voltage of semiconductors. This limitation can be overcome by using multilevel inverters. Such converters are mainly used in three-phase applications, [18]. On the other hand, the multiphase drives are most often powered from two-level VSIs, primarily due to the complex control of inverter that is necessary in the case of multilevel configuration. However, combination of the concepts of a multiphase AC machine and a multilevel inverter can be promising in terms of expected results. Such a drive system is characterized by higher fault tolerance, lower requirements for semiconductor devices, lower voltage stress and total harmonic distortion (THD) values, and the possibility of implementing the advanced control scheme for torque increase or independent control of a multi-motor drive. The application of such solutions seems to be the next logical step in the unfolding industrial developments. So, it is natural that this should be an actively researched topic in the scientific environment.

In high power applications, especially in medium-voltage applications, multilevel voltage source inverters are often used. The main advantages multilevel inverters are, [18], [19], [20]:

- Reduced total harmonic distortion (THD), and lower d*v*/d*t* stress, due to the leveling in the output voltage generation.
- Ability to operate with the lower switching frequency, especially needed in medium-voltage and high-power applications. Lower the switching frequency decreases the switching losses.
- The output current is drawn with very low distortion; i.e. enhanced output waveform quality.
- Low requirements for the parameters of motor/grid filters.

- Modular structure can be easily obtained.
- Generated common-mode (CM) voltage is smaller, and the motor bearing stress is reduced.
- possibility of using cheaper power switches with low blocking voltage ratings.

Among the disadvantages of multilevel inverters, the following are noted, [20]–[22]:

- Complex control and modulation algorithms are required.
- The voltage balancing problem have to be solved.
- Undue variation of current stresses on the constituting switching devices in some topologies.

Due to the higher number of switches, capacitors and drivers, the cost of the multilevel topology implementation seems to be higher compared to the two-level inverters. However, taking into account the costs of motor/grid filters and the possibility of using cheaper switches, the total costs may be at a similar level, or even the multilevel VSIs can be cheaper than their two-level counterparts. Therefore, multilevel inverters are an interesting alternative to two-level inverters, even in low-voltage range.

Various types of multilevel inverters are used in industrial applications. The most popular are: neutral-point clamped (NPC) or diode-clamped, flying capacitors (FC), and cascaded H-bridge (CHB) topology, [18], [23]. Active NPC (ANPC), T- type, [24], and F-type, [25], inverters are extension of the diode-clamped inverter topology family. Assuming equal DC-link voltages, the SVD for a three-level three-phase inverter is shown in Fig. 1.7.

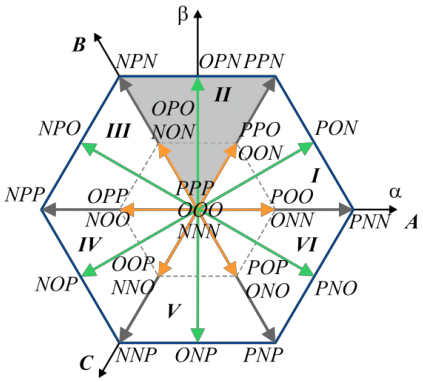


Fig. 1.7. Space vector decomposition for a three-level three-phase inverter.

Two dominant PWMs are used for all types of multilevel inverters: SPWM and SVPWM. Modifications of these can also be used, but they all use the same basic principles, [20], [23]. The selective harmonic elimination (SHEPWM) techniques are a popular approach as well. It suits well in high-power inverters with constant output voltage parameters; where reduction of the switching losses are the main issue to solve, [26]. In the case of CBPWM solutions, the following approaches are used to adapt them to a multi-level inverter: phase-shifted PWM (PS-PWM) and level-shifted PWM (LS-PWM), [23]. The LS-PWM techniques are usually utilized for diode-clamped inverters, the PS-PWM techniques are dedicated for CHB and FC inverters. Due to the nature of these modulation techniques, they are widely used in industrial applications.

The SPWM and SVPWM methods can be used for all types of topologies. However, with an increasing number of output voltage levels, the complexity of the SVPWM algorithms rapidly increases. Fundamentally, the SVPWM algorithm for multilevel inverters has the same structure as an algorithm presented for a two level VSI. But the process for identifying the sectors for multilevel inverters is much more complicated. This is due to the higher number of active vectors and their representation on the orthogonal plane. The number of the switching vectors is defined as l^n, where l is the number of levels in VSI, and n is the number of phases. The main challenge is to select the active vectors correctly despite the changes in subsectors' positions and shapes. The SVD for a three-level three-phase inverter when the DC-link voltages are different is given in Fig. 1.8. The cause of this phenomenon are the changes in DC-link voltages, and, as a result, the subsectors change their shape and positions. Incorrect active vector's selection results in incorrect output voltage generation. This makes the subsector determining process one of the most important parts of the SVPWM algorithm for multilevel inverters. Nevertheless, SVPWM has become widely used in three-level inverters, [20].

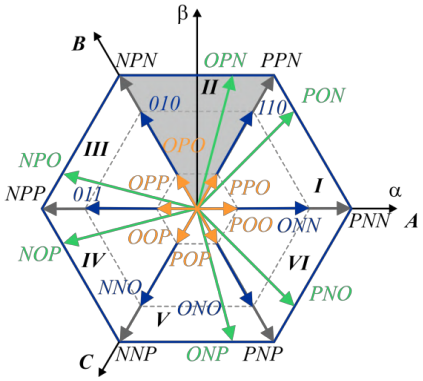


Fig. 1.8. SVD for a three-level three-phase inverter with imbalance in DC-link voltages.

During the last 15 years, more than five hundred articles (572 papers in 2022) were published where the various SVPWM techniques for three- and multi-level VSIs were proposed. Fig. 1.9. shows the number of the articles published per year, available in IEEE Xplore database.

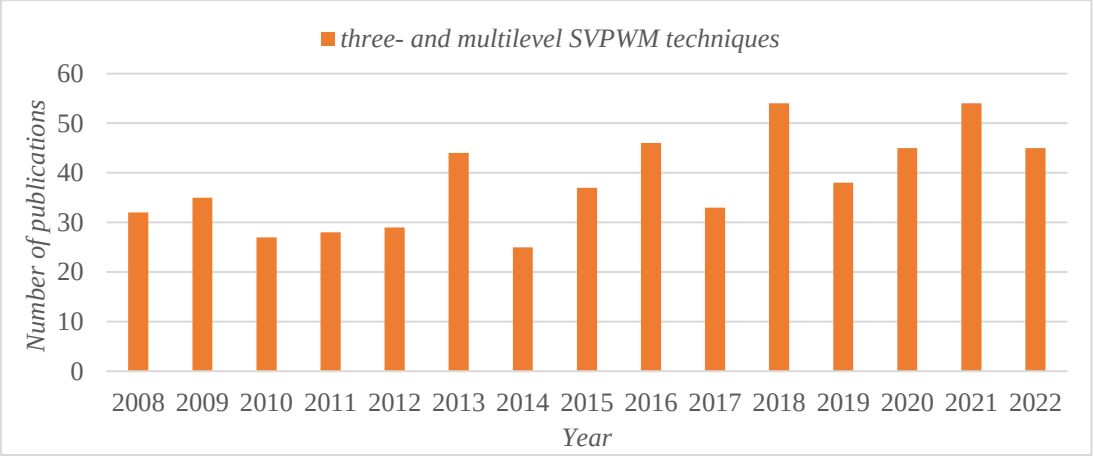


Fig. 1.9. The number of publications about three- and multi-level SVPWM techniques published in IEEE Xplore database, per year.

The researches focused on the DC-link voltages balancing problem, [27], common-voltage elimination, [28], execution time reduction [29], and even the SPWM techniques improvement, [30]. Each of these research topics shows that multilevel, multiphase VSI is an important and attractive topic. A detailed analysis of the existing solutions and inverter topologies is given in the next chapter.

This thesis focuses on the study of low-level control algorithms, such as pulse width modulation (PWM) strategies, for multilevel neutral point clamped (NPC) inverters supplying multiphase machines. The system of a five-phase induction motor and a three-level NPC VSI, Fig. 1.1. is analyzed. It is worth noting that in five phase system, the single VSI is able to control independently two five-phase motors with special connection, shown in Fig. 1.2 and described in [6]; or can be used for supplying the single AC motor with increased torque, [10]. In both cases, two orthogonal coordinate systems have to be analyzed, and (in the first case) two independent voltage vectors have to be generated in a single five-phase VSI.

1.2. Research objectives and originality of the research

The research topic of this doctoral dissertation is the Pulse-Width Modulation Strategy with DC-Link voltage balancing ability for a Five-Phase Three-Level NPC Voltage Source Inverter.

The principal objectives of this research are:

- To examine general principles of CBPWM and SVPWM techniques for inverters with more than two levels and more than three-phase numbers.
- To examine various topologies of the three-level (multilevel, [31]) VSI.
- To develop Space Vector PWM technique for three-level multi-phase NPC inverter.
- To perform a comparative analysis of modulation methods.

The aim of this doctoral research is to carry out original theoretical and experimental research on the SVPWM algorithm for the multiphase multilevel diode-clamped voltage source inverters (NPC and F-Type) with DC-link voltage balancing ability. Additionally, the Sinusoidal PWM technique was compared with the developed Space Vector Pulse Width Modulation scheme.

Referring to the above premises, the doctoral thesis presents the following research hypothesis:

A new universal modulation algorithm based on SVPWM approach for three-level five-phase NPC and F-Type voltage source inverters allows the generation of independently several output voltage vectors as well as balancing the DC-link voltages.

2. Multiphase drive systems

2.1. Introduction

Worldwide attention to the multiphase drives developments concentrates mostly on electric vehicles, EVs (and their hybrids), electrical ship propulsion and the More Electric Aircraft (MEA) concept, as the most perspective application areas, [6]. The reason for this is due to the advantages offered by multiphase drive systems, compared to their three-phase counterparts. The research overview provided in [32] hinged on the best configurations for the multiphase motors, for different areas in aircraft. Authors claim that for MEA applications, multiphase motors are limited to four- or five-phase drive systems. Motors with more than five-phase are overly complex to control and do not offer enough benefits, [32]. Such systems are characterized by low modulation index, *M*, (lower gain in DC-link utilization), at least 2^n space vectors required to control, for *n*-phase system, and -due to higher phase number- the possibility of single line failing increase, [32]. Maximum *M* values are: 1.0515, 1.0257 and 1.0154 for five-, seven-, and nine-phase motors respectively. The modulation index decrease is a consequence of the additional harmonics control in the all the available orthogonal planes. In the case of only fundamental harmonic control, the maximum achievable modulation index are: 1.2311, 1.2518 and 1.2603 for five-, seven-, and nine-phase motors respectively, [33]. However, the control of the fundamental harmonic only results in the presence of uncontrolled high-order harmonics. The *n*-phase motor must be controlled in *(n-1)/2* two-dimensional sub-spaces; which lead to quite complex control/modulation schemes. The odd-phase motors have higher frequencies and lower amplitudes of torque ripples, [34]; while even-phase drives can be utilized for unbalanced magnetic pull compensation when a phase is disabled, [35].

2.2. Modelling and control of multiphase machines

The first comprehensive research review of multiphase machines was presented in [6]. As a brief review, the referred paper showed principles of modelling and control of multiphase drive systems. In [6], a modelling procedure based on the general theory of electric machines was presented. Transformation from original machine model was realized by using a decoupling (Clarke's) transformation matrix, 2.8. This matrix replaces the original sets of *n* variables with new sets of *n* variables; *n* is the phase number. In the decoupling matrix, the first two rows present the variables which will generate fundamental flux and torque. The last two rows present two zero-sequence components; however, in the case of odd phase drives, the last row will be omitted. For a five-phase motor, with two degrees of freedom, the mathematical

model is transformed into two orthogonal planes: α_1-β_1 and α_3-β_3, which are mapped unto the 1st and 3rd planes, respectively.

The mathematical model of the five-phase induction machine was shown in several papers, e.g. in [6] where *n*-phase motors were considered, and in [36], [37], where five-phase induction motor was shown. The mathematical model of five-phase induction motor can be transformed from the natural ABCDE system to two independent orthogonal coordinate systems α_1-β_1, α_3-β_3. The zero-sequence component does not participate in the motor torque generation, so the equations of the five-phase motor for the orthogonal coordinate system are as follows, [37], [38]:

$$\begin{aligned}
\frac{di_{s\alpha}^{(i)}}{dt} &= -\frac{R_s^{(i)}\left(L_s^{(i)}\right)^2 + R_r^{(i)}\left(L_m^{(i)}\right)^2}{L_r^{(i)} w_\sigma^{(i)}} i_{s\alpha}^{(i)} + \frac{R_r^{(i)} L_m^{(i)}}{L_r^{(i)} w_\sigma^{(i)}} \psi_{r\alpha}^{(i)} + \omega_r^{(i)} \frac{L_m^{(i)}}{w_\sigma^{(i)}} \psi_{r\beta}^{(i)} + \frac{L_r^{(i)}}{w_\sigma^{(i)}} u_{s\alpha}^{(i)};\\
\frac{di_{s\beta}^{(i)}}{dt} &= -\frac{R_s^{(i)}\left(L_s^{(i)}\right)^2 + R_r^{(i)}\left(L_m^{(i)}\right)^2}{L_r^{(i)} w_\sigma^{(i)}} i_{s\beta}^{(i)} + \frac{R_r^{(i)} L_m^{(i)}}{L_r^{(i)} w_\sigma^{(i)}} \psi_{r\beta}^{(i)} - \omega_r^{(i)} \frac{L_m^{(i)}}{w_\sigma^{(i)}} \psi_{r\alpha}^{(i)} + \frac{L_r^{(i)}}{w_\sigma^{(i)}} u_{s\beta}^{(i)};\\
\frac{d\psi_{r\alpha}^{(i)}}{dt} &= -\frac{R_r^{(i)}}{L_r^{(i)}} \psi_{r\alpha}^{(i)} - \omega_r^{(i)} \psi_{r\beta}^{(i)} + \frac{R_r^{(i)} L_m^{(i)}}{L_r^{(i)}} i_{s\alpha}^{(i)};\\
\frac{d\psi_{r\beta}^{(i)}}{dt} &= -\frac{R_r^{(i)}}{L_r^{(i)}} \psi_{r\beta}^{(i)} + \omega_r^{(i)} \psi_{r\alpha}^{(i)} + \frac{R_r^{(i)} L_m^{(i)}}{L_r^{(i)}} i_{s\beta}^{(i)};\\
\frac{d\omega_r^{(i)}}{dt} &= \frac{1}{J}\left(\sum_{i=1}^{N} T_e^{(i)} - T_L\right);\\
w_\sigma^{(i)} &= L_r^{(i)} L_s^{(i)} - \left(L_m^{(i)}\right)^2.
\end{aligned} \tag{2.1}$$

where:

R_s, L_s are the stator resistance and inductance respectively,

R_r, L_r are the rotor resistance and inductance respectively,

L_m is the mutual inductance,

$\Psi_{r\alpha}$, $\Psi_{r\beta}$ are rotor flux components in α-β coordinates,

$i_{s\alpha}$, $i_{s\beta}$ and $u_{s\alpha}$, $u_{s\beta}$ are stator current and voltage components in α-β coordinates, respectively,

ω_r is the rotor speed and J is the moment of inertia,

T_e and T_L are the electrical and load torque, respectively,

index i – specify orthogonal coordinate systems α_1-β_1, α_3-β_3, while the index N indicates the number of available planes (2 for a five-phase motor, 3 for a seven-phase motor, etc.)

Induction motors with concentrated windings, and trapezoidal EMF, allow the generation of higher torque by synchronization of both virtual machines, defined in the 1st and 2nd planes. The frequency of the generated voltage in the 2nd plane is 3 times higher than frequency in the 1st plane $\omega_r^{(2)} = -3 \cdot \omega_r^{(1)}$. The resulting torque is the sum of the electrical torques generated in all virtual motors, e.g. for 5-phase motor:

$$T_e = T_e^{(1)} + T_e^{(2)} = \frac{L_m^{(1)}}{L_r^{(1)}}\left(\psi_{\alpha r}^{(1)} i_{\beta s}^{(1)} - \psi_{\beta r}^{(1)} i_{\alpha s}^{(1)}\right) + \frac{L_m^{(2)}}{L_r^{(2)}}\left(\psi_{\alpha r}^{(2)} i_{\beta s}^{(2)} - \psi_{\beta r}^{(2)} i_{\alpha s}^{(2)}\right) \tag{2.2}$$

In case of induction motors with distributed windings and sinusoidal EMF, the 2nd plane can be used for independent control of the second motors. In such drive systems, the generated torques of both motors can be define as, [38]:

$$T_e^{(i)} = \frac{L_m^{(i)}}{L_r^{(i)}}\left(\psi_{\alpha r}^{(i)} i_{\beta s}^{(i)} - \psi_{\beta r}^{(i)} i_{\alpha s}^{(i)}\right) \tag{2.3}$$

The multiphase motors can be controlled using scalar and vector control methods. The field-oriented control (FOC) and direct torque control (DTC) methods utilized in three-phase drive systems were used as a base for researches in multiphase applications. Fig. 2.1. (a) and (b) show the FOC and DTC control schemes for a five-phase drive system respectively. Different control strategies, mostly for asymmetrical six-phase and five-phase induction machines, were analyzed in the recent past. Nevertheless, acclaimed rotor-field-oriented control, RFOC, is the most popular control strategy for multiphase drive systems, [39]. As mentioned in [6], indirect RFOC schemes utilize two types of current control. First one uses (n - 1) stationary current controllers (assuming stator winding with a single neutral point), and the second version of the FOC control scheme has only two current controllers. The second scheme offers an advantage of limited number of the current controllers. The weaknesses of this control method are the need for an appropriate PWM technique and the necessity to include additional controllers. These controllers are essential if there exist any winding and/or supply asymmetries, as mentioned in [6]. Such PWM technique should be implemented to avoid unwanted low-order voltage harmonic creation.

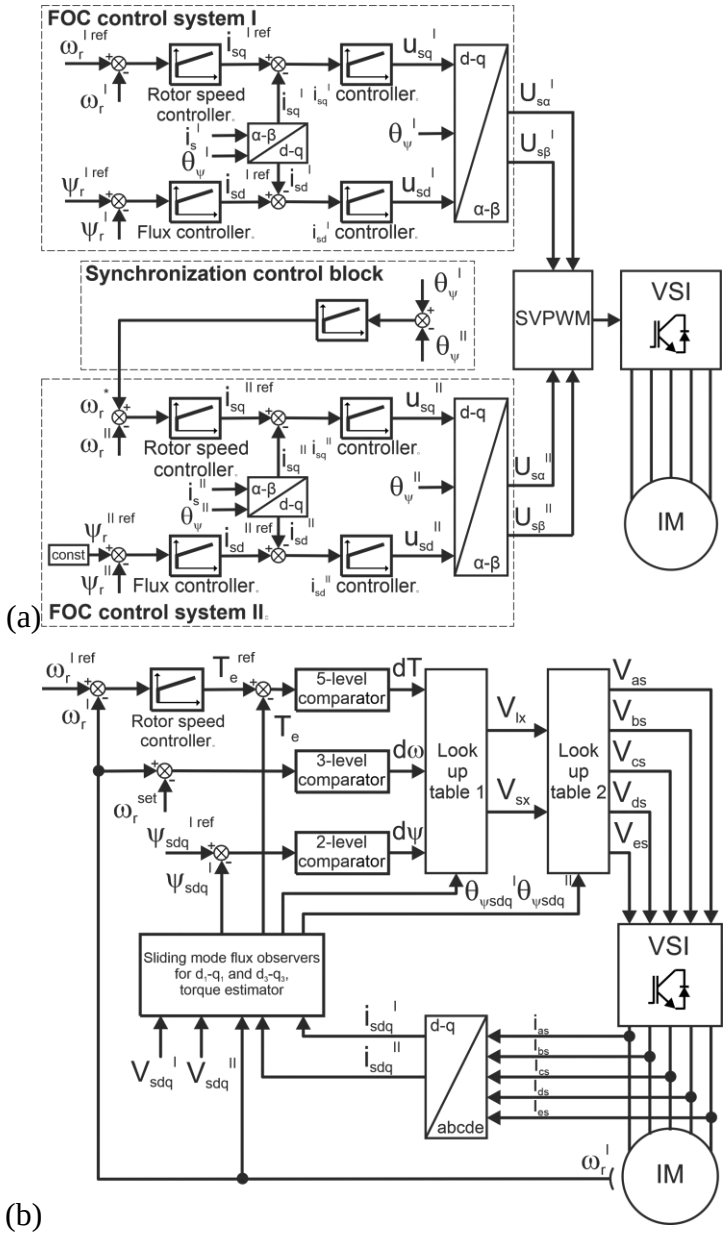


Fig. 2.1. (a) The FOC control scheme and (b) the DTC control scheme for a five-phase drive system.

The direct torque control (DTC) of three-phase drives is one of simplest control methods and can be developed using two different approaches, [40]. The first one, hysteresis stator flux and electrical torque controllers are utilized. The use of these controllers in conjunction with stator voltage vector selection table, result in a variable switching frequency. The second approach utilizes the PWM technique for keeping the switching frequency constant, [40]. Fig. 2.1. (b) shows the classic DTC scheme proposed in [41], where two orthogonal planes d_1-q_1 and d_3-q_3 (marked ^{I} and ^{II} respectively) were involved. The used variables therein are as follows:

Ψ_{sdq}^{I}, Ψ_{sdq}^{II} are stator flux components in *d-q* coordinates,

$\theta_{\Psi sdq}^{I}$, $\theta_{\Psi sdq}^{II}$ are stator flux linkage angles estimated by the d_1-q_1 and d_3-q_3 plane observers,

i_{sdq}^{I}, i_{sdq}^{II} and V_{sdq}^{I}, V_{sdq}^{II} are stator current and voltage components in *d-q* coordinates, respectively,

ω_r is the rotor speed and ω_r^{set} is the low-speed threshold,

V_{lx} and V_{sx} are the long and short virtual vectors respectively, these vectors are defined in the first look- up table. Selected V_{lx} and V_{sx} with angle $\theta_{\Psi sdq}^{II}$ define the inverter switching state and should be chosen in the second look-up table.

As noted in [39], the high-performance DTC control of multiphase machines is much more complicated than in three-phase drive systems. The main reasons are the principles and nature of the DTC control technique. In multiphase motors, there are (*n* - 1) independent currents, so the proper voltage vector selection is important for DTC scheme efficiency. The single voltage vector in each switching period is selected based on flux and torque requirements only; and the excessive non-flux/torque-producing currents result in low efficiency of the DTC scheme, [39].

The FOC, [42], and the DTC, [43] control schemes are the most popular options for multiphase drive system control. Some papers present the multiscalar control, [44] and model predictive control (MPC), [45], schemes. Mostly, these solutions are based on the drive system with two-level inverter, but, recently, various modulation schemes were also proposed for multilevel multiphase drive systems, as well. Different configurations for multilevel multiphase drive systems are a highly researched topics nowadays, [12].

All the control algorithms produce reference voltages in *(n-1)/2* coordinate systems. For motors with trapezoidal EMF, an increase in torque can be obtained by controlling the amplitude of the 3rd harmonic. The synchronization of the reference voltage vector position is easy and can be based on SVPWM technique utilizing 4 active vectors (2 long and 2 medium); where the proportion between these vectors is controlled. In multi-motor drive systems, where IMs with sinusoidal EMF are used, it is necessary to independently control the positions and amplitudes of many reference voltage vectors in all available planes.

2.3. PWM techniques for two-level multiphase inverters

The widely adopted methods for generating output voltages in VSIs are the SVPWM and SPWM. In the traditional implementation of the SVPWM technique, which is commonly

employed in three-phase inverters, the first step involves determining the specific sector, where the reference voltage vector is located. Subsequently, the durations of the active vectors surrounding the selected sector are computed. The SVPWM technique is based on the space vector decomposition approach, presented in [46], [47]. A two-level VSI typically utilizes two active vectors closest to the reference vector and a zero-voltage vector. The DC-link voltage can be optimally utilized if the active vectors are well-chosen. The duration of the active and zero voltage vectors are used to calculate the on-times of the switches in each of the inverter phases.

The CBPWM techniques utilize different approaches to achieve the same DC-link voltage utilization as SVPWM techniques. The most popular are, min-max approach and third-harmonic injection to the modulating signal, for three-phase system. In case of *n*-phase drive system, the *n*-harmonic should be injected to increase the DC-link voltage utilization. The modulation signal is then compared with a high-frequency carrier signal to generate the switching pulses.

In the five-phase system inverter the output phase voltages are described as, [36]:

$$\begin{aligned} V_a &= 0.5 \cdot V_{DC} \cdot M \cdot \sin(\omega t); \\ V_b &= 0.5 \cdot V_{DC} \cdot M \cdot \sin\left(\omega t - \frac{4\pi}{5}\right); \\ V_c &= 0.5 \cdot V_{DC} \cdot M \cdot \sin\left(\omega t - \frac{2\pi}{5}\right); \\ V_d &= 0.5 \cdot V_{DC} \cdot M \cdot \sin\left(\omega t + \frac{2\pi}{5}\right); \\ V_e &= 0.5 \cdot V_{DC} \cdot M \cdot \sin\left(\omega t + \frac{4\pi}{5}\right). \end{aligned} \tag{2.4}$$

where M is a modulation index. The SPWM technique uses these waveforms as voltage references, while the optimal level of the n^{th} harmonic component can be determine as, [17]:

$$V_n = \pm \frac{V_1}{n} \cdot \sin\left(\frac{\pi}{2 \cdot n}\right); \tag{2.5}$$

where: plus sign for n = 3, 7, 11, 15, … and minus for other odd phase number. The modulation signal in five-phase inverter under SPWM with fifth harmonic injector is equal to:

$$
\begin{aligned}
V_a^{ref} &= V_a + V_a^{5harm} = 0.5 \cdot V_{DC} \cdot M \cdot \sin(\omega t) + V_5 \cdot \sin(5\omega t);\\
V_b^{ref} &= V_b + V_b^{5harm} = 0.5 \cdot V_{DC} \cdot M \cdot \sin\left(\omega t - \frac{4\pi}{5}\right) + V_5 \cdot \sin\left(5\omega t - \frac{4\pi}{5}\right);\\
V_c^{ref} &= V_c + V_c^{5harm} = 0.5 \cdot V_{DC} \cdot M \cdot \sin\left(\omega t - \frac{2\pi}{5}\right) + V_5 \cdot \sin\left(5\omega t - \frac{2\pi}{5}\right);\\
V_d^{ref} &= V_d + V_d^{5harm} = 0.5 \cdot V_{DC} \cdot M \cdot \sin\left(\omega t + \frac{2\pi}{5}\right) + V_5 \cdot \sin\left(5\omega t + \frac{2\pi}{5}\right);\\
V_e^{ref} &= V_e + V_e^{5harm} = 0.5 \cdot V_{DC} \cdot M \cdot \sin\left(\omega t + \frac{4\pi}{5}\right) + V_5 \cdot \sin\left(5\omega t + \frac{4\pi}{5}\right).
\end{aligned}
\tag{2.6}
$$

Simplifications of the reference voltages under SPWM with 5th harmonic component injection result in:

$$
\begin{aligned}
V_a^{ref} &= 0.5 \cdot V_{DC} \cdot M \cdot \left[\sin(\omega t) - 0.0618 \cdot \sin(5\omega t)\right];\\
V_b^{ref} &= 0.5 \cdot V_{DC} \cdot M \cdot \left[\sin\left(\omega t - \frac{4\pi}{5}\right) - 0.0618 \cdot \sin\left(5\omega t - \frac{4\pi}{5}\right)\right];\\
V_c^{ref} &= 0.5 \cdot V_{DC} \cdot M \cdot \left[\sin\left(\omega t - \frac{2\pi}{5}\right) - 0.0618 \cdot \sin\left(5\omega t - \frac{2\pi}{5}\right)\right];\\
V_d^{ref} &= 0.5 \cdot V_{DC} \cdot M \cdot \left[\sin\left(\omega t + \frac{2\pi}{5}\right) - 0.0618 \cdot \sin\left(5\omega t + \frac{2\pi}{5}\right)\right];\\
V_e^{ref} &= 0.5 \cdot V_{DC} \cdot M \cdot \left[\sin\left(\omega t + \frac{4\pi}{5}\right) - 0.0618 \cdot \sin\left(5\omega t + \frac{4\pi}{5}\right)\right].
\end{aligned}
\tag{2.7}
$$

The Clark transformation for a five-phase system in the matrix form was given in [6], [37]:

$$
A = \sqrt{\frac{2}{5}} \begin{bmatrix}
1 & \cos(\alpha) & \cos(2\alpha) & \cos(2\alpha) & \cos(\alpha) \\
0 & \sin(\alpha) & \sin(2\alpha) & -\sin(2\alpha) & -\sin(\alpha) \\
1 & \cos(2\alpha) & \cos(4\alpha) & \cos(4\alpha) & \cos(2\alpha) \\
0 & \sin(2\alpha) & \sin(4\alpha) & -\sin(4\alpha) & -\sin(2\alpha) \\
1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2}
\end{bmatrix}
\begin{matrix}
\alpha_1 \\ \beta_1 \\ \alpha_3 \\ \beta_3 \\ 0_+
\end{matrix}.
\tag{2.8}
$$

The angle, $\alpha = 2\pi / 5$, is an angle between successive phases of the stator, as shown in Fig. 2.2.

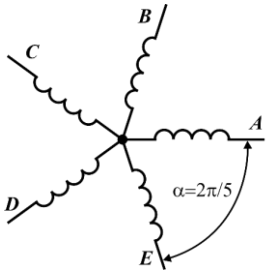


Fig. 2.2. The angle between phases of the stator in the five-phase machine.

In multiphase inverters with SVPWM, the problem of output voltage generation is more complicated. The multiphase inverter must simultaneously generate multiple output voltage vectors defined for many orthogonal systems, [48], as shown in Fig. 2.3. Active vectors of 5-phase VSI create a decagon with ten sectors, where each sector is divided into three subsectors depending on the length of the active vector (Fig. 2.3). Calculation of the durations of the active vector nearest to the reference ones can give the time values greater than a switching period or even negative. This is because in a multiphase VSI all the active vectors are simultaneously defined in many orthogonal planes and all these vectors are dependent on each other, as shown in Fig. 2.3. Therefore, it is not possible to generate the voltage vector in one of the orthogonal systems using two active vectors (as in a three-phase inverter) without simultaneously generating the voltage vectors in the other orthogonal systems. The main problem to be solved in SVPWM algorithms for multiphase VSIs is to indicate the set of active vectors for which non-negative durations will be computed, and also ensure minimum number of switching. If such vectors are found, the next steps are to determine their durations, calculate the on-times for inverter switches and send these on-times to the processor timers that finally generate the gating pulses.

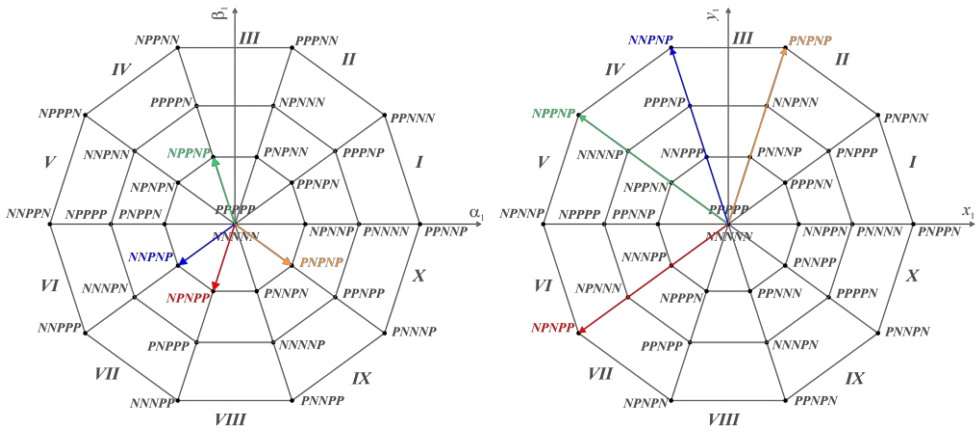


Fig. 2.3. The SVD for a five-phase, two-level inverter and selected active vectors placements in α_1-β_1 and x_1-y_1 orthogonal planes.

The methods for identifying the most relevant active vectors for SVPWM algorithms are complex and time involving. The active vectors may be indicated as the vectors nearest to the reference voltage vectors. If the calculated durations are negative, the next set of active vectors has to be determined, [49], and durations are recalculated. The computational efforts can be reduced if the off-line prepared lookup tables are utilized; where the active vectors are specified for any positions and lengths of reference voltage vectors, [50]. However, this method requires a large amount of processor memory. The proper active vectors can also be determined based on the analysis of additional variables (10 variables predefined for a two-level five-phase

VSI, as proposed in [51]). However, it should be taken into account that the complexity of SVPWM algorithms (as well as the number of active vectors and also the analyzed variables) increases with increase in the number of inverter phases. The number of switching vectors for two-level converters is equal to 2^n, where n is the number of phases.

In SVPWM algorithms, all the vector durations are determined during each cycle of the modulation algorithm using an inverted matrix. This matrix contains components of utilized active vectors specified for each of the orthogonal systems. The matrix inversion must be in each cycle of the modulation algorithm because the selection of active vectors depends on the positions and length of the reference vectors. Condition (1.4) can be used in the three- and multi-phase SVPWM techniques, however, the matrix components, $\boldsymbol{T}$, $\boldsymbol{V_{ref}}$, $\boldsymbol{V}$, are much complex and defined as follows (for a five-phase system):

$$\boldsymbol{V} = \begin{bmatrix} V_{\alpha 1} & V_{\alpha 2} & V_{\alpha 3} & V_{\alpha 4} \\ V_{\beta 1} & V_{\beta 2} & V_{\beta 3} & V_{\beta 4} \\ V_{x1} & V_{x2} & V_{x3} & V_{x4} \\ V_{y1} & V_{y2} & V_{y3} & V_{y4} \end{bmatrix}, \boldsymbol{T} = \begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \end{bmatrix}, \boldsymbol{V_{ref}} = \begin{bmatrix} V_{\alpha}^{ref} \\ V_{\beta}^{ref} \\ V_{x}^{ref} \\ V_{y}^{ref} \end{bmatrix}. \tag{2.9}$$

where: $\boldsymbol{V}$ is the coefficients matrix of the utilized active vectors, $\boldsymbol{V_{ref}}$ is a matrix containing reference voltage components, and matrix $\boldsymbol{T}$ contains durations of the selected active vectors.

This makes the SVPWM algorithms' computationally intensive. Besides, the size of the memory area is significant, since the components of all active vectors specified for all orthogonal systems should be preserved in the processor memory. All these results in the more often implemented SPWM algorithms in multiphase VSIs; which are relatively simple and trouble-free.

Three different types of SVPWM techniques, for two-level, five-phase inverter, were proposed in [52] with the main differences in the type of vectors (short, medium, large) selected for SVPWM synthesis. The first method uses two nearest large vectors which makes this method the simplest, compared to the others presented in [52], and allows to achieve the maximum modulation index. However, the modulation method should be modified due to significant low-order harmonics when only large vectors are used. Two other SVPWM techniques utilize four active vectors (two-medium and two-large) with the appropriate duration giving various shapes of the output voltage (pure-sinusoidal or near-sinusoidal). Modulation technique with pure sinusoidal output voltage allows obtaining 85.41% of the maximum length of the output voltage vector achieved for two large vectors technique. However, the undesirable

harmonics content is significantly lower than in two vector technique. To solve the issue with the maximum length of the output voltage, the near-sinusoidal method was proposed, where the achievable amplitude is equal to the two large vector method, and the undesirable harmonics content remains low.

Opposed to SVPWM concepts, the SPWM operational principle of generating gating signals is inverter phase-leg based. This precisely implies that the same control concept is repeated in each phase of the inverter; the only control parameter difference is the phase angle shift. Consequently, SPWM extension to multiphase systems presents no rigorous and complex computational difficulties, [53].

A comparison between CBPWM and SVPWM was made for a five-phase, two-level VSI in [54]. Analysis of both modulation approaches showed that carrier-based PWM is much simpler to implement, but for a sinusoidal output voltage generation, its performance can be equal to the performance of SVPWM using four active vectors (2 large and 2 medium). The advantages of SVPWM include a better understanding of the switching pattern, and easier control over harmonics, including the elimination of unwanted harmonic components. However, already for the five-phase system, authors have paid attention to the complexity of analysis and implementation for the SVPWM method, [54]. Dependence between two planes is the main complexity of SVPWM techniques for multiphase drives. In such systems, the same active vectors appear in both planes, however, their positions and lengths are different. The large vectors become short and the short vectors become large, while the medium vectors remain unchanged, as shown in Fig. 2.3. This leads to uncontrolled voltage generation in the second plane where only two active vectors will be used, and provides an undesirable harmonic content.

Hybridized SVPWM technique for 2 level VSIs presented in [55] shows the comparable execution time to SPWM modulation techniques. Herein, this technique is utilized as a fundamental platform in the development of this PhD thesis. The solution presented here allows the formulation of a three-level modulation technique with low computational requirements, that avoids additional sub-sector identification procedure.

3. Multilevel power converters

3.1. Multilevel power converters for three-phase drives

Multilevel inverters offer several advantages over two-level counterparts: lower *du/dt* stress, lower output total harmonic distortion (THD). The amplitude of the output voltage generated in ML power converter can be higher than the switches' blocking voltage ratings. The shape of the output voltage is closer to the sinusoidal waveform, so the input and output filter parameter can be reduced significantly compared to the 2-Level inverters, [56].

The most popular ML inverter is the 3-level neutral point clamped VSI. For the first time such a structure was presented in 1981, [57]; where due attention was paid to generation of less harmonic content in the inverter output voltage waveform. In addition, as mentioned in [57], the NPC inverter can be utilized in wide-range of variable-speed drive systems, due to the high efficiency and drive system characteristics. Family of NPC inverters was actively researched during the previous decades. Not only active NPC (ANPC) topology was proposed, T-type and F-type inverter topologies were proposed in [24] and [25], respectively. In terms of control, all these topologies can be controlled using the same modulation techniques, [25]. The main difference is in conduction and switching losses, [25].

The cascaded H-bridge (CHB) inverter was introduced in the late 60s, at the same year as flying capacitor (FC) inverter topology. Decades of development were spent to achieve a commercial solutions for both schemes in early 1990s for FC, and mid-90s for CHB inverter, [20]. These three types of multilevel VSIs become common in industrial applications and still, actively developing.

In paper [18], authors noted that the most popular commercial topologies are three-level NPC, four-level FC, and seven-level CHB. The manufacturers offer the CHB inverters in the nine-, eleven- or even thirteen-level configurations. The next decades were spent developing new topologies for the multilevel power converters or modifying solutions proposed before. Figure 3.1. shows the leg configurations of the most common multilevel inverter topologies.

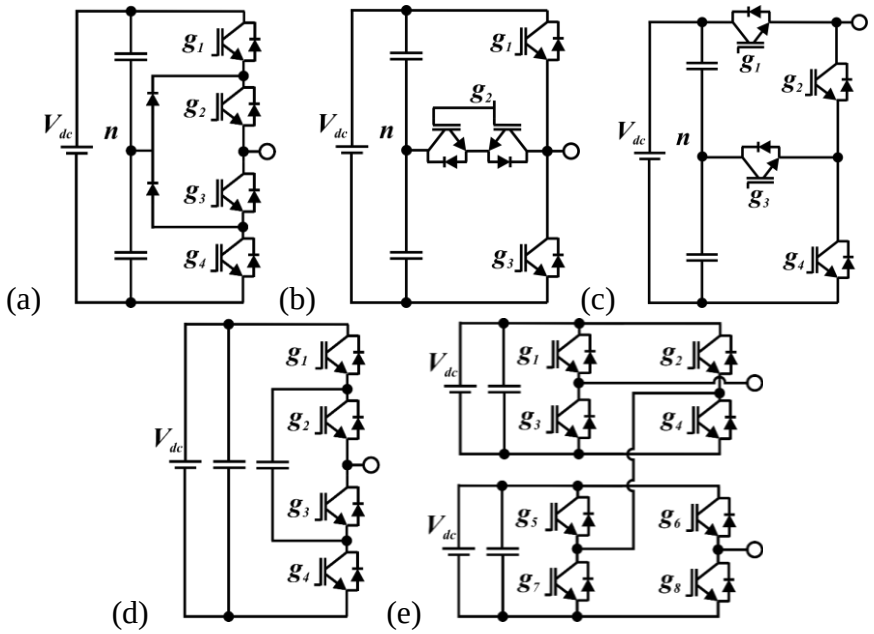


Fig. 3.1. Per-leg circuit configurations of the three-level (a) NPC; (a) T-Type; (a) F-Type; (d) FC; and (e) the five-level CHB inverters.

The idea of the F-type inverter was proposed by our research group in [25]. The F-type inverter reduced the switches' voltage stress, when compared to the T-type inverter. This feature is obtained by reducing the number of switches which have a full DC-link reverse blocking voltage rating. In the three-level F-type inverter, only one switch per leg must be rated at full DC-link voltage (25% of the switches per phase).

Figure 3.2. shows the switching sequence for the one phase-leg of the three-level F-type inverter. In Fig. 3.2. (a), (b) and (c), (d) the sequence transition I, II, III ensure natural commutation of the phase current in both directions, for the transition from positive potential, 'P', to neutral, 'O', and from 'O' to 'P'. The switching sequences for transition from negative potential, 'N', to neutral, 'O', and from 'O' to 'N' are shown in Fig. 3.2. (e), (f) and (g), (h), respectively. Moreover, the F-type topology allows for the identical modulation/control concept utilization as in 3-level NPC and T-Type inverters, [25]. Considering the switches' positions and the switching sequences from Fig. 3.2, it might be concluded that modulation techniques developed for NPC inverter can be used in the F-type inverter after the following modifications:

$$\begin{aligned} &G_{x1F-Type} = G_{x1NPC};\\ &G_{x2F-Type} = !G_{x1F-Type} = !G_{x1NPC};\\ &G_{x3F-Type} = G_{x2NPC};\\ &G_{x4F-Type} = !G_{x3F-Type} = !G_{x2NPC}; \end{aligned} \tag{2.10}$$

where x – is a phase number (*a, b, … , n*).

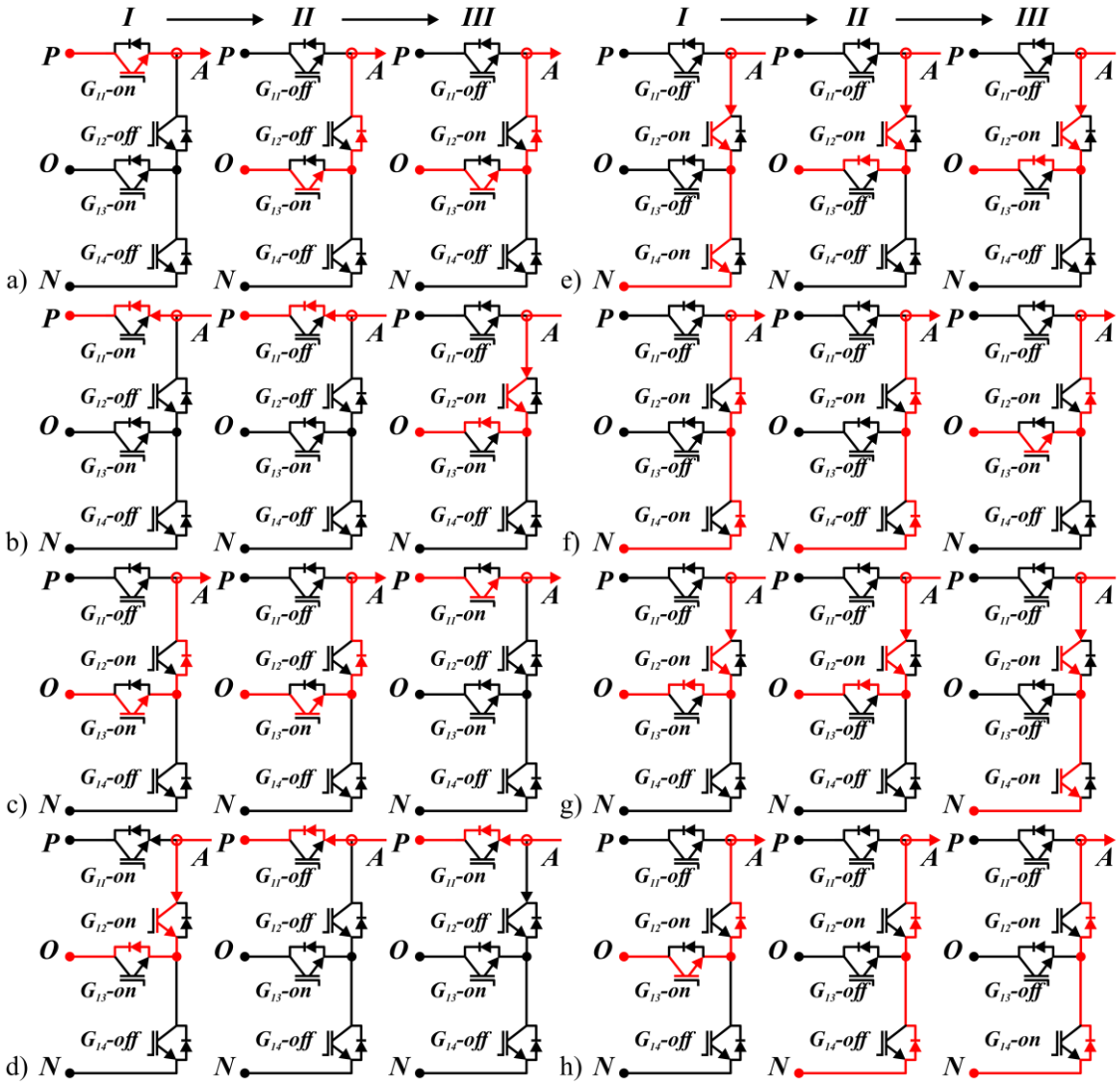


Fig. 3.2. Phase-leg currents transitions during the switching transition for different potentials: Positive, ‘P’, to Neutral, ‘O’: a) positive and b) negative; ‘O’ to ‘P’ c) positive and d) negative; Negative, ‘N’, to Neutral, ‘P’, e) negative and f) positive; ‘O’ to ‘N’ g) negative and h) positive currents.

The analysis shown in [25] prove that the innate topological features of the three-level F-type VSI reflects in lower losses and cost of the inverter for low- and medium-voltage applications. Moreover, the conduction losses, when compared to NPC and the T-type inverters, have been greatly reduced, (only 16.15% of the NPC conduction losses, [25]).

The main advantages of multilevel inverters are the improved quality of voltage waveforms and an increase in the output voltage for a low blocking voltage rating of the semiconductors. Fig. 3.3 shows the two- and three-levels output line-to-line voltage. These types of inverters can be utilized in medium-voltage as well as in low-voltage applications (usually reserved for two-level inverters). On the other hand, such inverters need to control the DC link voltages. The

lack of such control may damage the inverter as a result of exceeding the blocking voltage rating of the semiconductors or the rated voltages of the capacitors.

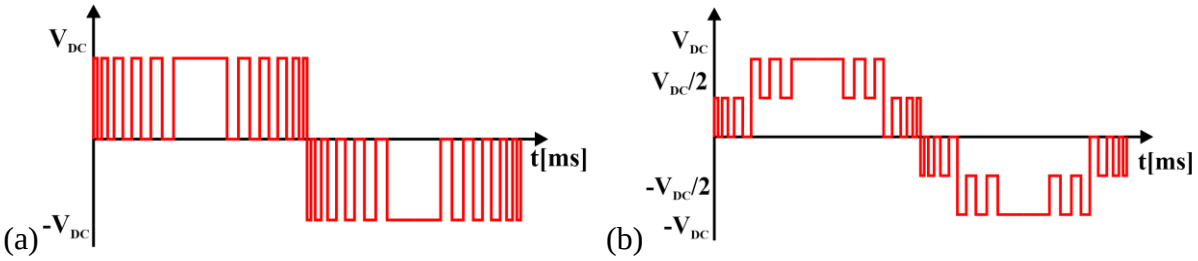


Fig. 3.3. The output line-to-line voltages for: a) two-level b) three-level inverters.

3.2. PWM techniques for multilevel, three-phase inverters

In the last decades the PS-PWM and LS-PWM techniques are widely researched, and different modifications of the PS-PWM, [58]–[60], and LS-PWM [61], [62] were presented. [63] proposed a PWM method which is a combination of both. The PS-PWM techniques associate each cell of CHB and FC with a pair of carriers. The phase-shift between carriers for the different cells in one inverter-leg is used to generate the stepped waveform due to the introduced asynchronism. The advantage of such a technique is that the power is evenly distributed between the cells throughout the modulation index. This approach allows the correct operation of the CHB inverter and the natural balance of the capacitors in the FC, [20]. The main disadvantage of the PS-PWM approach is a relatively high content of undesirable harmonics. The phase-disposition (PD) modulation technique was proposed to solve this problem, which is superior in comparison to the PS-PWM in a voltage harmonic characteristic; however, the high-frequency harmonic content is not different much, [64].

The LS-PWM techniques can be divided into several categories as well:

- phase disposition (PD), where all carriers are in phase;
- phase opposition disposition (POD); where the relationship depends on a sign. A certain phase of carriers when they have positive values and with opposite phase for negative values;
- the alternatively in opposition disposition (APOD), with carriers that alternatively change phase.

The carriers' position for different multilevel SPWM techniques are shown in Fig. 3.4.

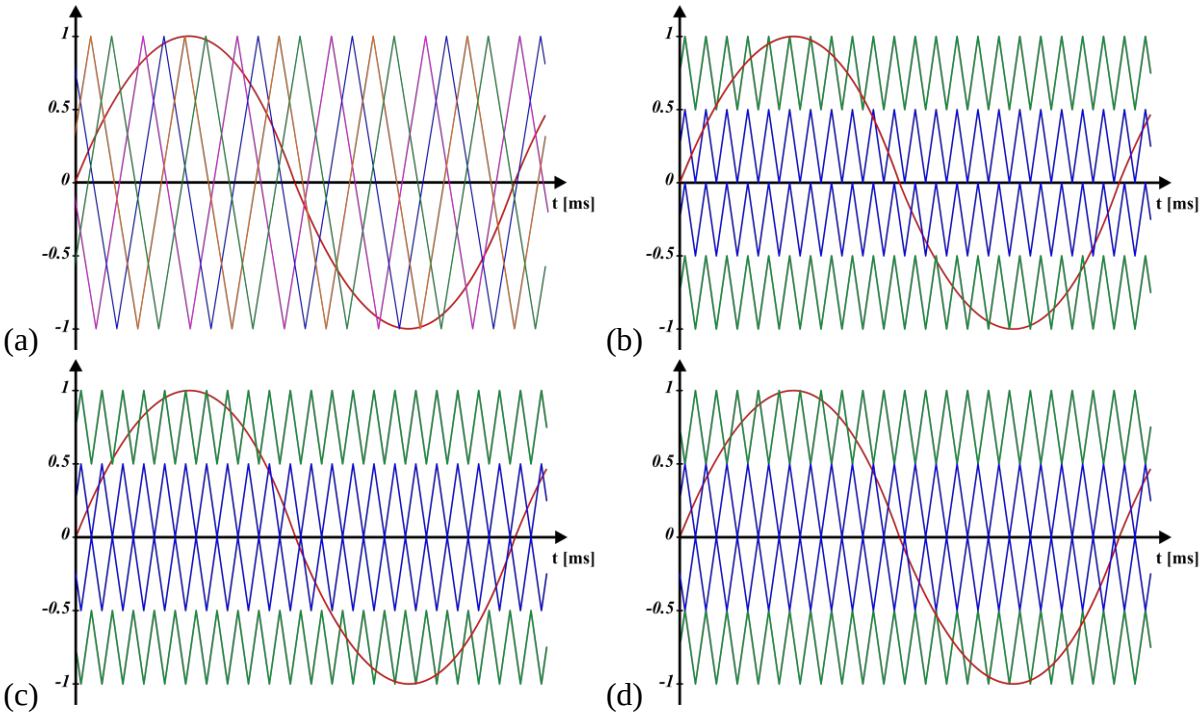


Fig. 3.4. The carriers' position for (a) PS- (b) PD- (c) PO- (d) APO-PWMs.

Some of the papers deal with multicarrier PWM techniques; these researches are based on analytical solutions presented in [65], [66], where the 2-D Fourier approach was presented. In [67] a detailed analysis of SPWM techniques was presented. Modulation methods were analytically compared using the 2-D Fourier approach. Analyses were done for single- and three-phase systems with spectrum calculation for a single inverter leg. The work in [64] proves that NPC and CHB inverters have comparable harmonic performance.

Various modifications of the SPWM technique for three- and multilevel three-phase inverter were presented as well. Such modifications were proposed to increase the effectiveness of the existing SPWM techniques [68], [69]; simplify existing methods, [70]; or optimize the calculation by a neural network implementation, [71]. The DC-link voltage balancing problem was discussed in [72] where an additional balancing algorithm was proposed. Several papers provide comparative studies between SVPWM and equivalent SPWM, [73], [74].

In [70], the simplified SPWM technique for a three-phase three-level inverter was proposed. The modulation index is equal to that of SVPWM, that was achieved by the common-mode voltage (CMV) injection. Compare to the conventional solutions, authors proposed to calculate the CMV value based on two independent terms, [70]. First term is a conventional min-max equation for two-level modulation, while the second is an independent form modulation index and depends only on the sign of the reference voltage. The main advantages of the PWM technique proposed in [70] are a short computation time and an easy implementation; however,

voltage balancing problem was not discussed. [71] proposed a modulation technique based on feedforward neural-network; it showed better results, compared to conventional SPWM for a three-level NPC inverter, with LCC filter only. Lower switching losses and lower phase-voltage THD value were achieved after applying the LCC filter. Without LCC filter, the obtained THD value is better under conventional SPWM technique. Additionally, authors did not compare the computation time of both methods, as well as the DC-link voltage balancing issue.

In [73], the relation between SVPWM and SPWM was investigated and a SFO2-PWM (second type of switch frequency optimal PWM) was proposed. The SFO2-PWM is a combination of the space vector PWM for a three-level and sinusoidal PWM for a five-level inverter. The advantages of this approach are: lower THD value compared to conventional SPWM and similar complexity as SPWM. Fig. 3.5. shows the conventional and proposed SFO2-PWM modulation signals. The weakness of the proposed technique is the absence of the DC-link voltage balancing algorithm which provides additional limitation for industrial applications.

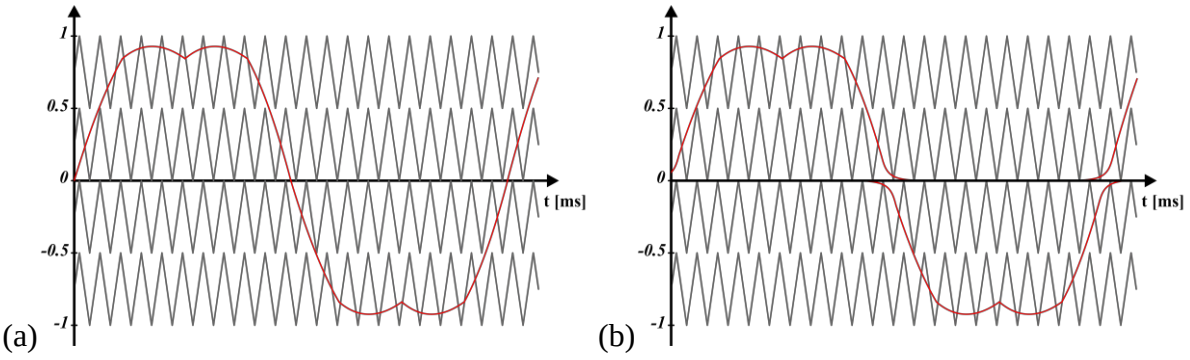


Fig. 3.5. The modulation signal for (a) sinusoidal PWM (conventional SFO) (b) SFO2-PWM.

In [74], the authors presented a relation between SPWM and SVPWM, and proposed an idea of virtual modulation wave (VMW). The VMW was used in the proposed special SVPWM sequences (SSVMS) modulation scheme which is a combination of sinusoidal and space-vector modulation techniques. The SSVMS is equal to the SPWM with zero component injection, where the injected component was calculated using the VMW concept. Proposed approach achieved lower THD than conventional CBPWM with zero component injection. However, the number of switching is higher, which leads to higher switching losses.

In addition to the modified sinusoidal PWM techniques, a high number of non-sinusoidal modulation techniques were presented in the last decades, [75]–[77]. Nevertheless, none of these modulation approaches made it in the industrial arena. This is due to the simplicity and

proven of the well-known sinusoidal modulation scheme, [20]. In spite of that, more and more schemes and methods were developed, using additional degrees of freedom, more voltage levels, reducing common-mode voltage to zero, switching-state or voltage-level redundancy, and space vector redundancy, which are not fully utilized by carrier-based PWM schemes, [12], [20].

The SVPWM schemes utilize additional degrees of freedom, offered by voltage source inverter, more effectively than sinusoidal modulation technique; and can be extended to *n*-level power converters using 2-D and 3-D algorithms, [78]–[81]. Generally, modulation schemes utilizing the space-vector concept are based on three stages algorithm executions. Firstly, active vectors need to be selected, usually closest to the reference and also depending on the subsector where the end of the reference vector is located. Secondly, on- and off- durations of utilized vectors should be computed. In the third stage, appropriate vector sequences are generated, [20].

In [28], [82]–[84], space vector modulation methods have been developed for different goals. Mostly, these goals are: to reduce the switching frequency and computational time, to eliminate or to reduce the common-mode voltage, to reduce total harmonic distortion (THD), and to achieve the ability of DC-link voltage balancing. In case of three-level three-phase inverter, 27 vectors are available, 6 – long, 6 – medium, and 12 – short active vectors and 3 zero vectors. The position and length of the medium (PON, OPN, NPO, NOP, ONP, PNO) and length of the short (POO, ONN, PPO, OON, OPO, NON, OPP, NOO, OOP, NNO, POP, ONO) vectors depends on the DC-link capacitor voltage imbalance. The length and position of the long active vectors are not affected by DC-link voltage imbalance, and their positions are the same for two- and multi-level inverters. Figure 3.6. shows the space vector of three-level three-phase inverter where the DC-link voltages are not (Fig. 3.6. (b)) and are (Fig. 3.6. (a)) balanced. In both cases, the same outer hexagon can be formed, however, the additional inner hexagons may be formed in the presence of DC-link voltage imbalance. Due to this, only short and medium vectors can be used for voltage balancing.

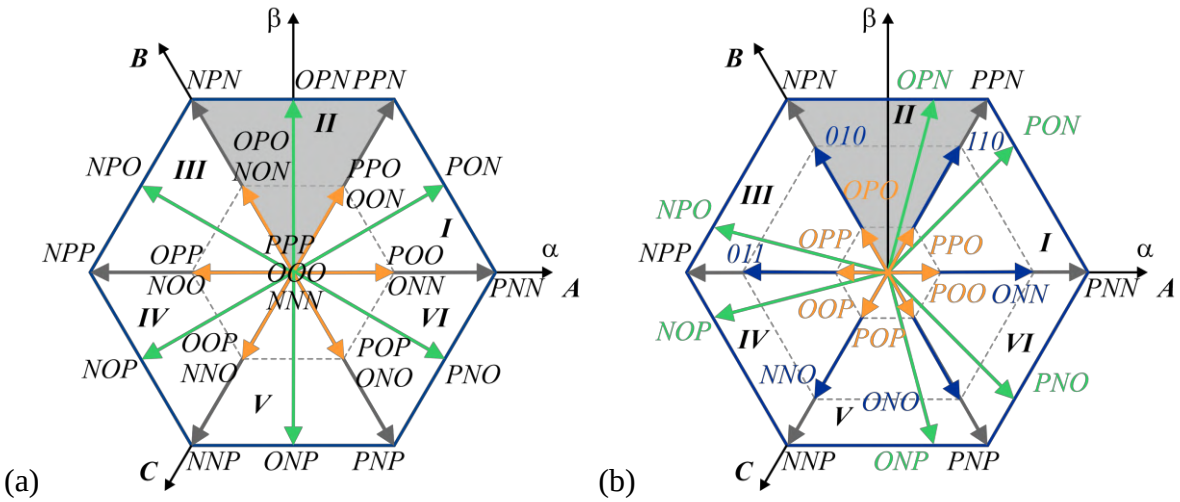


Fig. 3.6. The space vector decomposition: a) the DC-link capacitor voltages are equal $V_{DC1}=V_{DC2}=0.5V_{DC}$ b) the DC-link capacitor voltages are not equal $V_{DC1}=0.3V_{DC}$, $V_{DC2}=0.7V_{DC}$.

3.3. Multilevel inverters for multiphase drives

In the late 1990s, multilevel inverters were well-described for the drive systems where phase number is three or less. However, two decades back, researchers proposed several solutions, where the number of the inverter leg was increased to make up for lack of knowledge on the topic. A brief review of the multilevel inverters, [20], noted the possibility of future development of such systems. Authors mentions the electric vehicles (EVs) and railway traction drive systems as the most prospective direction for multilevel multiphase drive systems, (MMDS). Projections in [20] was proven by numerous article about MMDS in the EV and railway traction applications. The work in [85] presented a brief review of all the main types of multilevel inverters, their summarized comparisons and noted several control approaches. Such control schemes can be seen in [86], where three-level inverter fed dual three-phase PMSM drives was controlled with double SVPWM modulation technique. The system operates with two three-phase systems instead of one six-phase; this leads to simplification of voltage vector synthesis. While authors in [85] focused on the multilevel inverters utilization in the automotive area, researchers in [87] concentrated on traction systems. The several comments about multiphase drives were recapitulated in both articles; like improved fault tolerance capability, lower torque pulsations, and better noise characteristics. Multilevel converters in the multiphase drive systems might be useful to combine the best features of multilevel topologies and multiphase system. The multilevel topology allows for an increase in the drive voltage rating, while the multiphase configuration allows for a decrease in per-leg current for the same output power. Moreover, the quality of output voltage and power can be improved, while *(n-1)/2*, where *n* – phase number, motors can be independently controlled using a single inverter, [10].

4. PWM techniques for multilevel, multiphase NPC inverters

The main problem for multilevel inverters is to keep the DC-link voltages balanced. Lack of voltage balancing in the DC-link leads to the fluctuation in the neutral point and higher THD of the output voltage. The blocking voltage of the switches is lower than the inverter output voltage, so DC-link capacitors' voltage should be kept balanced to avoid undue voltage stress on the constituting switches. Moreover, the capacitance of the DC-link capacitor needs to be increased, which results in a higher cost for the multilevel inverter. The neutral point (NP) voltage drift and ripples should be reduced. Due to these requirements, several hardware [84], [88], [89] and software [90], [91], [92] solutions were proposed. In this part, the various software solutions are considered.

As noted in [93], the modulation techniques for the multilevel multiphase inverter can be divided into three categories: selective harmonic elimination (SHE), space vector and carrier-based methods. The SHEPWM calculate the switching sequence referenced to the voltages with required harmonic content. According to the load current, the switching instant can be adjusted to control the neutral point voltages, [94]. Nonetheless, this type of the modulation strategies requires a priori knowledge of the supplied load and deal with the steady-state of the power converter; knowledge of the connected load allows the estimation of the impact of the current on the DC bus voltages, [93]. Moreover, the SHE techniques are not suitable for applications where voltages and currents are often changed, or with varied load, due to their lack of robustness in these conditions. In [95], the SHEPWM technique with different optimization algorithms for a five-phase, multilevel cascaded inverter was proposed. The SHE modulation method for a three-level five-phase NPC inverter was proposed in [96]. The proposed modulation method achieved low harmonic distortions and reduced number of switching. In [96], the DC-link voltage balancing algorithm was not presented, the degree of freedom offered by a multiphase motor and a second plane control was not shown as well. No SHEPWM for a multiphase multilevel VSI, where all degrees of freedom used and DC-link voltage balancing algorithm proposed, has been presented till now, according to the stock in the literature.

4.1. Sinusoidal PWM techniques for multiphase, multilevel NPC inverters

The CBPWM techniques are focused on per-leg solutions and three-phase modulation techniques can be easily extended to multiphase configuration. The main advantage of this approach is a short computation time, [97]. The most popular CBPWM techniques utilize the multicarrier signals when a single reference compares with at least two triangular carriers in single duty cycle, [98]. Principles of the multicarrier approach was shown in Fig. 1.5. The main

advantage of this approach is the low number of power devices' switching. During a duty cycle, switching devices can be switched between the neutral point (NP) and positive or negative potential; this switching mode is termed single step (SS). However, the NP current cannot be controlled, which lead to imbalance in the DC-link and can attenuate the low-frequency NP voltage ripples, [27]. This feature makes the modulation approach unsuitable for industrial applications. The common mode injection (CMI) technique was proposed to solve this problem, [27], [99], [90], [91]. The sense in this is to inject an additional signal to the reference leg voltage and retake control over the NP current. In [93], the authors mentioned that this approach is equal to the SVPWM proposed in [100]. Nevertheless, both approaches provide limited ability of NP current control for high modulation indexes, due to the CMI limitation, [93]. To remove the limitations of the classical CBPWM approach working on SS mode, the multistep CBPWM techniques were proposed. The idea is to incorporate the ability of switching the leg output voltage between the negative, positive rails, and NP in a single switching period. The NP current is controllable in such modulation techniques, as shown in [101], [92]. Figure 4.1. shows the single step and multistep switching modes in multilevel SPWM techniques. The multistep CBPWM techniques feature higher losses than the single-step techniques, due to higher number of switching, [92], and have higher computational requirements due to the greater number of operation during the single execution cycle. Several papers utilize a combination of both methods [93], [72]. In [72], a hybrid CBPWM technique was proposed, where the main idea was to combine the CMI and the multistep approaches for the DC-link voltage balancing using only one leg for the NP control. For multiphase purposes, this modulation method was extended in [93] .

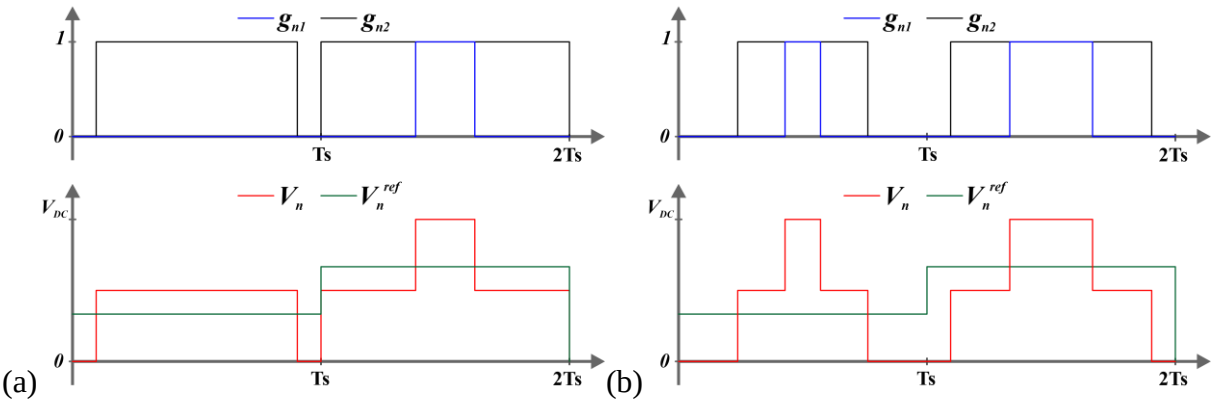


Fig. 4.1. The switching mode: (a) single step (b) multistep.

The extended CBPWM approach utilize the same idea with a multistep approach and optimal common-mode injection; however, the algorithm of their combination was changed for

the multiphase inverter. The authors successfully utilize the degree of freedom offered by the multiphase drive system. Nevertheless, the complicated optimization procedure requires high computational resources. First, the changes in the NP current should be determined. Next, the optimal value of the common mode voltage should be found, depending on the DC-link voltage balancing. In terms of this, the hybrid SVPWM algorithm proposed here achieved comparable, or even shorter, execution times. However, the CBPWM in [93] offers a simpler implementation for drive systems of any number of phases, than the classical SVPWM algorithms.

Another approach to control the DC-link voltage are the solutions based on controller utilization. The basic solution is based on proportional, P, controller utilized as an additional stage in the PWM algorithm. In [102], a modulation scheme was presented, which is a combination of CBPWM and SVPWM for zero-sequence voltage offset injection; the implemented modifications lead to reduced voltage and current ripples and balanced the neutral point voltage. The output signal of P-controller, proposed in [102], depends on DC offset and gain coefficient. The simplicity of P-controller implementation is the main reason for the usage of this type of controller; however, its drawbacks need to be highlighted. Firstly, the same value of gain parameter cannot provide the same dynamics for the entire modulation index range and the absence of the integrating term does not allow to get rid of the steady-state error. The quality of balancing depends on the inverter load parameters, peak value of the fundamental voltage, load power factor, and capacitance of the DC-link capacitors. In [103], the proportional resonant (PR) controller was presented; this solution aimed at voltage drifts reduction and voltage ripples decrease. Due to the proposed structure, PR-controller utilizes two coefficients, similar to the conventional PI controller, but with an additional integrator block; whose gain depends on the product of the durations of small vectors and neutral point current, [103]. In all structures with coefficients, the values of these coefficients should be chosen accordingly. Another disadvantage of that controller structure is the impossibility to eliminate the low-order harmonic component of the neutral-point current for all operating conditions. In [104], the voltage balancing algorithm utilizing the PI controller was proposed by our research team. The simplicity of the sinusoidal PWM presented there is the main advantage of this solution. Nevertheless, the balancing time is still much higher than in DC-link balancing schemes without classical P/PI controllers, e.g. CMI techniques or using additional hardware circuits. This feature is typical for any modulation scheme with P/PI controllers. In [105], two PI-controller were implemented. One controller regulates the DC-link voltages, while the second PI-

controller is used for load voltage control. Such approach achieved lower THD value, however, the balancing time remains relatively high and the output filter should be implemented. Fig. 4.2. shown the SPWM techniques with one and two PI-controllers, proposed in [104] and [106] respectively.

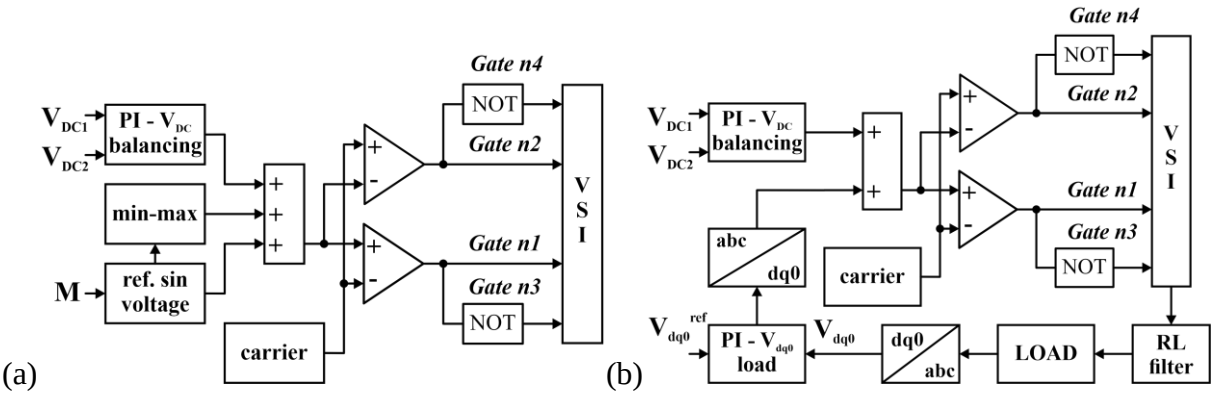


Fig. 4.2. The DC-link voltage balancing technique with: (a) single PI-controller (b) two PI-controllers.

4.2. Space Vector PWM techniques for multiphase, multilevel NPC inverters

During the last few years, the different modifications of space vector modulation techniques for the three-phase multilevel inverters were proposed. In [107], a modulation algorithm for a three-level five-phase VSI was proposed, which was based on solutions for three-phase systems. The aforementioned algorithm suggested dividing each of the 36-degree sectors into four sub-sectors and using three active vectors to obtain the output vector. The disadvantage of this approach was the presence of unwanted low-order harmonics caused by ignoring the second plane. In the articles [108] and [100], two different three-level SVPWM techniques were proposed, which took into account the need for control in all available planes, for five- and seven-phase VSIs, respectively. The work in [108] suggests dividing the sector into 10 subsectors and using four active vectors to determine the corresponding output vector. The proposed solution made it possible to eliminate low-order harmonics, which was significant problem of previous solutions. The authors also drew attention to the possibility and necessity of voltage balancing on the DC-link capacitors, but did not offer corresponding algorithm, leaving this topic open. In [100], the main focus was on optimizing the process of selecting the appropriate active vectors. The proposed modulation method divides the sector into 18 subsectors and finds the optimal switching pattern. As the authors noted, despite the small improvement in THD compared to CBWPM, the execution time of the SVPWM algorithm is twice as long, which, together with the complexity of algorithm, makes its deployment in

industrial applications unlikely. At the same time, the main advantage of SVPWM is the ease in controlling the harmonics in different planes. In the article [97], the authors confirmed this statement by conducting a comparative analysis of five different modulation algorithms.

The pulse width modulation technique is based on the simplification of the space vector switching diagram proposed in [109]. That algorithm leads to reduce the common-mode voltage (up to one-six of V_{DC}) and propose a neutral point voltage control. In [109] switching sequence was adopted utilizing the idea of the two-level common-mode voltage reduction PWM (CMV-R PWM), [82]. The DC-link voltage control in [109] assumes the use of the zero-sequence voltage injection, which is investigated as an additional degree of freedom to improve the PWM characteristics. Another approach to control the DC-link voltage and suppress common-mode is a virtual space vector PWM (VSVPWM). In [110], modification of the VSVPWM was proposed. It was termed improved virtual space vector PWM (IVSVPWM); such improvement stems from the expansion of the active neutral point voltage control (ANPVC). The idea of virtual space vector modulation leads to controlled DC-link voltages and to reduction of the common-mode voltage (CMV), [111]. The IVSVPWM algorithm focused on DC-link balancing, CMV suppression and optimization of virtual vector construction. An analytical procedure, which achieved reduction of the CMV, was proposed in [118]. In the analysis, the common-mode voltage generated by each small vector was compared and vectors with high CMV were omitted. Additionally, authors proposed the optimization procedure of the virtual vector generations by adjusted coefficients in the implementation. Such coefficients have impact on the small and medium virtual vectors selection, on the NP current and CMV values. Disadvantage of this modulation method is the limitation in the CMV suppression – coefficients used in the proposed algorithm must be limited to make CMV reduction efficient. In [110], active neutral point voltage control (ANPVC) was based on the adjusted time of the small and medium virtual vectors. For the ANPVC, small and medium vectors can be modified, depending on the sector where the vector is situated. Possible adjustment range, where virtual vectors can change their length, and virtual vectors placement, for all coefficients equal to 1, are shown in Fig. 4.3. The combination in [110] will be chosen, which offers higher charge incrementation. However, the proposed balancing scheme has various characteristics under different modulation index and power factor values. The adaptation speed of the balance coefficients slows down if the power factor goes to 1. In [112], a modified space vector PWM technique was proposed, where researchers aim to eliminate current ripples and reduce the harmonic distortion. However, the balancing of DC-link voltages was not incorporated.

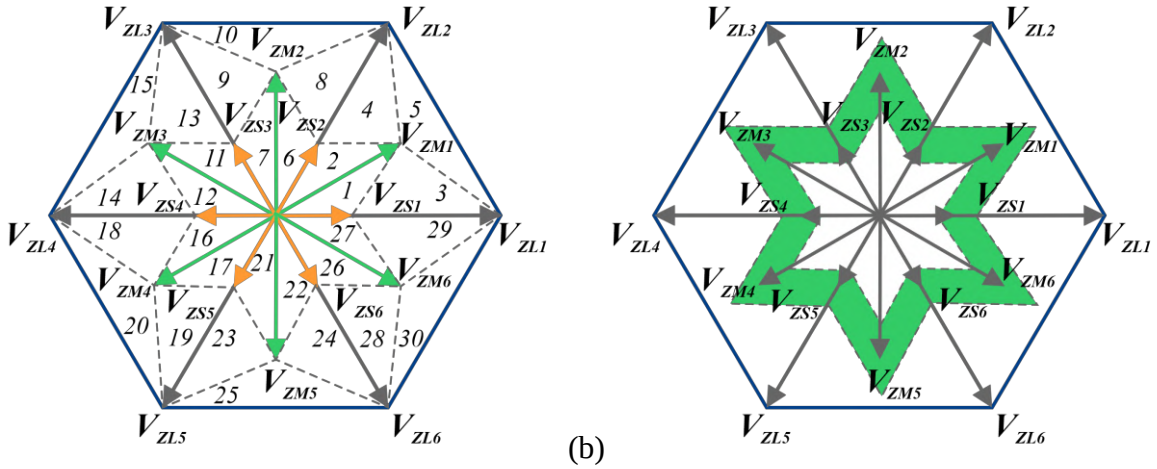


Fig. 4.3. The space vector diagram for IVSVPWM technique (a) virtual vectors' positions (b) possible adjustment area of the short and medium virtual vectors.

In the case of three-level multiphase NPC inverters, the synthesis of space vectors requires the analysis of a large number of active vectors defined simultaneously in many orthogonal systems, [113]. And at the same time, the position and length of these vectors depend on DC - link voltage asymmetry. While a two-level five-phase VSI can produce 32 switching vectors determined in two orthogonal planes, a nine-phase two-level VSI can produce 512 vectors, depending on each other in four orthogonal spaces, [114]. In three-level inverters, it is possible to generate 3^n switching vectors (n is the phase number) with positions and lengths depending on the DC-link voltages. For a three-level five-phase inverter, 243 vectors are available. Fig. 4.4. shows the space vector placement in the first plane only when the DC-link voltages are and are not the same. Moreover, these vectors are in two orthogonal planes and generating voltage in the first plane prompts voltage vector generation in the second plane. At the same time, the positions and lengths of the voltage vectors depend on DC-link voltage balancing. Additionally, the switching pattern should ensure a minimum number of commutations. These properties make, in general, SVPWM algorithms for multiphase inverters complex.

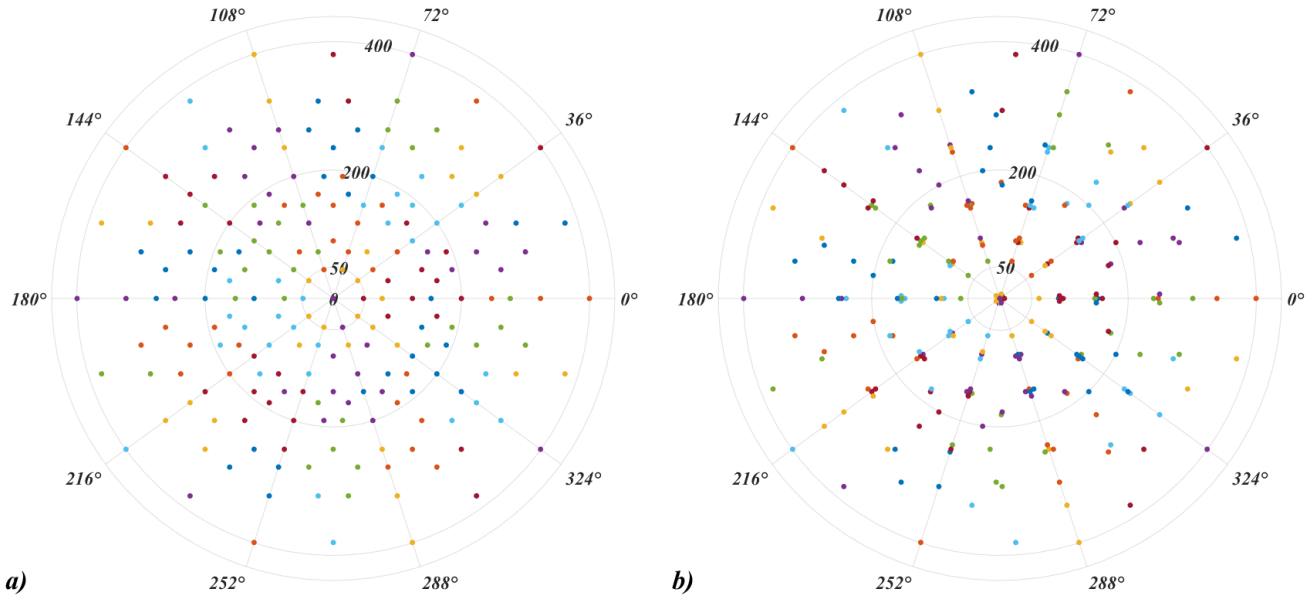


Fig. 4.4. The space vector decomposition for a three-level five-level inverter, dots indicate the ends of available vectors in the first plane , when: a) the DC-link capacitor voltages are balanced $V_{DC1}=V_{DC2}=0.5V_{DC}$ b) the DC-link capacitor voltages are not balanced $V_{DC1}=0.4V_{DC}$, $V_{DC2}=0.6V_{DC}$.

So far, most of the proposed SVPWM solutions for three-level multiphase inverters assume that only one output voltage vector is generated in the inverter, [100], [115]. The analysis presented in the papers assumes that the voltages on the DC-link capacitors are the same and the main emphasis is on the selection of active vectors for which it is possible to determine non-negative activation times, [100]. The synthesis of active vectors, that can be used to generate the output voltages, is based on the analysis of the reference values of phase voltages, [100]. In some solutions, the activation times are calculated not for the active vectors specified in the orthogonal systems (which is the core of SVPWM algorithms), but for the reference phase voltages using the vectors specified in individual phases (which corresponds to carrier-based PWM algorithms), [116], [117].

As shown above, the topic of SVPWM algorithms for inverters with an increased number of levels and phases is still open. As the number of voltage levels and phase number increases, the number of papers describing SVPWM methods decreases. Figure 4.5. shows the analysis of the IEEE Xplore database, number of the publications where the SVPWM techniques were proposed counted.

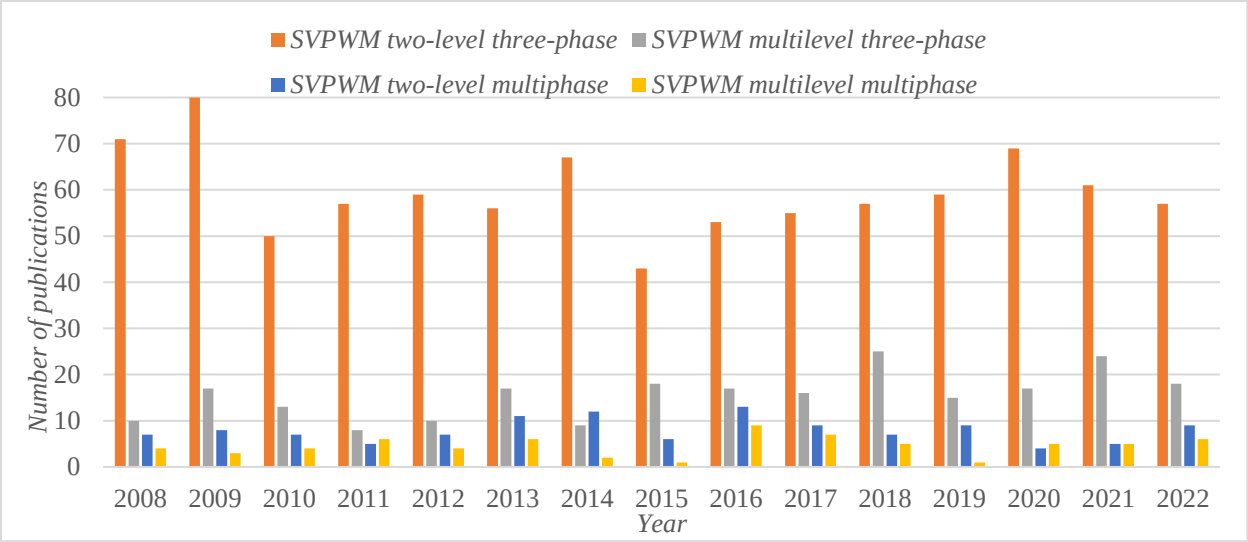


Fig. 4.5. The number of publications in IEEE Xplore database describing SVPWM techniques for two- and multilevel three- and multiphase VSIs.

Relatively few papers were concerned with the possibility of correct output voltage generation in the case of DC-link voltage imbalance even in the case of three-phase inverters, [118]–[120]. Most solutions assume that the DC-link voltages are balanced by additional algorithms and the synthesis itself is based on the assumption of the same voltages on DC-link capacitors, [100]. Even a slight DC-link voltage imbalance can affect the selection of active vectors - and finally, affect the quality of the output voltage. This is due to the deviations in the lengths and positions of active vectors if the DC-link voltages are unbalanced. According to the best of my knowledge, no effective space vector modulation algorithms have been developed for multiphase three-level VSIs, where the DC-link voltages can be balanced as well as the output voltage vectors can be generated correctly when the DC-link voltages are not balanced.

In summary, following this doctoral study, a new PWM algorithm based on Space-Vector approach for three-level multiphase inverters was developed. Proposed modulation technique allows independent generation of $(n-1)/2$ output voltage vectors (n is an odd phase number) given by the superior control system (like FOC) even in the scenario of DC-link voltage imbalance. It proffers solution for proper selection of active voltage vectors and will make it possible to balance the DC-link voltages of three-level multiphase power converters. The neutral point voltage control scheme is an integral part of the modulation process without requirement of additional balancing circuit usage. Synthesis of a modulation algorithm is realized using active vectors specified in orthogonal systems and taking into account the DC-link voltage imbalance.

5. Proposed space vector modulation technique and DC-link voltage balancing algorithm

5.1. SVPWM algorithm for two- and three-level five-phase inverter

The three-level inverter can be forced to work as a two-level inverter. This feature can be obtained when both upper: g_{x1}, g_{x2}, and lower: g_{x3}, g_{x4}, switches are activated concurrently in each phase, *x*– phase number (x= a, b, c, d, e). Fig. 5.1. shows the power circuit of the three-level five-phase NPC VSI.

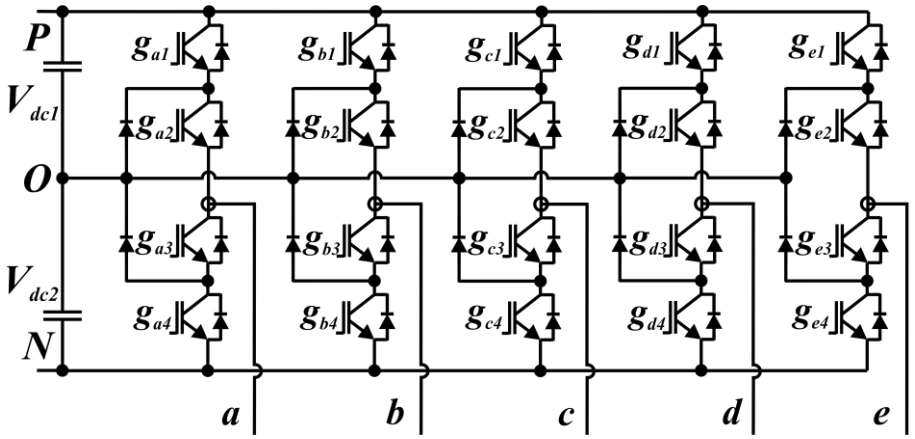


Fig. 5.1. The power circuit of the five-phase, three-level NPC inverter.

During the modulation process, the lower switching devices are controlled with the inverted signal of the upper ones, as follows:

$$\begin{aligned} g_{x3} &= !g_{x1}; \\ g_{x4} &= !g_{x2}; \end{aligned} \tag{5.1}$$

where $g_{x1...4}$ are the gate signals for the switches, x – phase number. These variables can take binary values only. The high value, or 1 – the switch is ON, and low value, 0 – the switch is OFF.

For a multiphase inverter, the active vectors are placed in many orthogonal systems, e.g. two planes for five-phase, three planes for seven-phase inverters, etc. Fig. 2.3. shows the space vectors placement in the first and second planes for a two-level five-phase VSI. Positions of the medium active vectors are the same in both planes. However, the short and long active vectors changed their positions and length. In the second plane short vectors become long and long vectors become short, Fig. 2.3.

The sector and subsector identification are required for selection of the active vectors. When the common solutions utilize different techniques for sector dividing, the proposed SVPWM

use the 4 freely selected active vectors, [121]. These active vectors might be the same for any reference voltage vectors regardless of their position and length. The only requirement for the active vectors is: their components must create an invertible matrix $\boldsymbol{V^{-1}}$. The optimal sequence of active vectors is determined in the final stage of the modulation algorithm based on the previously determined durations, as in [55], [121]. This approach allows the simplification of the initial stage of the algorithm because the subsector determination procedure is omitted.

During the initial stage, the two-level space vector diagram was used and active vectors: PPPPN, PNNNN, NNPPP, NNNPP were pre-selected (as shown in Fig. 5.2), for example. Herein, SVPWM algorithm for 3-level NPC inverter is based on the ideas presented in [121] and [55] for five- and multiphase 2 level inverters respectively. Principles of the presented initial procedure were utilized and the expanded hybridized PWM technique for a three-level inverter was proposed in this thesis.

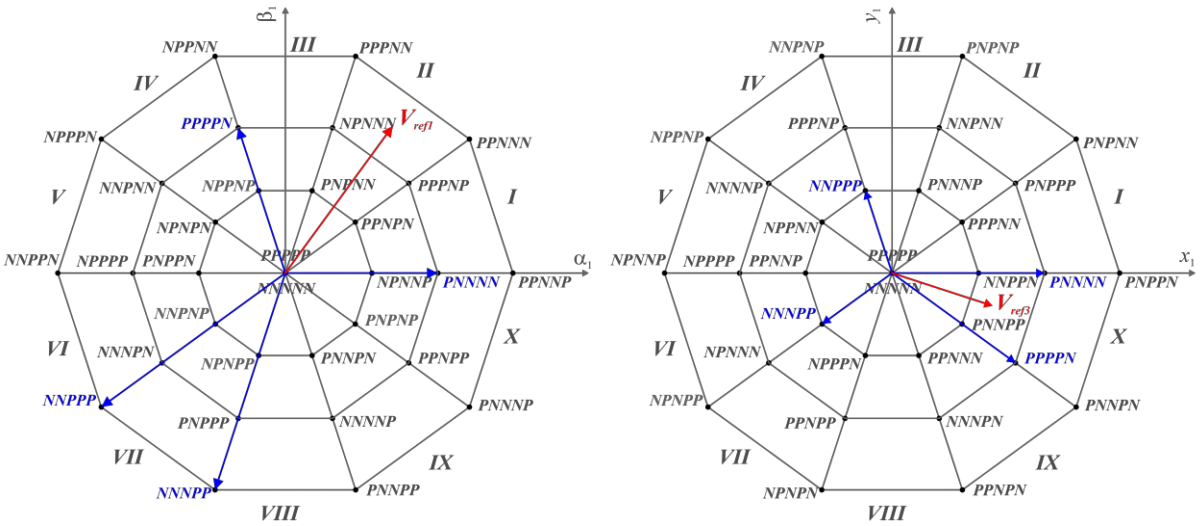


Fig. 5.2. The reference and selected active vectors placements in α_1-β_1 and x_1-y_1 orthogonal planes for a five-phase, two-level inverter.

Condition (1.4) is used to calculate durations of the four pre-selected active vectors:

$$\boldsymbol{T} = \frac{T_s}{V_{DC}} \cdot \boldsymbol{V^{-1}} \cdot \boldsymbol{V_{ref}} \Rightarrow \begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \end{bmatrix} = \left(T_s \cdot \boldsymbol{V^{-1}}\right) \cdot \begin{bmatrix} V_\alpha^{ref} \\ V_\beta^{ref} \\ V_x^{ref} \\ V_y^{ref} \end{bmatrix} \cdot \frac{1}{V_{DC}}; \tag{5.2}$$

where: $(\boldsymbol{T_s V^{-1}})$ is calculated only once and stored in the processor memory. The coefficients matrix $\boldsymbol{V}$ contains the components of the pre-selected active vectors. The vectors component

can be calculated from the Clarke transformation matrix - $\boldsymbol{A}$ (2.8) and the output voltages of a five-phase VSI:

$$\begin{bmatrix} V_{\alpha i} & V_{\beta i} & V_{xi} & V_{yi} \end{bmatrix}^T = \boldsymbol{A} \cdot \begin{bmatrix} V_{aN} & V_{bN} & V_{cN} & V_{dN} & V_{eN} \end{bmatrix}^T \cdot 1 \big/ V_{DC}; \tag{5.3}$$

where: i is a vector number, and the output voltages for a five phase VSI can be calculated as:

$$V_{xN} = \frac{V_{DC}}{2} \cdot \left(S_{xU} - S_{xL} - \frac{1}{5} \sum_{x=a}^{e} \left(S_{xU} - S_{xL} \right) \right), \tag{5.4}$$

where: x is a leg number (x=a,b,c,d,e), S_{xU} and S_{xL} are the gate signals for the upper (U) and the lower (L) transistor in the leg x. The variables S_{xU} and S_{xL} can take 2 values: 1 – switch is *ON*, and – switch is *OFF*.

The components of the active vectors from Fig. 5.2. filled the coefficients matrix $\boldsymbol{V}$ as:

$$\begin{bmatrix} v_{i=1} & v_{i=2} & v_{i=3} & v_{i=4} \\ V_{\alpha i} & V_{\alpha i} & V_{\alpha i} & V_{\alpha i} \\ V_{\beta i} & V_{\beta i} & V_{\beta i} & V_{\beta i} \\ V_{xi} & V_{xi} & V_{xi} & V_{xi} \\ V_{yi} & V_{yi} & V_{yi} & V_{yi} \end{bmatrix} = \begin{bmatrix} v_{i=PPPPN} & v_{i=PNNNN} & v_{i=NNPPP} & v_{i=NNNPP} \\ -0.1954 & 0.6325 & -0.8279 & -0.3162 \\ 0.6015 & 0 & -0.6015 & -0.9733 \\ 0.5117 & 0.6325 & -0.1207 & -0.3162 \\ 0.3717 & 0 & -0.3717 & 0.2297 \end{bmatrix}$$

Due to the freely selected active vectors, the durations calculated from eq. (5.2) can be positive or negative. In case of negative durations, the active vector can be replaced by the opposite one, as shown in Fig. 5.3, and their duration can be re-calculated according to:

$$if\ T_i < 0 \Rightarrow \begin{cases} T_i = -T_i \\ v = 2^x - 1 - v \end{cases}, i = 1,2,3,4; \tag{5.5}$$

where x is an inverter phase number, v indicates the selected vector number and is equal to:

$$v = 2^0 \cdot S_{aU} + 2^1 \cdot S_{bU} + ... + 2^4 \cdot S_{eU}, \tag{5.6}$$

After eq. (5.5) all durations are positive, but their sum can exceed the pulse period T_s.

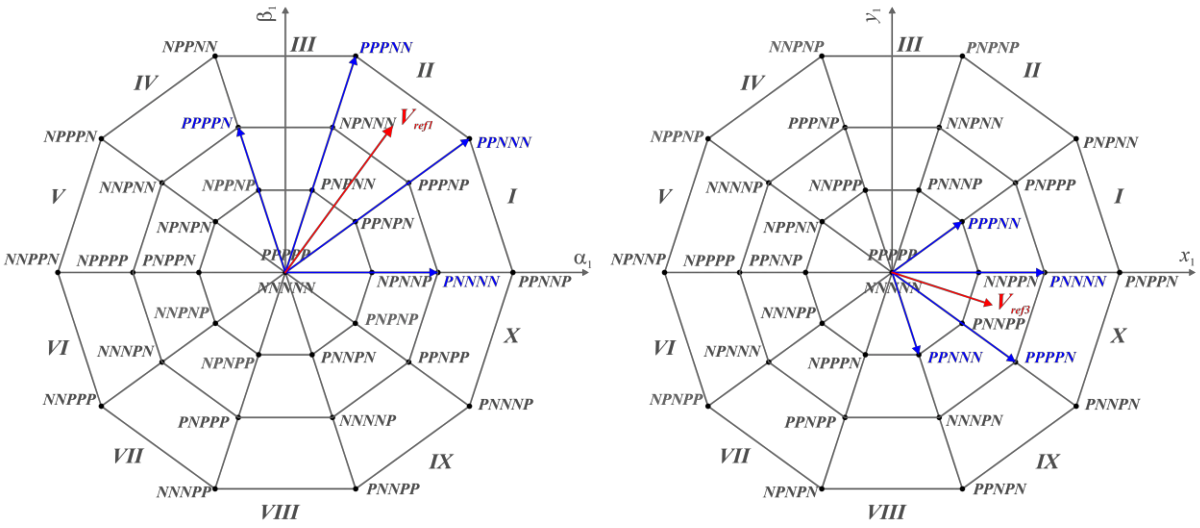


Fig. 5.3. The reference and selected active vectors placements in α_1-β_1 and x_1-y_1 orthogonal planes for a five-phase, two-level inverter.

The order of the active vectors' activations does not affect the output voltage. Switching on the upper or lower switches affects the average value of the phase voltage only. Thus, the signals switching on the upper and lower switches can be freely placed in the time domain, including "grouping" them to avoid unnecessary switching. The average value of the phase voltage $V_{x(av)}$ can be calculated using determined durations $T_{x(ON)}$ and $T_{x(OFF)}$, (where x is an inverter phase (x=a, b, c,…,e)).

$$V_{x(av)} = \frac{1}{T_s} \cdot \sum_{i=1}^{4} \left(V_{DC} \cdot \left(S_{xU(i)} - S_{xL(i)} \right) \cdot T_{(i)} \right) = \frac{V_{DC}}{T_s} \cdot T_{x(ON)} - \frac{V_{DC}}{T_s} \cdot T_{x(OFF)}, \tag{5.7}$$

where i is a number of the active vector, and durations $T_{x(ON)}$ and $T_{x(OFF)}$ are defined as:

$$\begin{aligned} T_{x(ON)} &= \sum_{i=1}^{4} \left(S_{xU(i)} \cdot T_{(i)} \right) \\ T_{x(OFF)} &= \sum_{i=1}^{4} \left(S_{xL(i)} \cdot T_{(i)} \right) \end{aligned}, \; x = a, b, .., e. \tag{5.8}$$

The gating signals determined using eq. (5.8) are shown in Fig. 5.4. (a). It is worth noting, that the sum of positive and negative state's durations is greater than the pulse period. To solve this, the zero vector have to be found and eliminated (Fig.5.4. (b)). As shown in the Fig. 5.4. (a), the duration of the zero vector is shortest durations among $T_{a(ON)}$ … $T_{e(ON)}$

The duration of zero vector T_0 can be calculated using the function:

$$T_0 = \min\left(T_{a(ON)}, ..., T_{x(ON)} \right), \; x = a, b, .., e. \tag{5.9}$$

The gate signals' durations were changed as follows:

$$T_{x(ON)} = T_{x(ON)} - T_0,\ x = a,b,..,e. \tag{5.10}$$

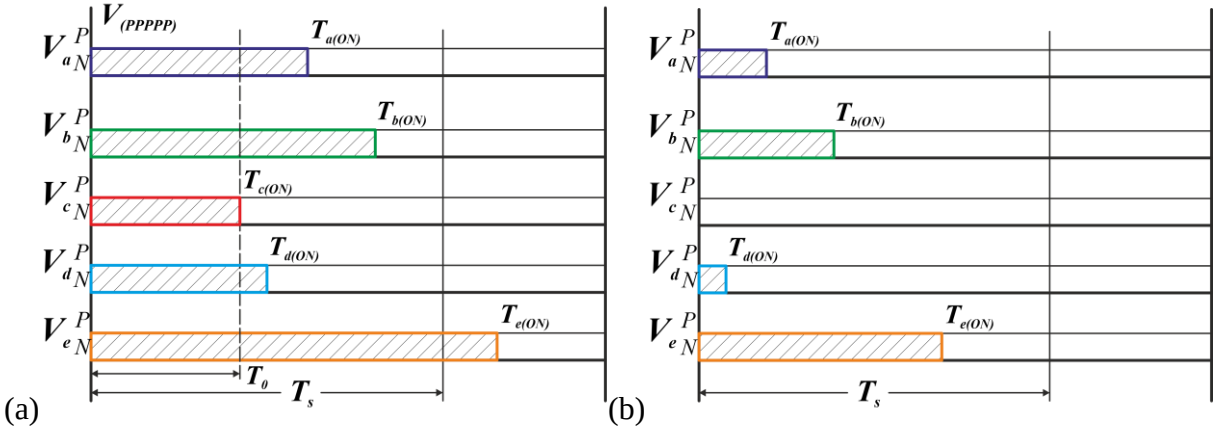


Fig. 5.4. Gate signal and durations: (a) before zero vector elimination (b) after zero vector elimination.

The last step of the two-level SVPWM modulation algorithm is to introduce two zero vectors to the resulting switching sequence and recalculate all, previously obtained, durations. Duration of the introduced zero vectors can be calculated as:

$$T_0 = 0.5 \cdot T_s \cdot \max\left(T_{a(ON)},...,T_{x(ON)}\right),\ x = a,b,..,e. \tag{5.11}$$

While the gate signals' durations are equal to:

$$\begin{aligned} T_{x(ON)} &= T_{x(ON)} + T_0 \\ T_{x(OFF)} &= T_s - T_{x(ON)} \end{aligned},\ x = a,b,..,e. \tag{5.12}$$

The same effect (shown in Fig. 5.5.) can be also obtained, if half of the zero-vector duration will be subtracted:

$$T_{x(ON)} = T_{x(ON)} - \frac{T_0}{2},\ x = a,b,..,e. \tag{5.13}$$

Zero vector injection is shown in Fig. 5.5, where the resulting switching sequence is presented as well. After this step the PWM algorithm for a two-level five- and multiphase VSIs is completed. Obtained durations are compared in the processor timer and the corresponding gate signals are generated.

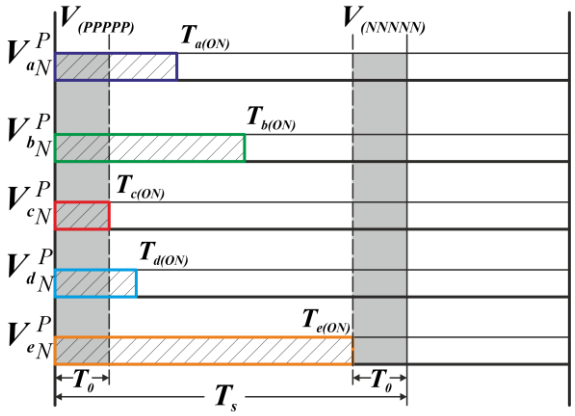


Fig. 5.5. Final switching sequence after zero vector T_0 introduction.

5.2. SVPWM algorithm for three-level multiphase VSIs

The thee-level inverter allows to introduce an additional level to the output voltage waveforms. This can be done introducing the DC-link neutral point potential to the output voltage waveforms.

In two-level switching mode the gate signals S_{xU}, presented in Fig. 5.5., activate switches in pair: $S_{xU}=g_{x1}=g_{x2}$, while $S_{xL}=g_{x3}=g_{x4}$, according to Fig. 5.1. Resulting switching sequence from Fig. 5.5. with additional potential is shown in Fig. 5.6. (a). Figure 5.7. shows the generated voltage vectors in the first and second planes when the switching sequence from Fig. 5.6. (a) is used. Transition to the three-level switching pattern can be done by the zero vector $V_{(OO\ldots O)}$ introduction, as shown in Fig. 5.6. (b). The introduction procedure consists of partially replacing the existing zero vectors with a new zero vector. The duration of this zero-vector cannot exceed the sum of the existing zero vectors and can be defined as:

$$0 \le T_{(OOO\ldots O)} \le T_{(0)(NNN\ldots N)} + T_{(x)(PPP\ldots P)}; \tag{5.14}$$

where the $T_{(NNN..N)}$ and $T_{(PPP..P)}$ are the durations of the existing zero vectors $V_{(NNN..N)}$ and $V_{(PPP..P)}$.

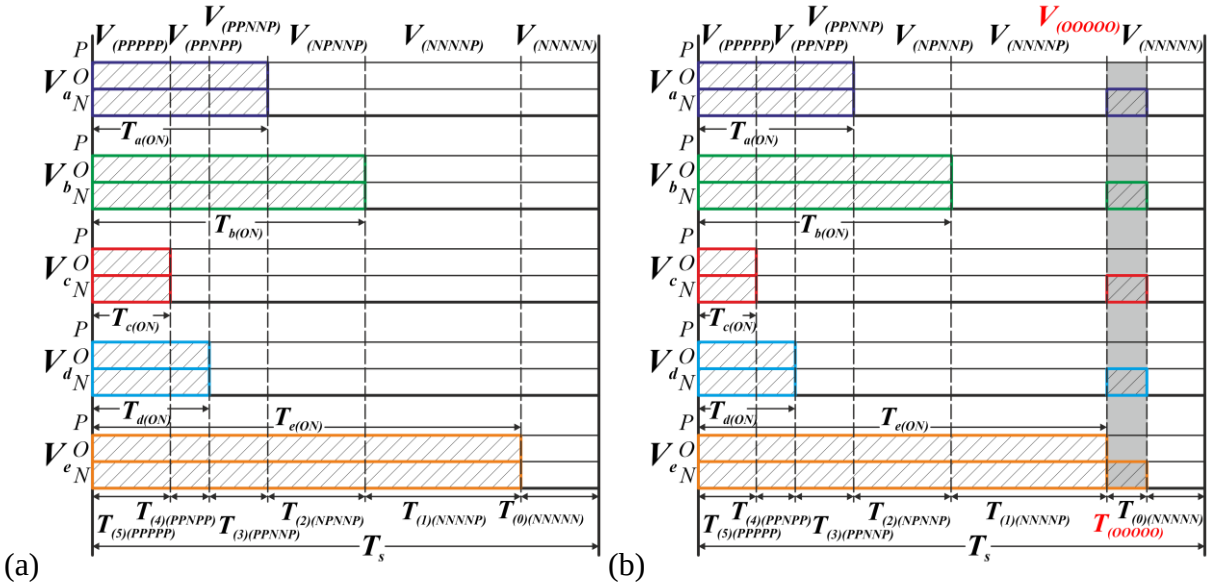


Fig. 5.6. The switching pattern of: (a) the three-level five-phase NPC VSI working in two-level mode; (b) zero-vector injection for the three-level modulation.

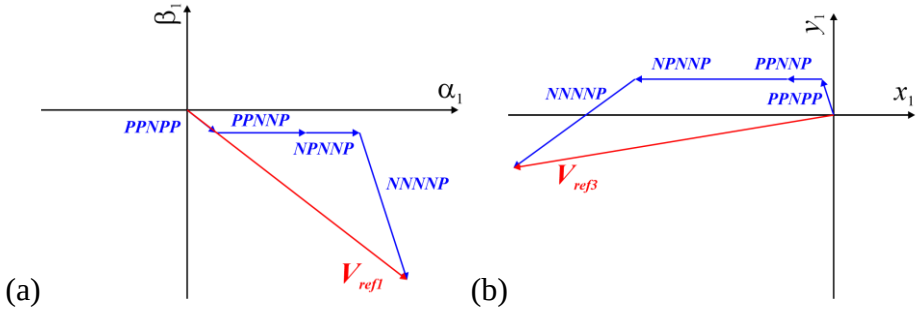


Fig. 5.7. The resulting voltage vector in: (a) the first and (b) the second orthogonal planes.

The switching sequence after zero vector injection contains all zero vectors: $V_{(NNN..N)}$, $V_{(OOO..O)}$and $V_{(PPP..P)}$ which results in a higher number of switching. The switching sequence can be optimized by an 'O' state shifting. This operation has not affected on the average output voltage value by mutual cancellation of forced active vectors. The duration of the 'O' states for each inverter phase is the same and identical to the zero vector duration $T_{(OOO..O)}$:

$$T_{a(0)} = T_{b(0)} = \ldots = T_{x(0)} = T_{(000\ldots0)} \tag{5.15}$$

The durations of the gate signals should be recalculated, as follows:

$$\begin{aligned} &T_{a(P)} = T_{a(P)} - T_{a(O)} \cdot 0.5; \quad \ldots; \quad T_{x(P)} = T_{x(P)} - T_{x(O)} \cdot 0.5; \\ &T_{a(N)} = T_{a(N)} - T_{a(O)} \cdot 0.5; \quad \ldots; \quad T_{x(N)} = T_{x(N)} - T_{x(O)} \cdot 0.5; \end{aligned} \tag{5.16}$$

As a result, a new switching sequence is presented, Fig. 5.8. (a), where the additional active vectors utilize the third-level $V_{(PPOPP)}$, $V_{(PPOOP)}$, $V_{(PPNOP)}$, $V_{(OPNNP)}$, $V_{(NONNP)}$, $V_{(NNNNO)}$. These active vectors connect the load current to the 'O' potential, Fig. 5.1. When the durations of the

'O' state are the same in each inverter phase, the DC-link capacitor voltages are unchanged, because the sum of the phase currents is equal to 0.

5.3. DC-link voltage balancing

The duration of the 'O' state can be used for controlling the DC-link voltages. The DC-link voltages V_{dc1}, V_{dc2} (as shown in Fig. 5.2.) depend on the neutral point current, as follows:

$$V_{dc1}(t) = \frac{1}{C}\int_0^t \left(\frac{i(\tau)}{2}\right) d\tau, \quad -V_{dc2}(t) = \frac{1}{C}\int_0^t \left(\frac{i(\tau)}{2}\right) d\tau; \tag{5.17}$$

where i is a DC-link neutral point current and t is a 'O' state duration. From eq. (5.17) the unbalance between both DC-link capacitors are:

$$\Delta V = V_{dc1}(t) - V_{dc2}(t) = \frac{1}{C}\int_0^t \left(i(\tau)\right) d\tau = \frac{1}{C} i \cdot t; \tag{5.18}$$

An actual voltage imbalance in the DC-link can be determines by a charge delivered to the neutral point, Q_{actual}, which can be expressed from eq. (5.18) as follows:

$$Q_{actual} = i_x \cdot T_x = C \cdot \Delta V \tag{5.19}$$

where T_x is the time to eliminate the DC-link voltage imbalance when the neutral point current is equal to i_x, and x is the phase denotation. The current i_x is supplied by each inverter phase to the neutral point of the DC-link.

The average value of the phase voltage should stay unchanged, so it is necessary to determine the possibility of the duration change of '0' state in each phase for a balancing process. The duration of 'N' and 'P' states can be shortened maximally by the duration $T_{x(max)}$ defined as:

$$\begin{aligned} &if\left(T_{x(P)} \cdot V_{dc1} < T_{x(N)} \cdot V_{dc2}\right) \Rightarrow T_{x(\max)} = T_{x(P)}; or \\ &if\left(T_{x(N)} \cdot V_{dc2} < T_{x(P)} \cdot V_{dc1}\right) \Rightarrow T_{x(\max)} = T_{x(N)}; \end{aligned} \tag{5.20}$$

where $T_{x(N)}$, $T_{x(P)}$ are the durations, when the 'N' and 'P' potentials are connected in the phase, and x – is a phase number ($x=a, b, \ldots, e$), eq. (5.16), Fig. 5.8. (a).

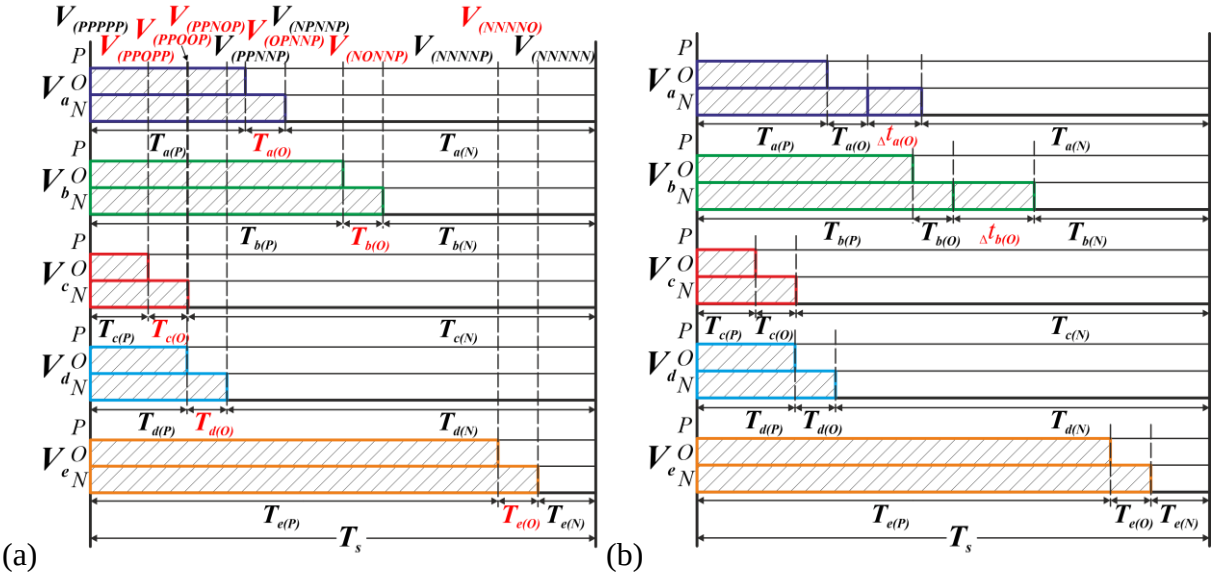


Fig. 5.8. The switching pattern for five-phase NPC: (a) working in the three-level mode after the vector $V_{(OOO..O)}$ shifting; (b) with pulses extensions for balancing purpose $i_a>0$, $i_b>0$, $i_c<0$, $i_d<0$, $i_e<0$.

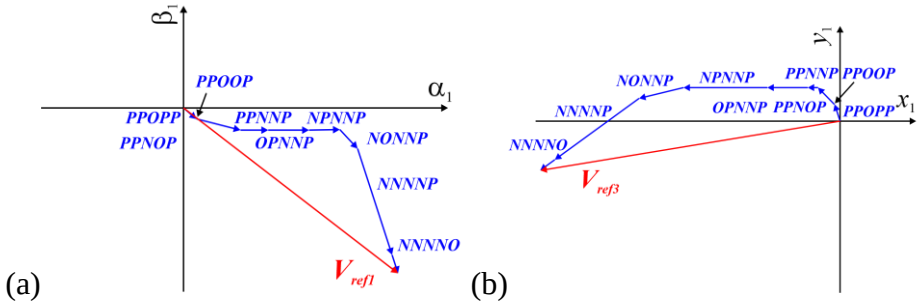


Fig. 5.9. The resulting voltage vector in: (a) the first and (b) the second orthogonal planes.

After transition to the three-level switching pattern, the generated voltage vectors in the first and second planes do not change their positions and lengths. Figure 5.9 shows these vectors when the switching sequence from Fig. 5.8 (a) is used.

The charge, which might be used to balancing the DC-link capacitor voltages and can be delivered to the neutral point by each of inverter phases is determining as follows:

$$Q_{x(\max)} = T_{x(\max)} \cdot i_x; \tag{5.21}$$

An additional limitation should be included to the modulation algorithm to ensure the desired direction of DC voltage changes and is expressed as follows:

$$if\left(\operatorname{sgn}\left(Q_{x(\max)}\right) \neq \operatorname{sgn}\left(Q_{actual}\right)\right) \Rightarrow Q_{x(\max)} = 0, \tag{5.22}$$

where x – is an inverter phase number ($x=a, b, \ldots n$), the function $sgn()$ – is a positive or negative sign of the variables ($Q_{x(max)}$, Q_{actual}). If the signs of $Q_{x(max)}$ and Q_{actual} are not the same, the charge delivered to that phase increases imbalancing in the DC-link voltages. Taking into

account all the limitations, the maximum value of the available charge that can be delivered to the neutral point by the current of each phase, can be calculated as:

$$Q_{all(\max)} = \sum_{x=a}^{n} Q_{x(\max)}; \tag{5.23}$$

where x – is an inverter phase number ($x=a, b, \ldots n$). The eq. (5.23) provides an additional degree of freedom, due to a total $Q_{all(max)}$ value. While this value is ensuring balancing purposes, phases with the opposite charge direction can be unchanged.

The capacitor voltages can be balanced by the charge supplied from the individual VSI phases. The charge might be delivered in any proportion by particular inverter phases, including the situation, where the charge $Q_{x(max)}$ with opposite direction is not be set to zero, as in (5.22). The original value of $Q_{x(max)}$ can remain the same in the area where the balancing process is possible. To determine this area, the sum of available charge values from the other phases must be greater than the sum of charges $Q_{x(max)}$ in phase(s) that would unbalance the DC-links. This introduces additional degrees of freedom in constructing the sequence of gate signals and, thus, in constructing the switching pattern. The PWM algorithm shown here utilizes the phases' charge proportional to the total charge value $Q_{all(max)}$ and only the energy from phases with the appropriate direction is taken into account (5.22). The charge delivered by particular inverter phases can be determined as follows:

$$Q_{x(balancing)} = Q_{x(\max)} \cdot \frac{Q_{actual}}{Q_{all(\max)}}; x = a,b,...,e; \tag{5.24}$$

To complete the balancing process in a single switching period T_s, the charge Q_{actual}, which is required to balance the process, should be smaller than the available charge that can be delivered by all inverter phases:

$$0 \le abs\left(Q_{actual}\right) \le abs\left(Q_{all(\max)}\right), \tag{5.25}$$

otherwise, the balancing procedure will be done during the several switching periods.

As shown in Fig. 5.8. (b), the duration of the 'O' state in some of the inverter phases should be extended to perform the balancing procedure. The extension values for these phases can be determined by:

$$\Delta t_{x(O)} = \frac{Q_{x(balancing)}}{i_x} \tag{5.26}$$

To keep the average value of the phase voltages unchanged, corrections need to be implemented. The durations of the 'N', 'O', and 'P' state, defined in eq. (5.15) and (5.16) should be modified as follows:

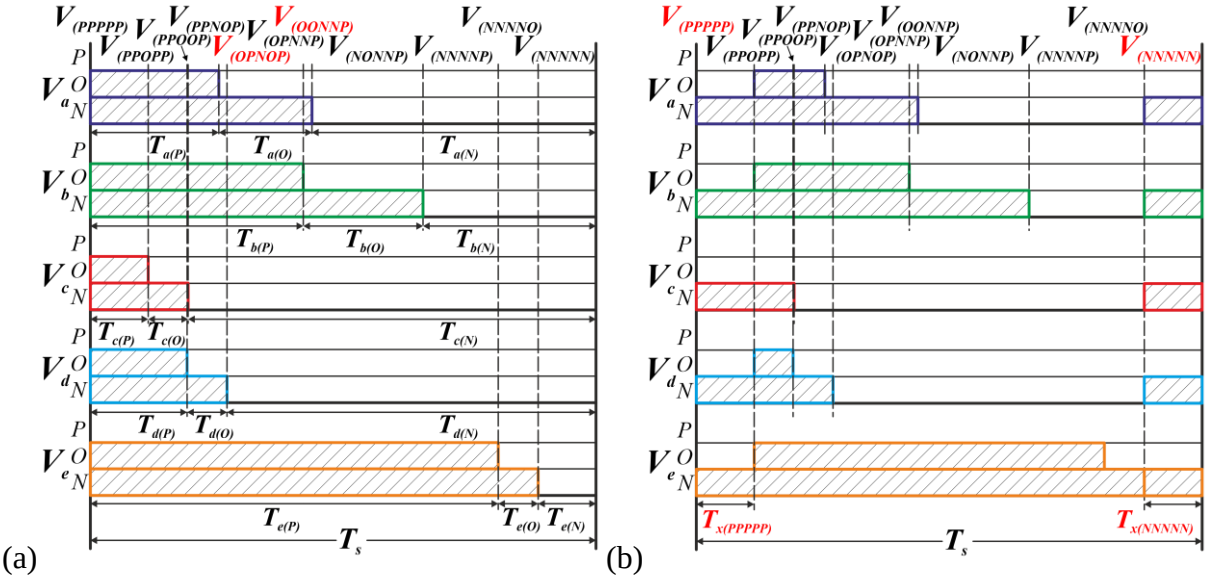
$$\begin{aligned}
&T_{a(P)} = T_{a(P)} - {}_{\Delta}t_{a(O)} \cdot \frac{V_{dc2}}{V_{dc2}+V_{dc1}}; T_{a(O)} = T_{a(O)} + {}_{\Delta}t_{a(O)};\\
&T_{a(N)} = T_{a(N)} - {}_{\Delta}t_{a(O)} \cdot \frac{V_{dc1}}{V_{dc2}+V_{dc1}};\\
&\vdots\\
&T_{x(P)} = T_{x(P)} - {}_{\Delta}t_{x(O)} \cdot \frac{V_{dc2}}{V_{dc2}+V_{dc1}}; T_{x(O)} = T_{x(O)} + {}_{\Delta}t_{x(O)};\\
&T_{x(N)} = T_{x(N)} - {}_{\Delta}t_{x(O)} \cdot \frac{V_{dc1}}{V_{dc2}+V_{dc1}};
\end{aligned} \tag{5.27}$$

Coefficients $\frac{V_{dc2}}{V_{dc2}+V_{dc1}}, \frac{V_{dc1}}{V_{dc2}+V_{dc1}}$ in (5.27) are required for a correct output voltage generation under DC-link voltage imbalance. The obtained durations $T_{x(N)},\ldots,T_{x(P)}$ can be positive or zero, due to the limitation implemented in eq.(5.20). Fig. 5.10. (a) shows the resulting switching pattern at this stage of the modulation algorithm. The utilized active and zero vectors are also shown in Fig. 5.10. (a).

The average value of the phase voltage $V_{x(av)}$, defined in eq. (5.7), can be re-calculated using the modified durations $T_{x(P)}$, $T_{x(O)}$ and $T_{x(N)}$ as:

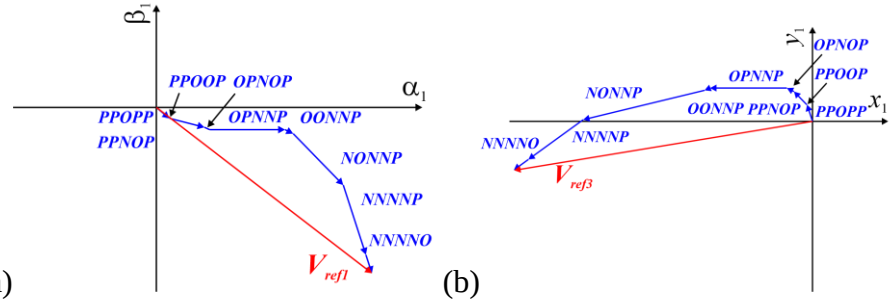
$$\begin{aligned}
&V_{x(av)} = \frac{V_{DC}}{T_s}\cdot T_{x(ON)} - \frac{V_{DC}}{T_s}\cdot T_{x(OFF)} \Rightarrow \frac{V_{dc1}}{T_s}\cdot T_{x(P)} + 0\cdot T_{x(O)} - \frac{V_{dc2}}{T_s}\cdot T_{x(N)} =\\
&= \frac{V_{dc1}}{T_s}\cdot\left(T_{x(P)} - {}_{\Delta}t_{x(O)}\cdot\frac{V_{dc2}}{V_{dc2}+V_{dc1}}\right) + 0\cdot\left(T_{x(O)} + {}_{\Delta}t_{x(O)}\right) - \frac{V_{dc2}}{T_s}\cdot\left(T_{x(N)} - {}_{\Delta}t_{x(O)}\cdot\frac{V_{dc1}}{V_{dc2}+V_{dc1}}\right) =\\
&= \frac{1}{T_s}\cdot\left(V_{dc1}\cdot T_{x(P)} - {}_{\Delta}t_{x(O)}\cdot\frac{V_{dc1}\cdot V_{dc2}}{V_{dc2}+V_{dc1}} - V_{dc2}\cdot T_{x(N)} + {}_{\Delta}t_{x(O)}\cdot\frac{V_{dc1}\cdot V_{dc2}}{V_{dc2}+V_{dc1}}\right) =\\
&= \frac{1}{T_s}\cdot\left(V_{dc1}\cdot T_{x(P)} - V_{dc2}\cdot T_{x(N)}\right);
\end{aligned} \tag{5.28}$$

This proves that the balancing procedure has not affected on the average phase voltage values. Figure 5.11 shows the vectors' positions when the balancing procedure was done and the switching sequence from Fig. 5.10 (a).



(a) (b)

Fig. 5.10. The switching pattern for three-level five-phase NPC: a) after the DC-link balancing procedure; b) with replaced zero vectors $V_{(NNN..N)}$, $V_{(PPP..P)}$ by vector $V_{(OOO..O)}$.



(a) (b)

Fig. 5.11. The resulting voltage vector in: (a) the first and (b) the second orthogonal planes.

5.4. Optimization of switching pattern

The number of the switches' commutations can be reduced when optimization procedure will be applied. The optimization part is not mandatory for successful DC-link voltage balancing or correct output voltage generation. However, the number of the active vectors used in the switching pattern can be reduced, so the switching losses might be decreased as well. In general, all the zero vectors can be treated interchangeably and can be replaced by others, regardless of their length. In the presented example, at the initial stage of the optimization procedure zero vectors $V_{(NNN..N)}$, $V_{(PPP..P)}$ should be replaced by zero vector $V_{(OOO..O)}$, as indicated in Fig. 5.10. (b). For correct vectors identification the shortest zero vectors should be chosen, (the shortest $T_{x(N)}$ for $V_{(NNN..N)}$, and $T_{x(P)}$ for $V_{(PPP..P)}$). The following equations determine the initial step of the optimization process:

$$\begin{aligned} T_{x(NNN..N)} &= T_{x(N)(\min)} = \min\left(T_{a(N)}....T_{x(N)}\right); \\ T_{x(PPP..P)} &= T_{x(P)(\min)} = \min\left(T_{a(P)}....T_{x(P)}\right); \end{aligned} \tag{5.29}$$

where x – is an inverter phase number ($x=a, b, \ldots n$), n – is a number of the inverter phases.

The next step of the optimization is to sum up all durations, when the same state, ‘P’, ‘O’, or ‘N’ are activated, as shown in Fig. 5.12. (a). This procedure keeps the average output phase voltage value unchanged. The final stage is to re-calculate the durations of the gate signals $T_{x(N)},\ldots,T_{x(N)}$, $T_{x(P)},\ldots,T_{x(P)}$, as:

$$\begin{aligned} &T_{a(N)} = T_{a(N)} - T_{x(NNN..N)}; \ldots; T_{x(N)} = T_{x(N)} - T_{x(NNN..N)}; \\ &T_{a(P)} = T_{a(P)} - T_{x(PPP..P)}; \ldots; T_{x(P)} = T_{x(P)} - T_{x(PPP..P)}; \end{aligned} \tag{5.30}$$

While the durations of the ‘O’ state can be re-calculated as:

$$\begin{aligned} &T_{a(O)} = T_{a(O)} + T_{x(NNN..N)} + T_{x(PPP..P)}; \\ &\vdots \\ &T_{x(O)} = T_{x(O)} + T_{x(NNN..N)} + T_{x(PPP..P)}; \end{aligned} \tag{5.31}$$

where $T_{x(NNN..N)}$ and $T_{x(PPP..P)}$ – are the durations of a ‘O’ state zero vectors calculated from eq. (5.29).

Figure 5.12. (b) shows the final switching sequence, with reduced number of the active vectors, while Figure 5.13 shows the positions of the resulting voltage vectors. The obtained positions of the voltage vectors at each step of the proposed algorithm demonstrate the correctness of this approach, as they remain unchanged.

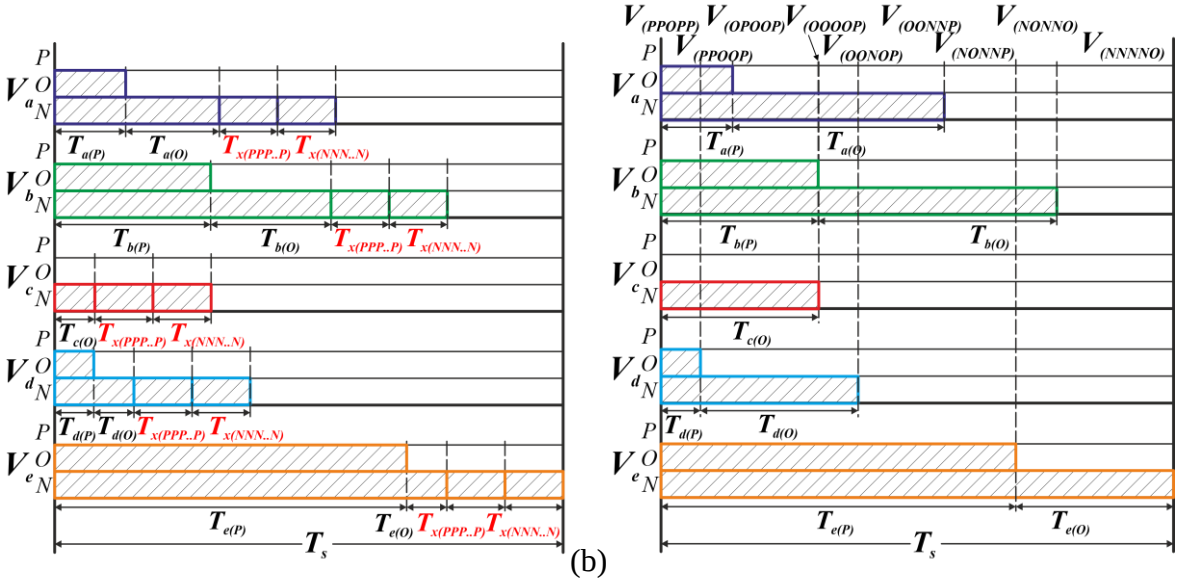
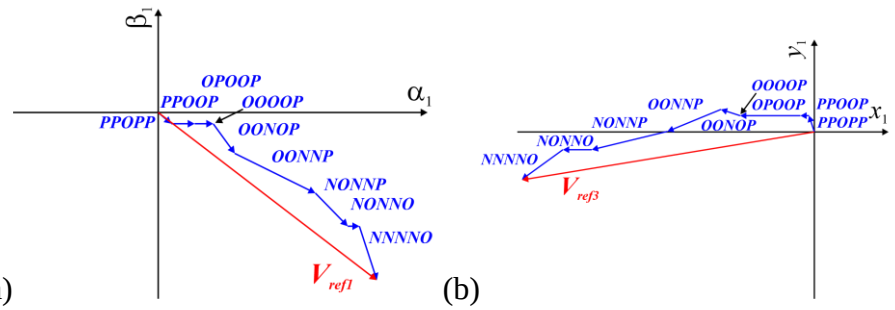


Fig. 5.12. The switching pattern for three-level five-phase NPC: a) after the same states durations grouping; b) the final, optimized, switching pattern.



(a) (b)

Fig. 5.13. The resulting voltage vector in: (a) the first and (b) the second orthogonal planes.

The final step of the modulation procedure is to activate switches for the obtained durations. All durations are related to the specified gates, so these gates receive the signal for activation for the duration defined as:

$$\begin{aligned} T_{Gx1} &= T_{x(P)}; \\ T_{Gx2} &= T_{Gx3} = T_{x(O)}; \\ T_{Gx4} &= T_{x(N)}; \end{aligned} \tag{5.32}$$

where x – is an inverter phase number (x=*a, b, … n*).

In result, each switch, including the middle ones, receive a signal of different length, which results in a stepped output voltage waveform, as shown in Fig. 3.3 (b).

Figure 5.14. shows the flow-chart representing the whole SVPWM algorithm step-by-step.

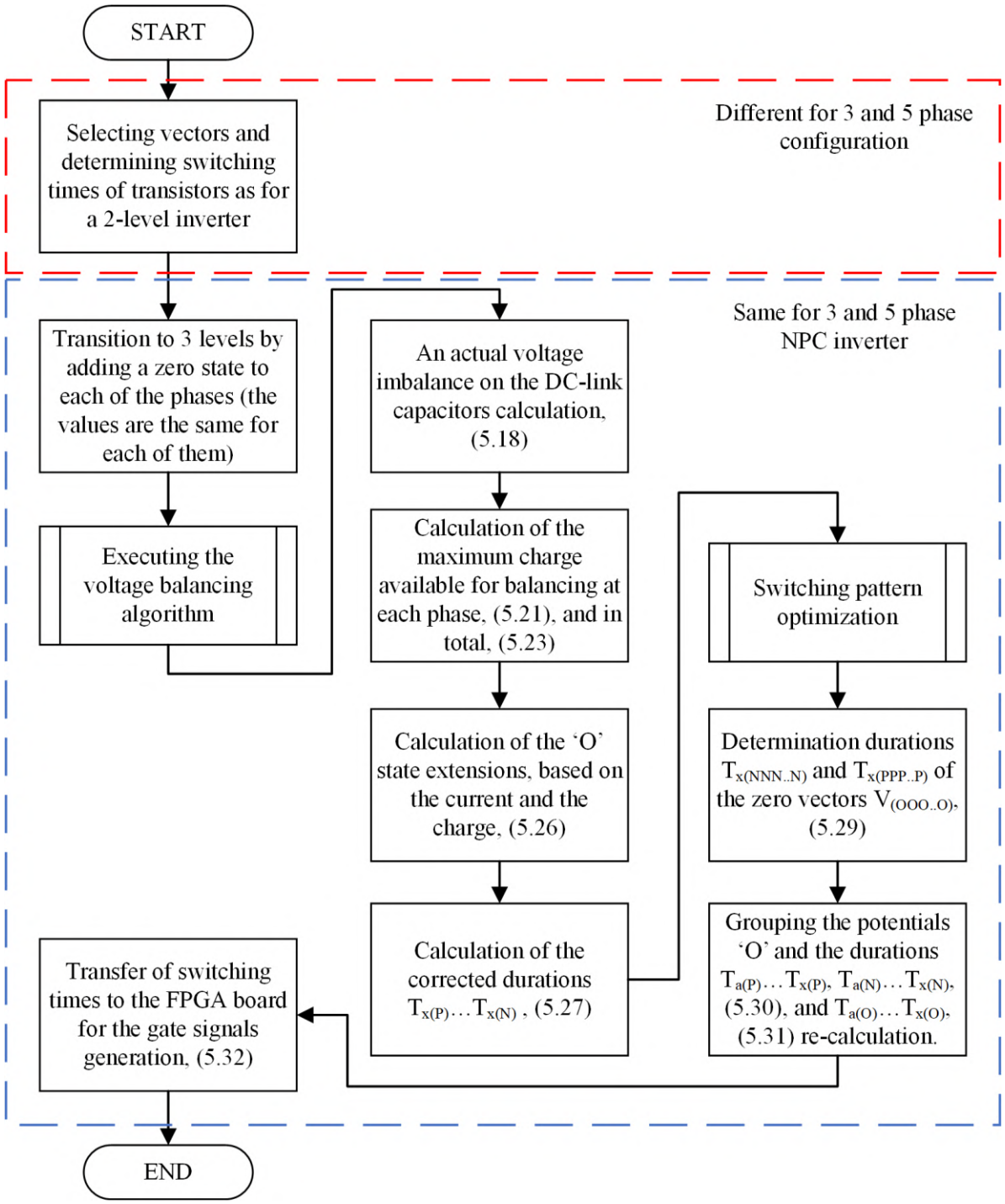


Fig. 5.14. Flow-chart for the proposed SVPWM scheme and DC-link balancing algorithm.

6. Simulation and experimental investigations

6.1. Introduction

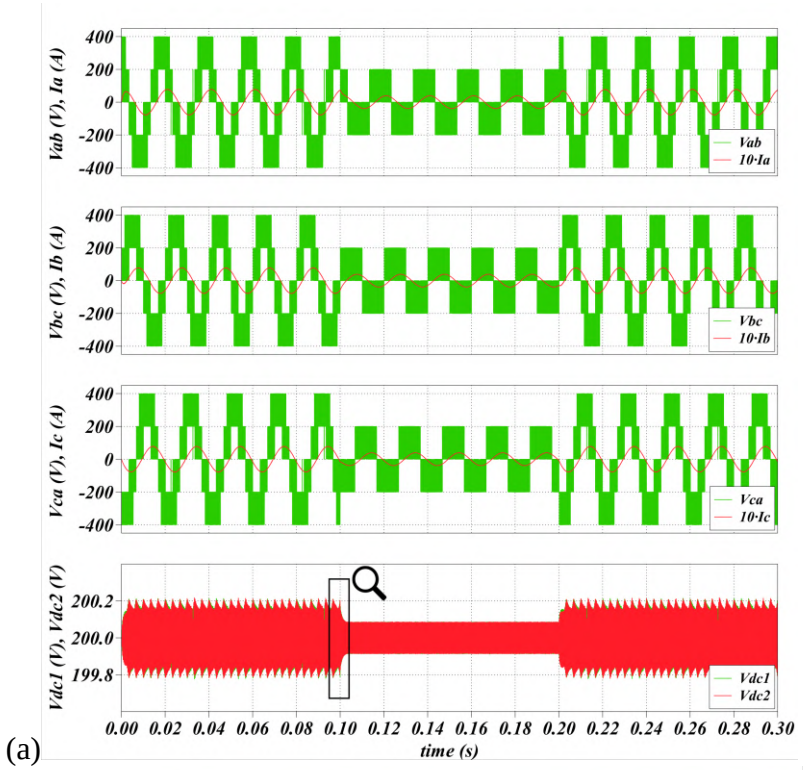
In this chapter, results of simulation and experimental research studies on the proposed modulation algorithms are presented. In section 6.4, comparison between sinusoidal and proposed space vector modulation strategies used in controlling three-phase NPC is given.

Simulation models of three- and five-phase drive systems have been developed in the PLECS software package. The experimental investigations were carried out using the inverter prototype with DSP and FPGA control boards. The hardware specifications are given in section 6.3. The developed modulation technique has the structure earlier shown in the summary section of the previous chapter.

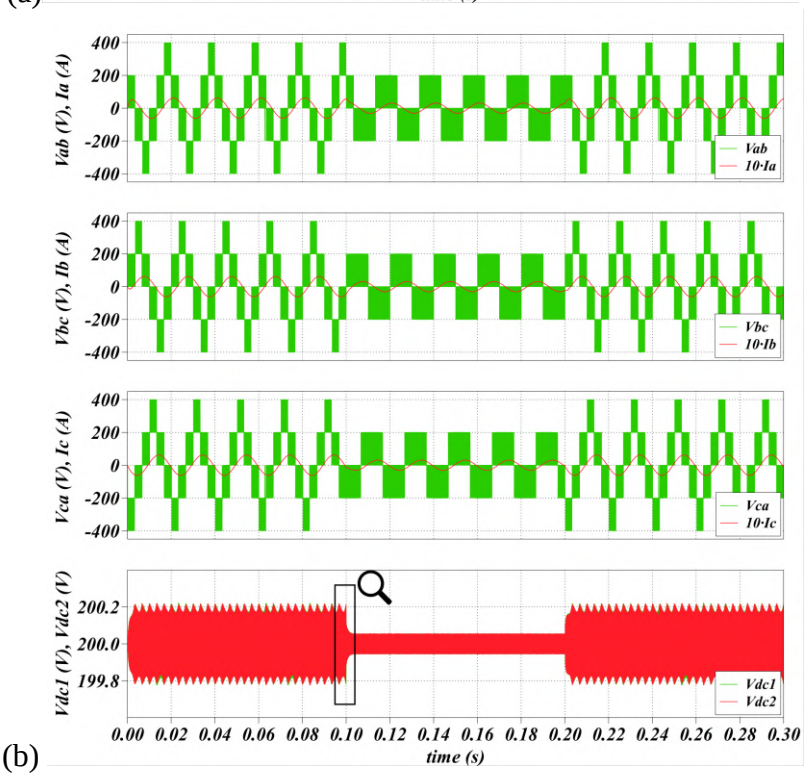
6.2. Simulation investigations

6.2.1. Three-phase NPC inverter

Simulation studies were carried out in order to showcase the system behaviors under different conditions and also to verify the assumed theoretical properties. Initially, simulation studies were provided for three-level, three-phase configurations of the NPC and F-type voltage source inverters. Then, the three-phase configuration was extended to five-phase NPC topology to prove the effectiveness of the proposed modulation technique in five-phase, three-level topology. Under different modulation indices, the behavior of the proposed modulation technique was firstly investigated. Figure 6.1. shows the dynamic system responses for step changes in modulation index; from 1 to 0.5, then back to 1 (Fig. 6.1. a) and from 0.8 to 0.4, then back to 0.8 (Fig. 6.1.(b). Figure 6.1 presents the line voltages and output current waveforms, as well as the waveforms of the upper and lower capacitor voltages. The obtained waveforms have the expected shapes, but an additional analysis of the DC-link voltages' behaviors in the transient state is required. Figure 6.2. shows zoomed portions of the DC-link voltage waveforms under the modulation index variation. Fig. 6.2. (a) and (b) were obtained for the same step change as in Fig 6.1. (a) and (b), respectively. As could be seen, the DC-link voltage variation depends on modulation index, which have an impact on the amplitude of the disturbances in the DC-link.



(a)



(b)

Fig. 6.1. The line voltages (v_{ab}, v_{bc}, v_{ca}), output currents (i_a, i_b, i_c) and DC-link capacitor voltages (v_{dC1}, v_{dC2}) waveforms under the step changes in the modulation index: (a) from 1 to 0.5 and back to 1 again; (b) from 0.8 to 0.4 and back to 0.8 again.

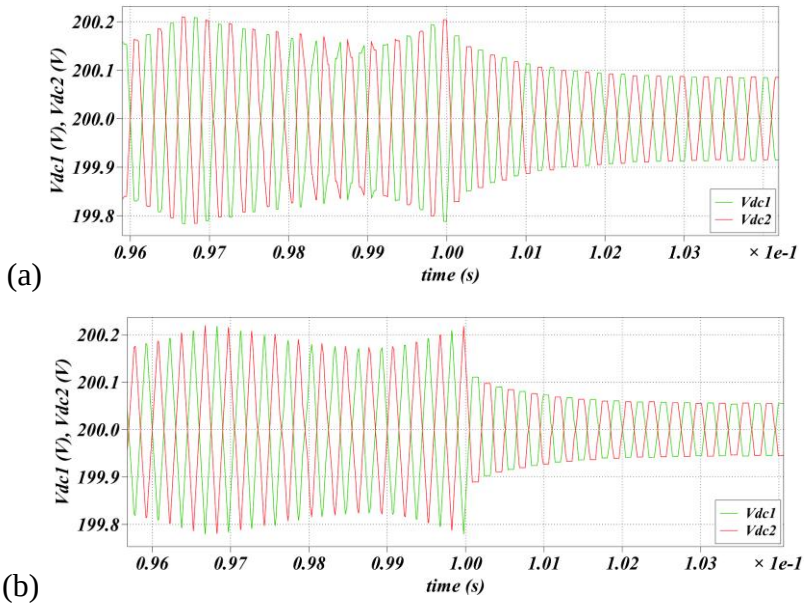


Fig. 6.2. DC-link capacitor voltages (v_{dC1}, v_{dC2}) variation during the step changes in the modulation index: (a) from 1 to 0.5 and back to 1 again; (b) from 0.8 to 0.4 and back to 0.8 again. Zoomed regions from Fig. 6.1.

The next step in the algorithm verification is to check its balancing abilities. The nature of the neutral-point clamped inverter family makes it absolutely necessary for capacitor voltages' balancing. The DC-link voltages should be balanced to provide the proper voltage waveform generations under any modulation index value, and loading conditions. For both cases, the proposed modulation technique ensures proper generation of the output voltages, for balanced and unbalanced capacitor voltages. Simultaneously, an effective balancing algorithm was introduced to the modulation strategy. Figure 6.3. shows the results of the incorporated balancing algorithm for wide range of the modulation index, from 1.15 to 0.2. The balancing performance allows for the syntheses of the output voltages without quality reduction.

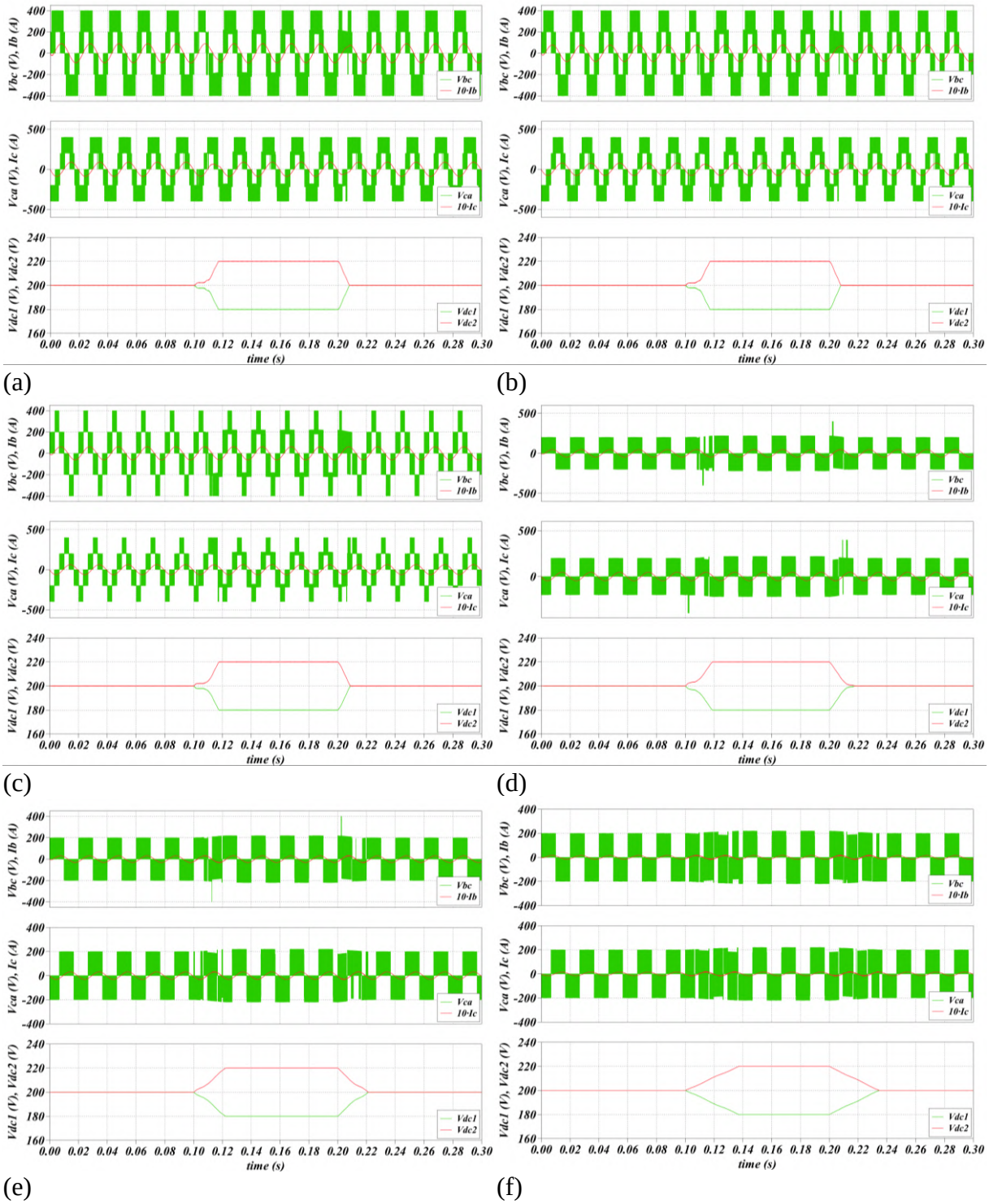


Fig. 6.3. The line voltages (v_{bc}, v_{ca}), output currents (i_b, i_c) and DC-link capacitor voltages (v_{dC1}, v_{dC2}) waveforms under the forced unbalance in the DC-link capacitor voltages, for the modulation index: (a) 1.15; (b) 1; (c) 0.8; (d) 0.6; (e) 0.4; (f) 0.2.

In order to verify the quality of the generated voltages, FFT analysis of the obtained line voltage waveform was carried out and the THD values were determined for various modulation index values; from 1.15 to 0.2. Figure 6.4. shows the line voltage, THD value and the corresponding FFT analysis. The THD values were obtained by using internal PLECS blocks.

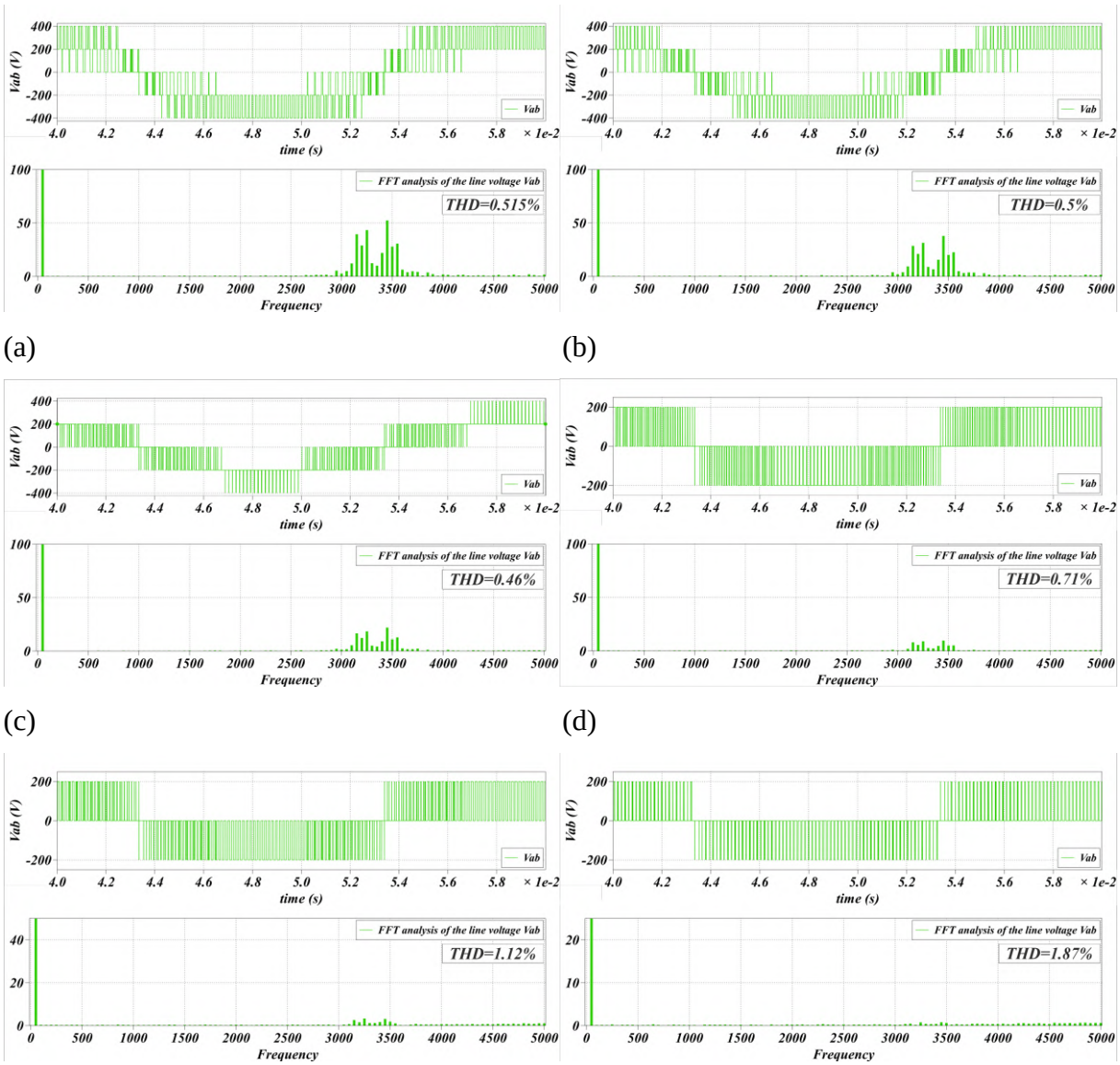


Fig. 6.4. Line voltage (v_{ab}), FFT – analysis, and calculated THD value, for the modulation index: (a) 1.15; (b) 1; (c) 0.8; (d) 0.6; (e) 0.4; (f) 0.2.

The line voltage THD value increases as the modulation index decreases. This behavior is typical for space vector and sinusoidal modulation techniques. This is due to the synthesis of low amplitude of the fundamental harmonic, when low modulation index is used. Figure 6.5. shows the variation of THD value versus the modulation index.

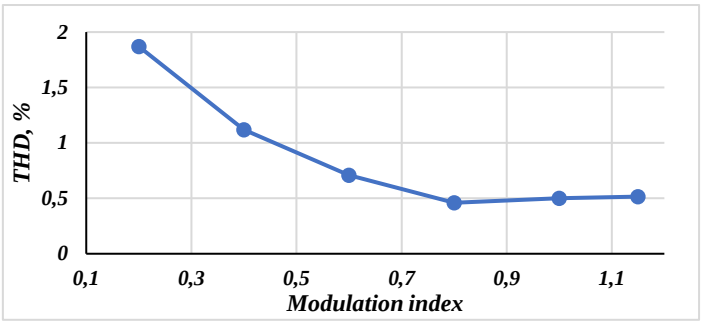


Fig. 6.5. The line voltage THD value versus the modulation index.

In a bid to improve the balancing algorithm performance (reduction of the balancing time), additional research investigation was provided. Balancing time can be reduced in the proposed modulation technique by the modification of the duration of the zero-vector introduced in the first steps of algorithm (5.14). This zero-vector was used to force the third-level utilization in all the inverter phases. Reducing its durations gives additional time that can be used for balancing purposes. Figure 6.6. shows the balancing speed for different zero-vector durations, where the modulation index was set to 0.6. As expected, the reduced zero-vector duration allows for faster balancing process; without significant changes in the THD value, as shown in Fig. 6.7.

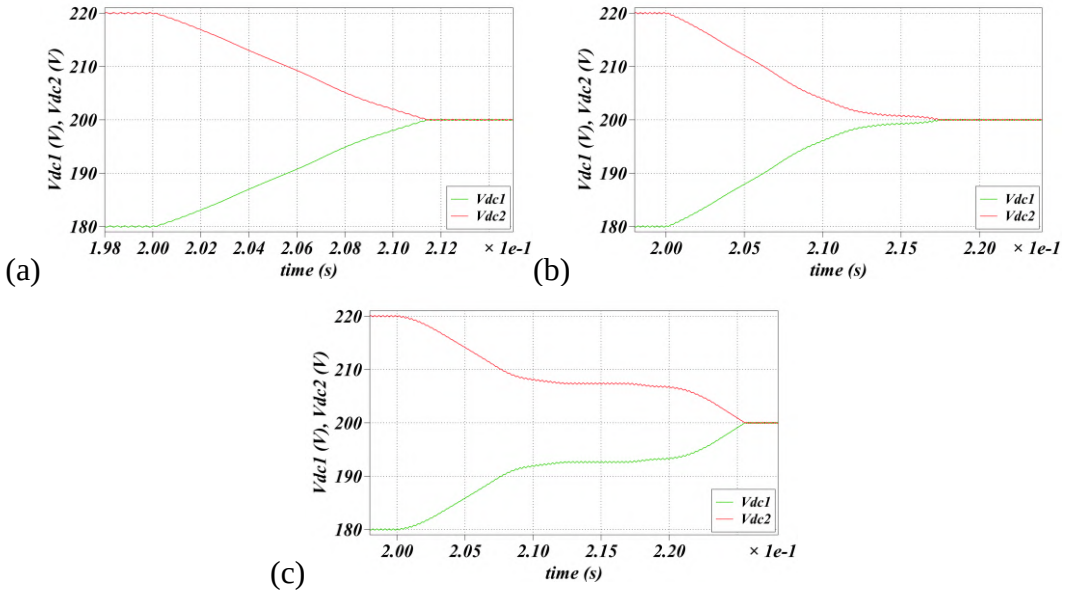


Fig. 6.6. DC-link voltages close view for different value of the initialized zero vector duration: (a) $0.01 \cdot T_s$; (b) $0.1 \cdot T_s$; (c) $0.5 \cdot T_s$.

The balancing performance was widely analyzed for three different initial value of the zero-vector duration under the experimental studies. During the simulation studies, $0.01 \cdot T_s$ was chosen. Lower values don't have significant impact on the balancing time, so this value will be chosen for investigation in five-phase configuration, as well.

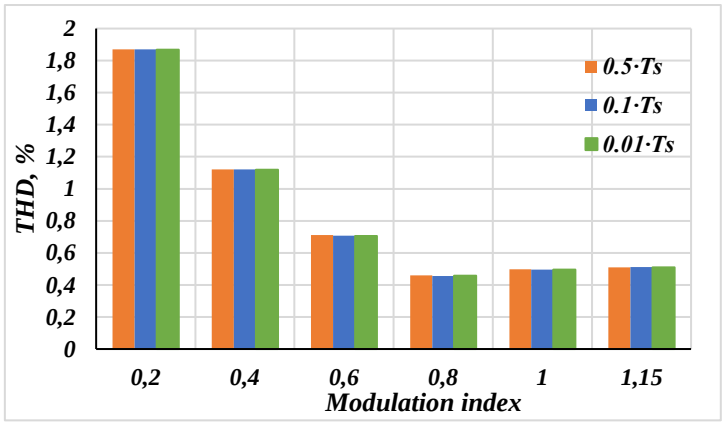


Fig. 6.7. The line voltage THD values for different initial duration of the zero vector.

6.2.2. Three-phase F-type inverter topology

The proposed modulation technique can be implemented in the F-type inverter utilizing eq. (2.10). Figure 6.8. shows the dynamic response of the three-phase, three-level F-type inverter for step changes in the modulation index; from 1 to 0.5, and back to 1 (Fig. 6.8. a), and from 0.8 to 0.4 and back (Fig. 6.8. b). Line voltages and output current waveforms, and DC-link voltages are shown therein.

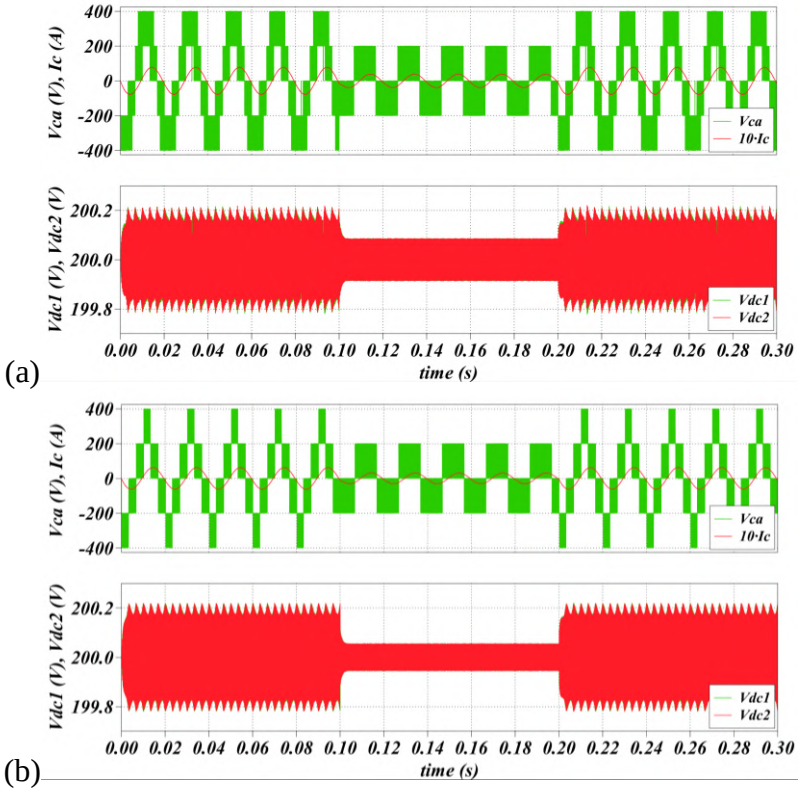


Fig. 6.8. The line voltage (v_{ca}), output current (i_c) and DC-link capacitor voltages (v_{dc1}, v_{dc2}) waveforms for the F-type inverter under step changes in the modulation index: (a) from 1 to 0.5 and back to 1 again; (b) from 0.8 to 0.4 and back to 0.8 again.

Figure 6.9. shows the system behavior, when the unbalance in DC-link was forced, for a wide range of the modulation indexes, from 1.15 to 0.2. Line and phase voltages, output current waveform and DC-link voltages are indicated.

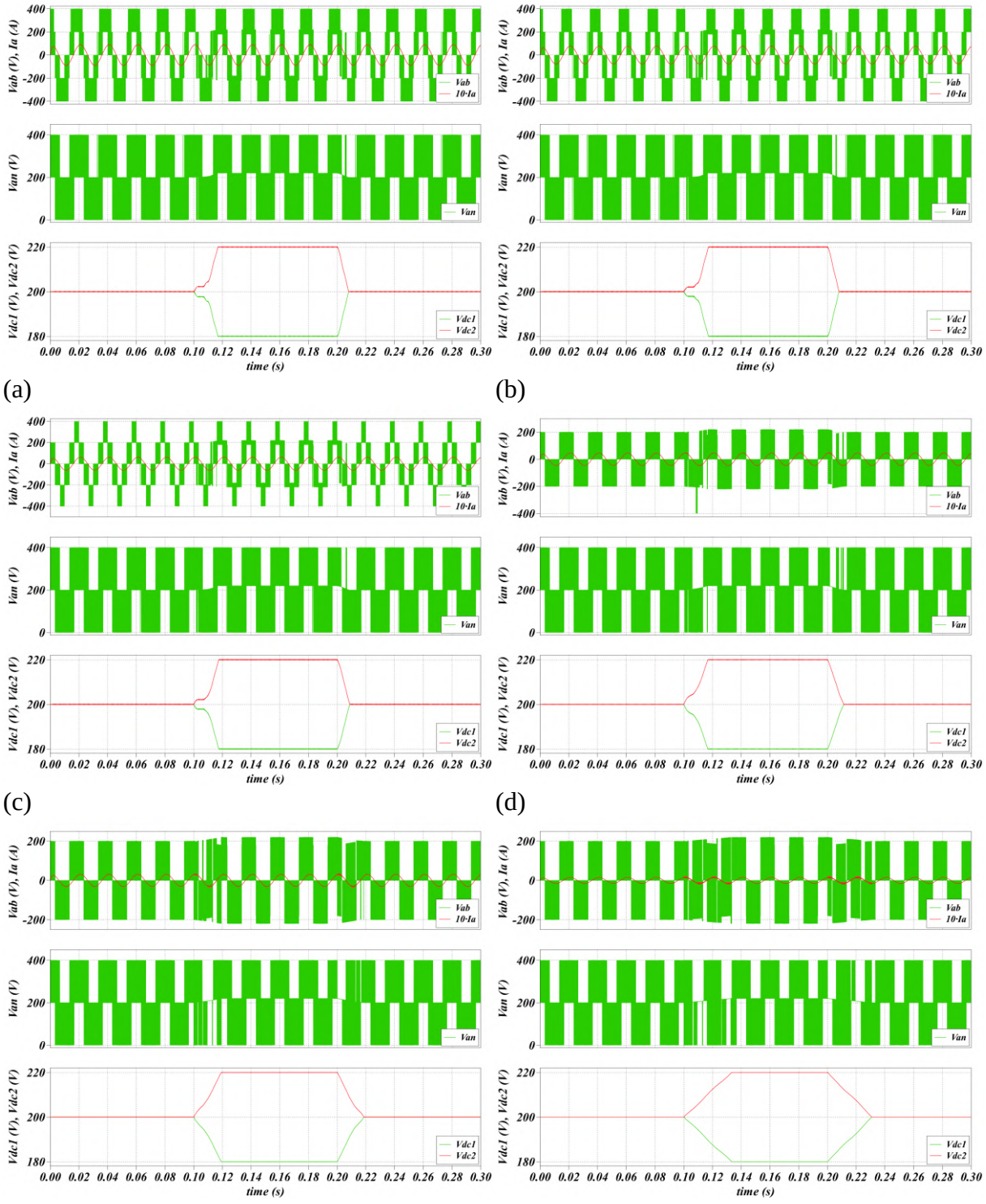


Fig. 6.9. The line voltage (v_{ab}), output current (i_a), phase voltage (v_{an}) and DC-link capacitor voltages (v_{dc1}, v_{dc2}) waveforms of the F-type inverter under the forced unbalance in the DC-link capacitor voltages, for the modulation index: (a) 1.15; (b) 1; (c) 0.8; (d) 0.6; (e) 0.4; (f) 0.2.

The FFT analysis for the output line voltage generated by F-type inverter with calculated THD values were given in Fig. 6.10. The same range of the modulation index was chosen, from 1.15 to 0.2, as in NPC topology. The simulation results for the F-type inverter were summarized and shown in Fig. 6.11. The THD values are given in Fig. 6.11.

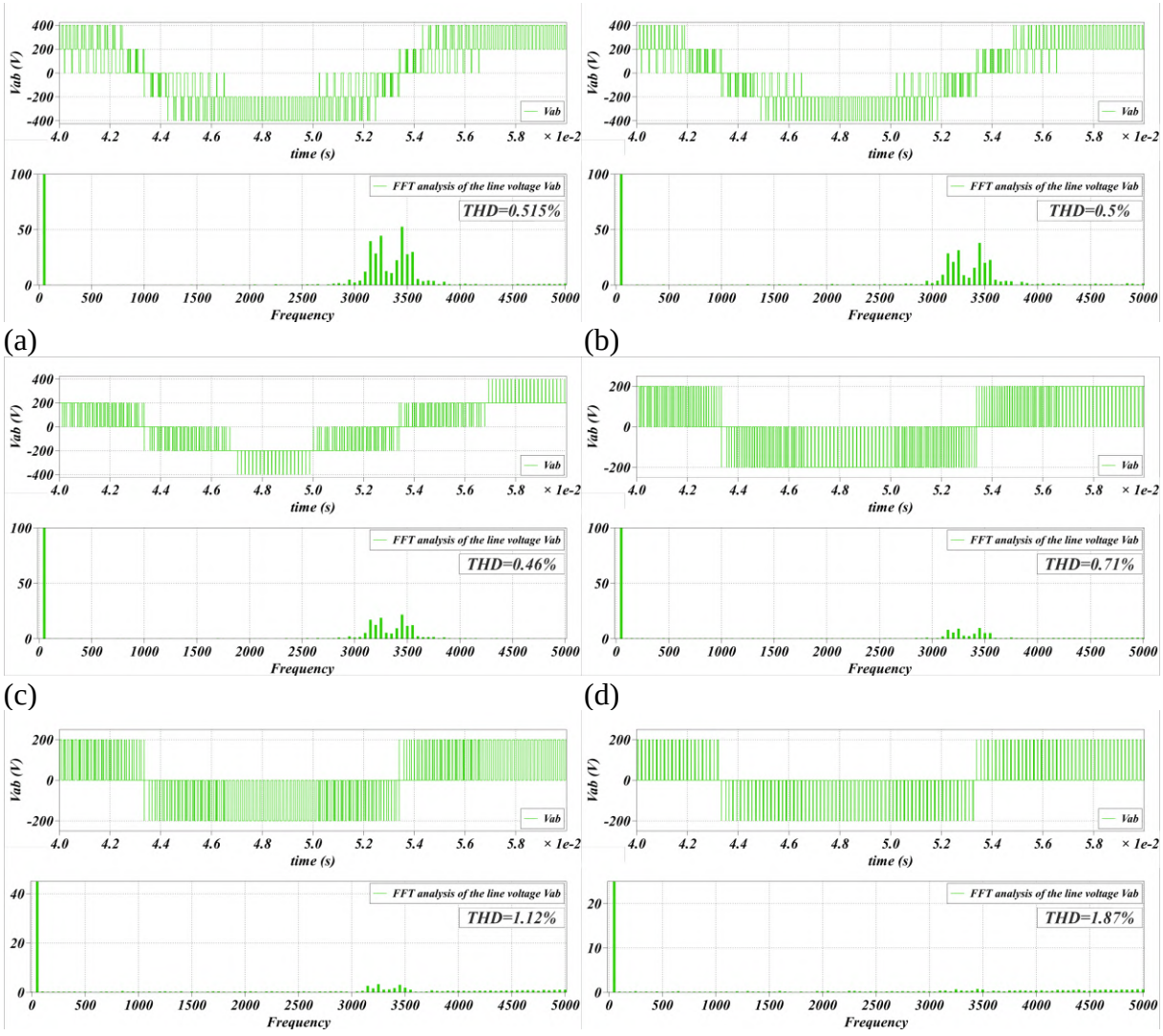


Fig. 6.10. F-type inverter, the line voltage (v_{ab}), FFT – analysis, and calculated THD value, when the modulation index is equal to: (a) 1.15; (b) 1; (c) 0.8; (d) 0.6; (e) 0.4; (f) 0.2.

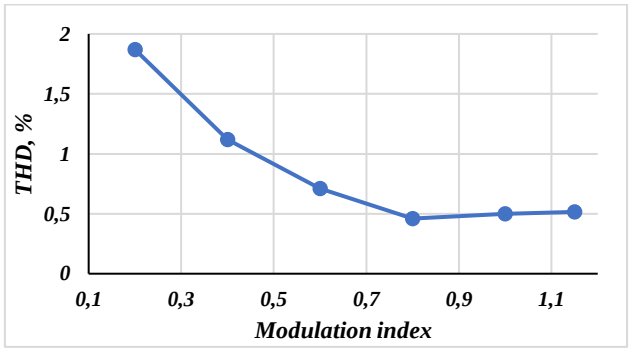


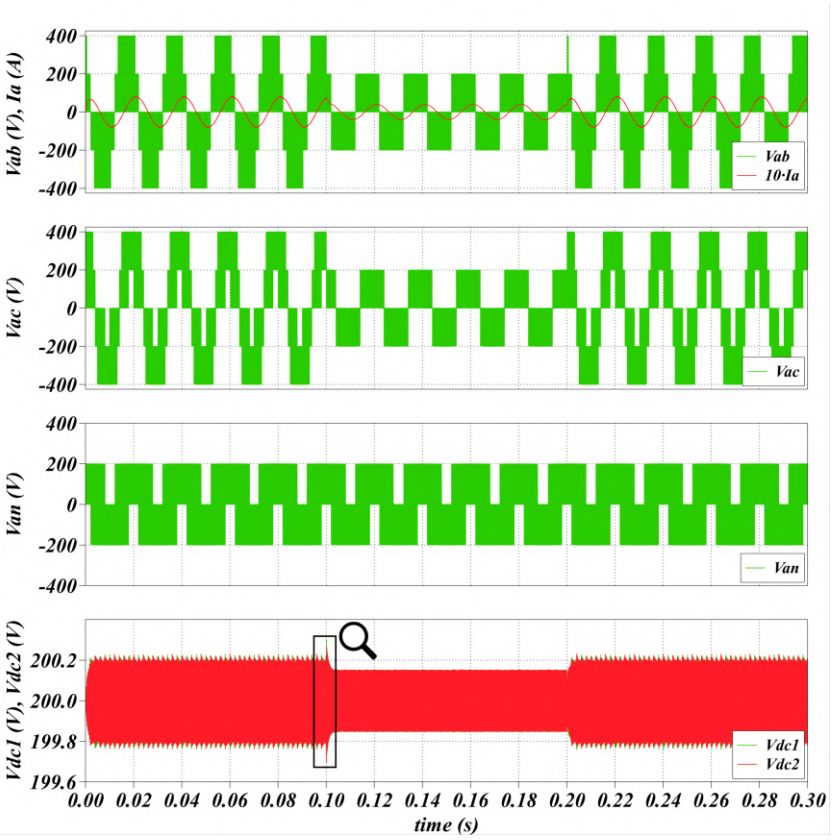
Fig. 6.11. The line voltage THD value versus the modulation index for F-type inverter.

As expected, proposed modulation technique achieves the same results for both topologies. Moreover, the same gate signals might be used for T-type inverter, as well. This behavior can be explained by the nature of the neutral-point clamped topology family. The THD values and balancing times are the same for both topologies, so the quality of generated voltages is the same.

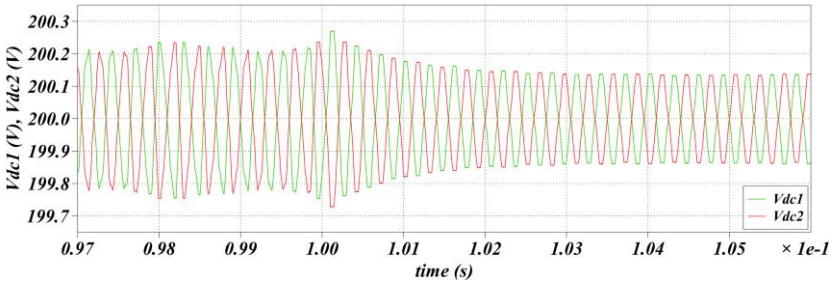
6.2.3. Five-phase NPC inverter

The modulation algorithm was modified for a five-phase, three-level NPC inverter. All previously described dependencies are also applicable here, and should be taken into account for proper adjustment of the balancing dynamics of the DC-link voltages. However, in multiphase multilevel configuration, the advantages of the proposed approach (two-level initial procedure) became clearly visible. The same initial step of the modulation algorithm in three- and two-level configurations allows for reduction of the execution time. The proposed approach avoids the problem with large number of space vectors and their selection. It results in significant decrease of the SVPWM strategy complexity

Figure 6.12. shows the dynamic response of the five-phase inverter for step changes in the modulation index; while Fig. 6.12. (b) shows zoomed DC-link voltage waveforms in the transient state. Figure 6.13. shows the system behavior, when an imbalance in DC-link was forced, for a wide range of the modulation indexes; from 1.05 to 0.2.



(a)



(b)

Fig. 6.12. The line voltages (v_{ab}, v_{ac}), output current (Ia), phase voltage (v_{an}) and DC-link capacitor voltages (v_{dC1}, v_{dC2}) waveforms for a five-phase NPC inverter: (a) under step changes in the modulation index from 0.8 to 0.4 and back to 0.8 again; (b) fluctuation of the DC-link voltages.

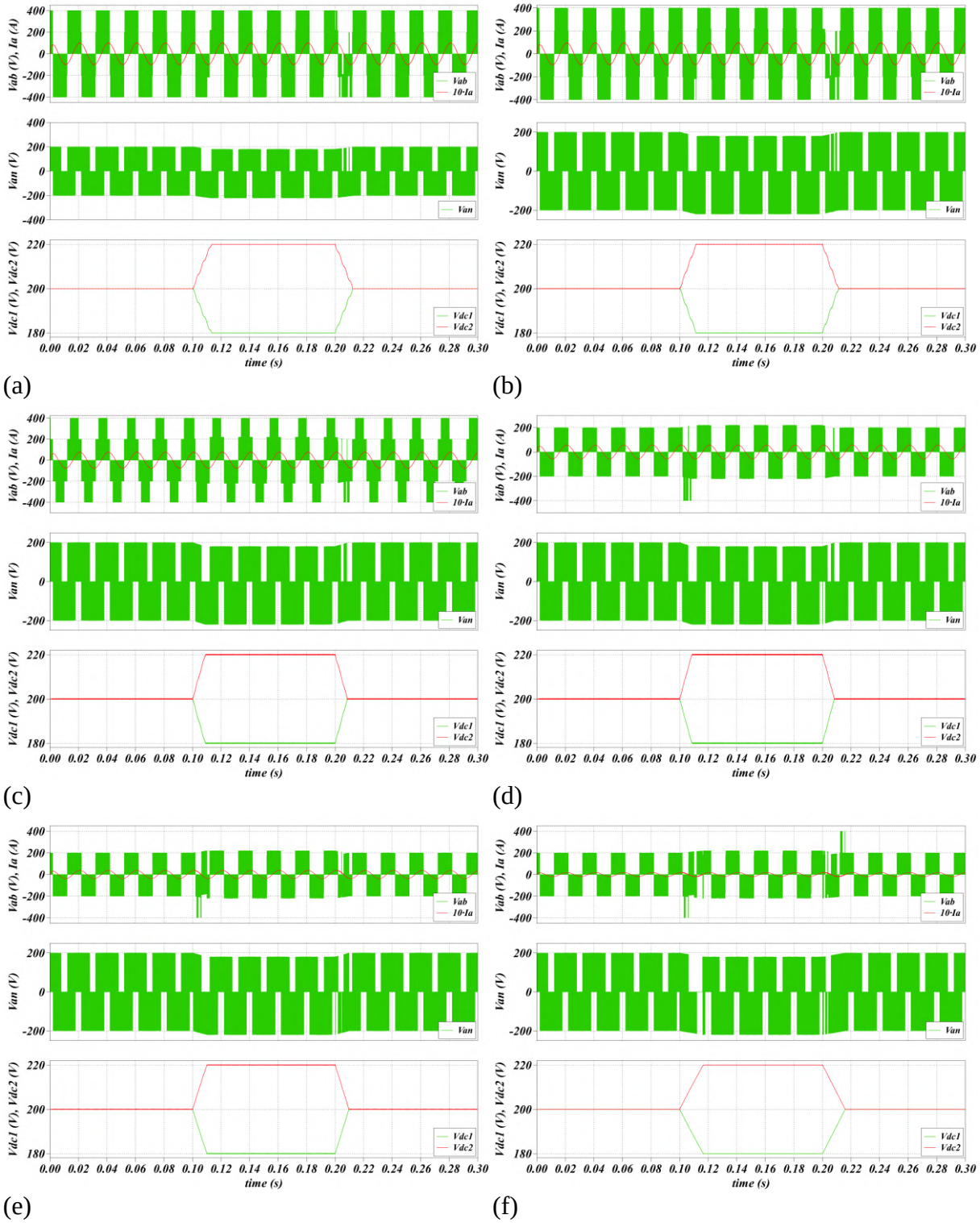


Fig. 6.13. The line voltage (v_{ab}), output current (i_a), phase voltage (v_{an}) and DC-link capacitor voltages (v_{dC1}, v_{dC2}) waveforms of the five-phase NPC inverter under the forced unbalance in the DC-link capacitor voltages, for the modulation index: (a) 1.05; (b) 1; (c) 0.8; (d) 0.6; (e) 0.4; (f) 0.2.

The presented waveforms prove the effectiveness of the modulation algorithm in output voltage generations, as well as, in DC-link voltage balancing for a five-phase NPC inverter. To verify the quality of the generated voltage, the line voltage FFT-analysis was provided and the

corresponding THD value was determined. Figure 6.14. shows the FFT analysis for a wide range of the modulation index (from 1.05 to 0.2), while Fig. 6.15. contains summarized results for five-phase inverter. The THD and balancing time are shown in Fig. 6.15. (a) and (b), respectively.

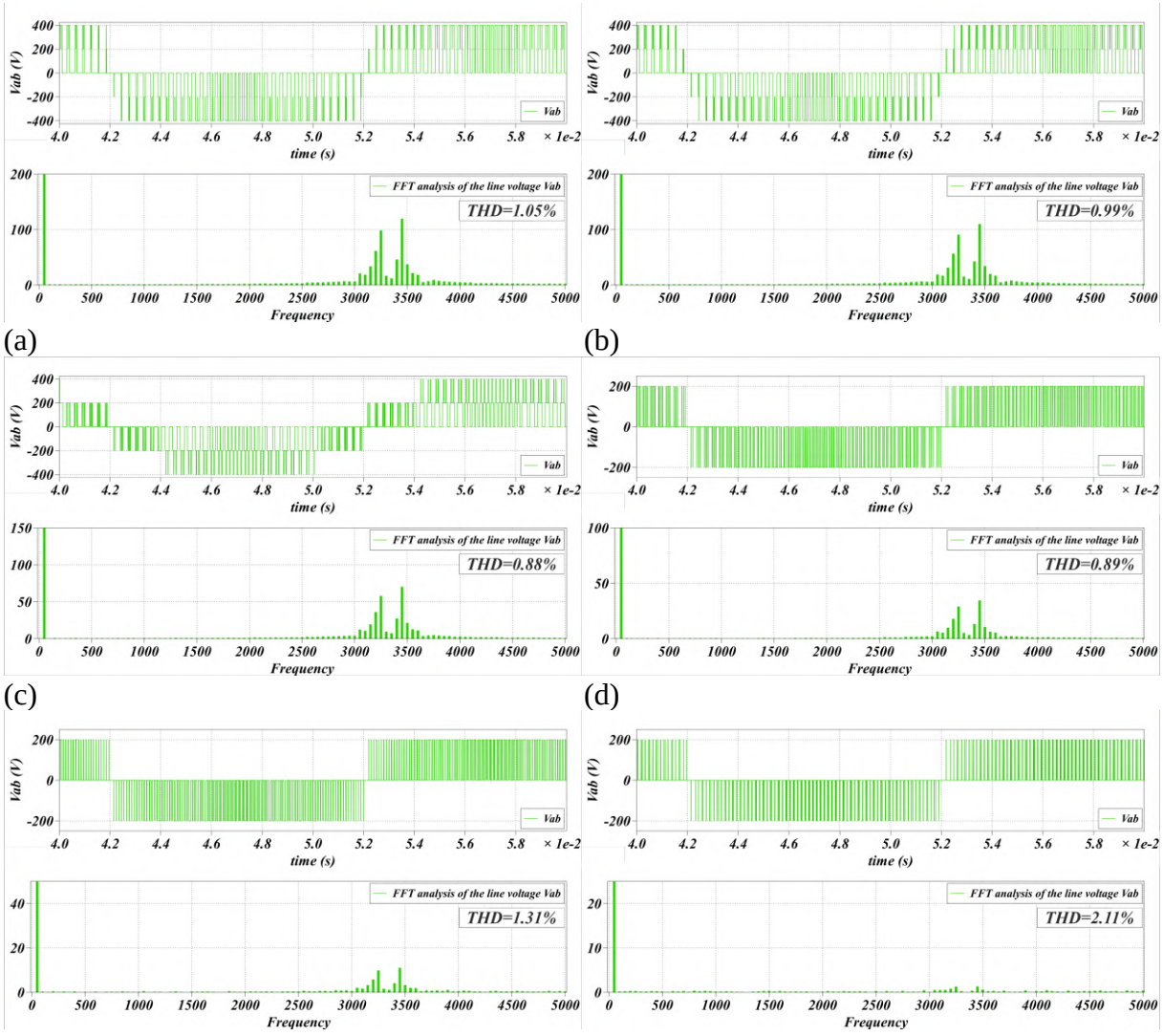
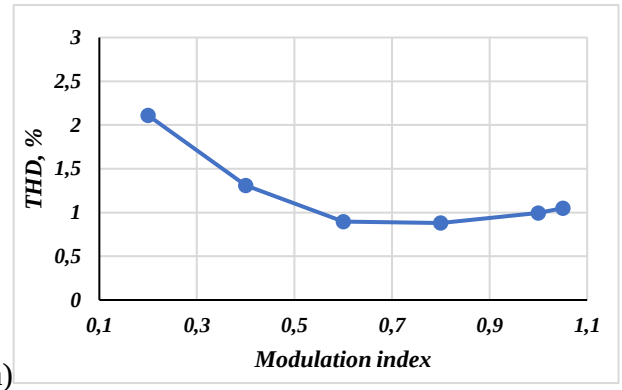
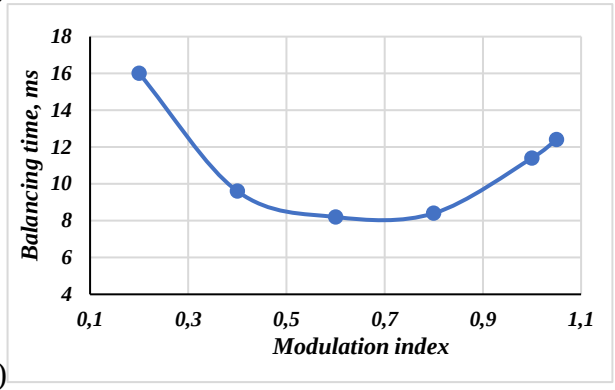


Fig. 6.14. Five-phase NPC inverter, the line voltage (v_{ab}), FFT analysis, and calculated THD value, when the modulation index is equal to: (a) 1.05; (b) 1; (c) 0.8; (d) 0.6; (e) 0.4; (f) 0.2.



(a)



(b)

Fig. 6.15. The line voltage THD value (a) and balancing time (b) versus the modulation index for five-phase NPC inverter.

Important feature of the multiphase systems is the possibility of additional voltage harmonic generations. These harmonics should be controlled by modulation algorithm and might be used for increasing the electromagnetic torque in IM motor; or for independent controlling the multimotor drive systems, when several motors are supplied from single VSI. During the simulation studies presented previously, proposed modulation algorithm was used to generate only one output voltage vector related to fundamental, (or first), harmonic. To verify the effectiveness of the proposed SVPWM technique in the independent control of many output voltage vectors, the additional voltage vector with four times higher frequency (forth harmonic) was generated. The additional harmonic of fourth order is not natural to five-phase VSI, but of course, 3rd harmonic is. However, this unnatural harmonic order was chosen to emphasize the ability of independent generation of the output voltages. During the simulation studies, the fundamental frequency was set to 50Hz, so the fourth harmonic frequency was 200Hz. Fig. 6.16. shows the dynamic response of the five-phase inverter for step changes in the modulation index related to the fundamental harmonic voltage, from 0.6498 to 0.325, and back to 0.6498; while the modulation index of the fourth harmonic voltage is constant and equal to 0.6498, [55], [122].

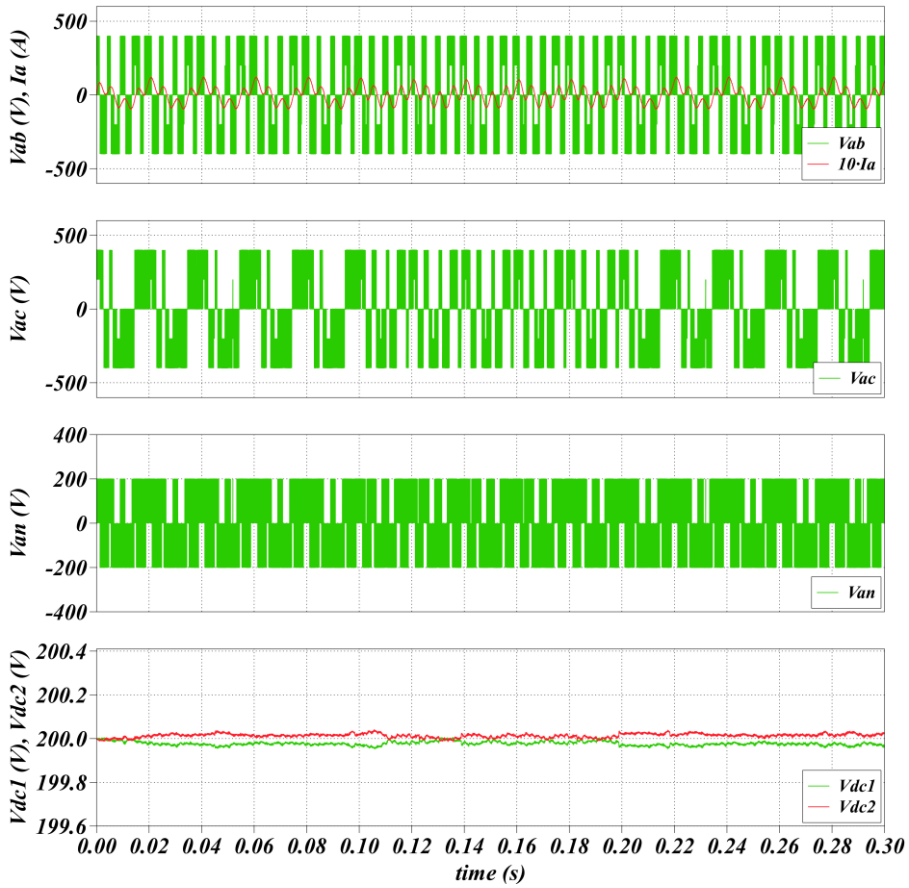


Fig. 6.16. The line voltages (v_{ab}, v_{ac}), output current (i_a), phase voltage (v_{an}) and DC-link capacitor voltages (v_{dc1}, v_{dc2}) waveforms for a five-phase NPC inverter under step changes in modulation index of fundamental harmonic voltage: from 0.6498 to 0.325 and back to 0.6498.

Figure 6.17. shows the balancing abilities of the modulation algorithm when there is forced DC-link voltage imbalance. The balancing speeds for various modulation index values for the fundamental harmonic voltage (from 0.6498 to 0.1), and fourth harmonic voltage (0.6498) are given in Fig. 6.17.

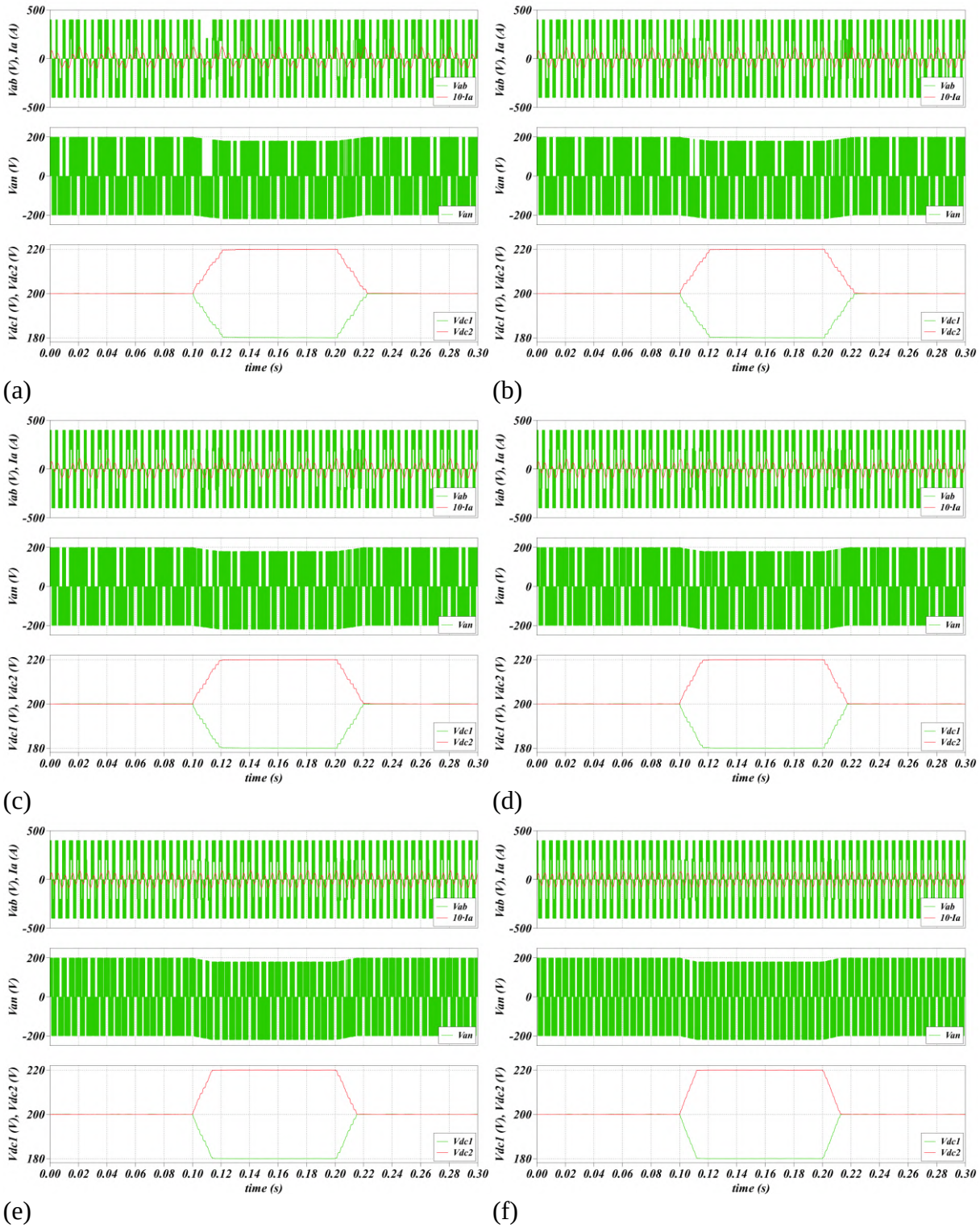


Fig. 6.17. The line voltage (v_{ab}), output current (i_a), phase voltage (v_{an}) and DC-link capacitor voltages (v_{dc1}, v_{dc2}) waveforms of the five-phase NPC inverter under the forced unbalance in the DC-link capacitor voltages, when the modulation index of fundamental harmonic voltage is equal to: (a) 0.6498; (b) 0.5; (c) 0.4; (d) 0.3; (e) 0.2; (f) 0.1. The modulation index of fourth harmonic voltage is 0.6498.

The FFT analyses were provided for modulation indexes chosen previously. Figures 6.18. and 6.19. show the line voltage and phase voltage FFT analyses, respectively. The THD value

was not calculated due to lack of standardized calculation method for a waveform with several desirable harmonics. For a five-phase inverter, two desirable harmonics were generated.

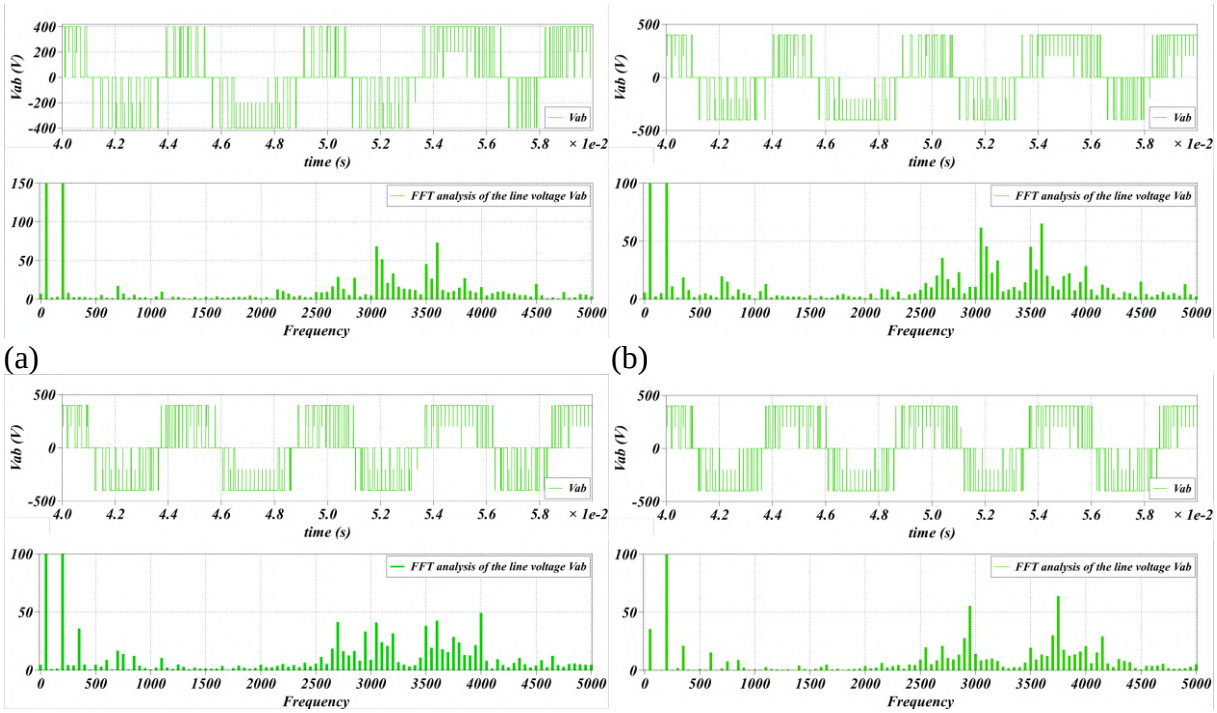


Fig. 6.18. Line voltage (v_{ab}) and FFT analysis, when the modulation index of the fourth harmonic voltage is 0.6498 and of the first harmonic voltage: (a) 0.6498; (b) 0.5; (c) 0.3; (d) 0.1.

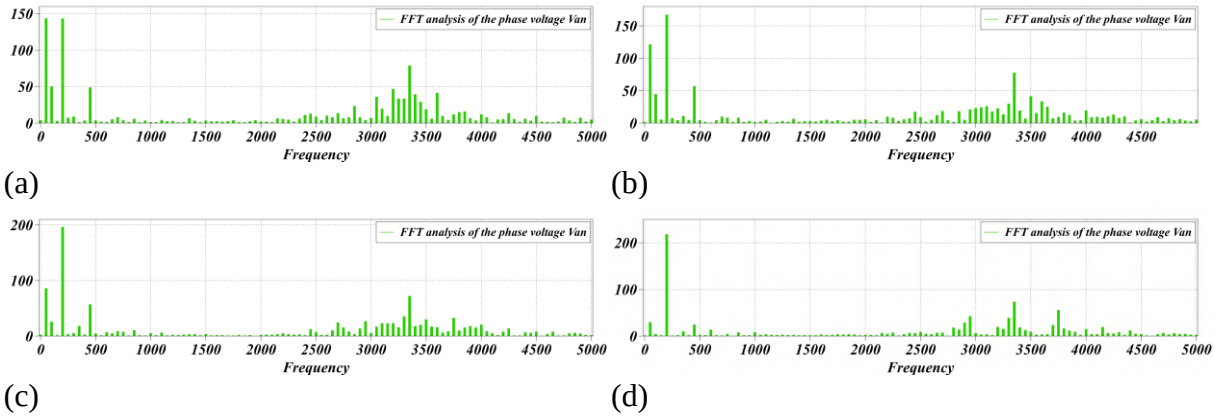


Fig. 6.19. The phase voltage (v_{an}) FFT analysis, the modulation index of the fourth harmonic voltage is 0.6498 and of the first harmonic voltage: (a) 0.6498; (b) 0.5; (c) 0.3 (d) 0.1.

The amplitudes of the first and fourth harmonic components are the same, when the modulation indexes are equal to 0.6498 for both voltages, as shown in Fig. 6. 19. (a). This result proves the correctness of the output voltage generation. The independent control of the additional harmonics was tested by the dynamic change in the order of generated harmonics, from four to six times higher than fundamental frequency. Fig. 6.20. shows the dynamic

response of the five-phase inverter for step changes in the additional harmonic frequency, while the first harmonic frequency is constant.

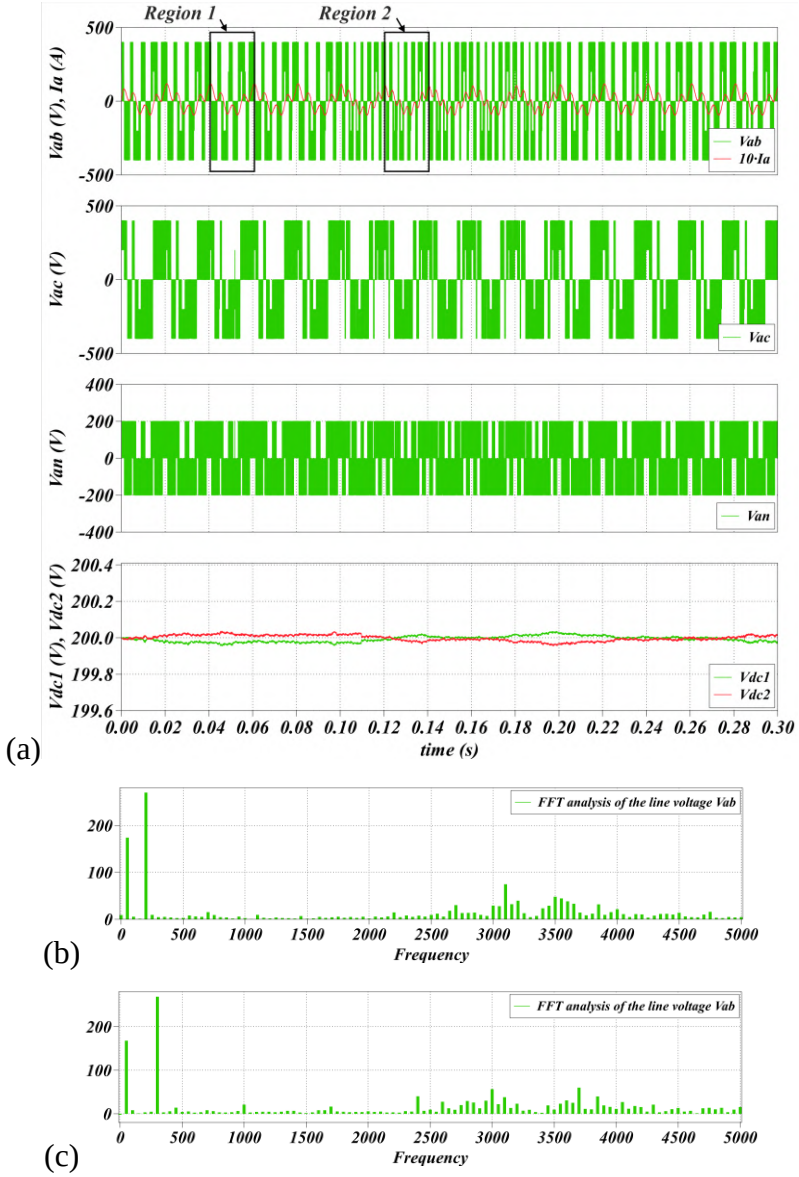


Fig. 6.20. (a) The line voltage (v_{ab}, v_{ac}), output current (i_a), phase voltage (v_{an}) and DC-link capacitor voltages (v_{dC1}, v_{dC2}) waveforms of the five-phase NPC inverter for the change in the additional harmonic frequency from 200 Hz to 300 Hz, the modulation indexes are equal to 0.6498. The FFT analysis for: (b) the region 1 and (c) 2 from Fig. 6.20.(a).

As expected, the simulation studies proved the effectiveness of the proposed technique in three- and five-phase configurations; for NPC inverter and three-phase F-type inverter topologies.

6.3. Experimental investigations

6.3.1. Structure of the experimental laboratory setup

Experimental studies were carried out on a laboratory prototype inverter connected to an RL load. This inverter prototype was developed and built as a three-level, five-phase NPC inverter. However, it can be used in various configurations: as NPC, F-type, and T-type inverter. Phase number can also be reduced, so three- and single-phase systems can be tested, as well. The laboratory prototype is shown in Fig. 6.21. Developed prototype inverter utilize DSP and FPGA control boards. The DSP (ADSP21363L) processor is responsible for the superordinate control (control system, observer structures, etc.) and modulation algorithms executions; providing corresponding calculations. The FPGA (Altera Cyclone II EP2C8F256I8) is used to control the digital-to-analog converters (DAC) and power switches. The hardware specifications and load parameters are given in Table I.

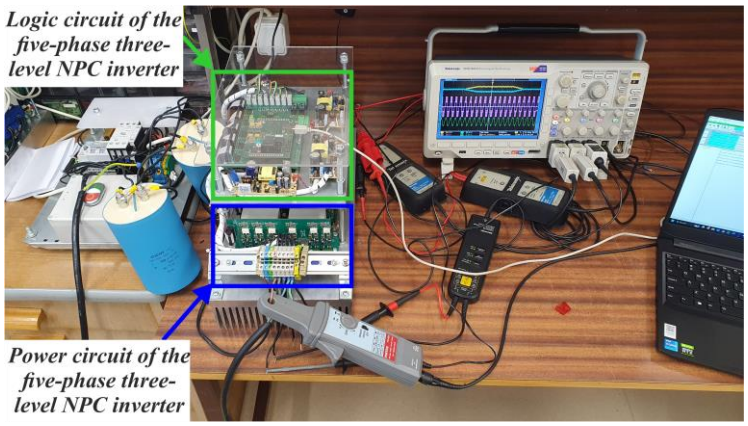


Fig. 6.21. The laboratory prototype five-phase, three-level inverter.

Table I. Experimental setup specification

Component	Specification
Power switches	NGTB25N120FL3WG
Switching frequency	$3.3kHz$
Capacitor banks, C_1, C_2	$500\mu F$, $600V$
RL load	20Ω, $20mH$
DC-link voltage	$360V$

The modulation technique was implemented on the prototype setup and the same investigations, as in section 6.2., were repeated.

6.3.2. Experimental results

The main goal of the experimental studies is to provide proof of concept and validate the effectiveness of the proposed modulation technique. Simultaneously, the validity of the simulation results was verified. Figure 6.22. shows the dynamic response of the three-phase inverter for modulation index change, from 1 to 0.5, and back to 1. Line voltage, output current and DC-link capacitor voltages are shown.

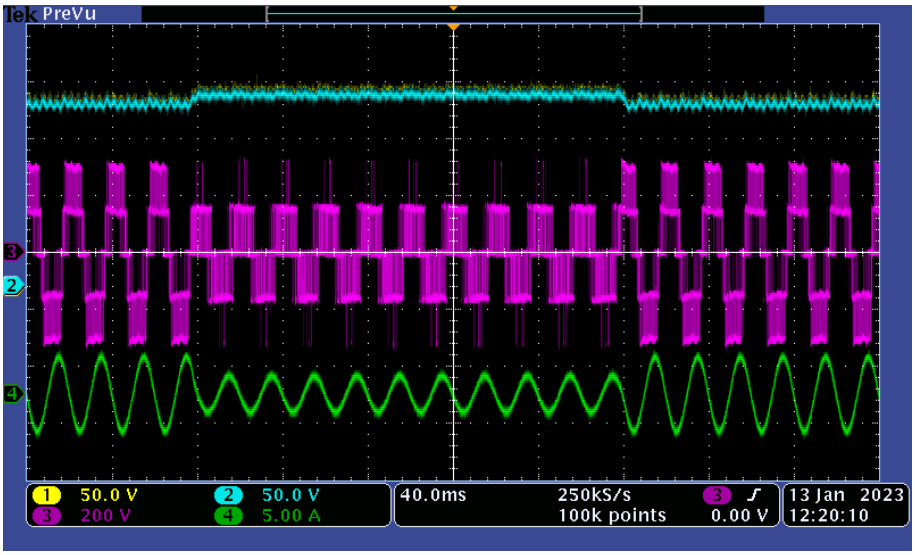


Fig. 6.22. The line voltage v_{ab} (3), output current i_a (4) and DC-link capacitor voltages v_{dC1} (1), v_{dC2} (2) waveforms of the three-phase NPC inverter for step changes in the modulation index, from 1 to 0.5 and back to 1 again.

Figure 6.23. shows the system behavior, when imbalance in DC-link voltage was forced; for a wide range of the modulation indexes (from 1.15 to 0.2). Line voltage, output current waveform and DC-link capacitor voltages are indicated in Fig. 6.23. The same voltage imbalanced (40 *V)* was forced; as in simulation studies. The initial duration of the zero-vector has an impact on the balancing time, as shown in section 6.2. Here, for experimental purpose, the zero-vector duration was set as $0.01 \cdot Ts$. System behavior comparison, when different durations were chosen, will be shown later in this section. The initial zero-vector duration effect on the THD value will also be given next.

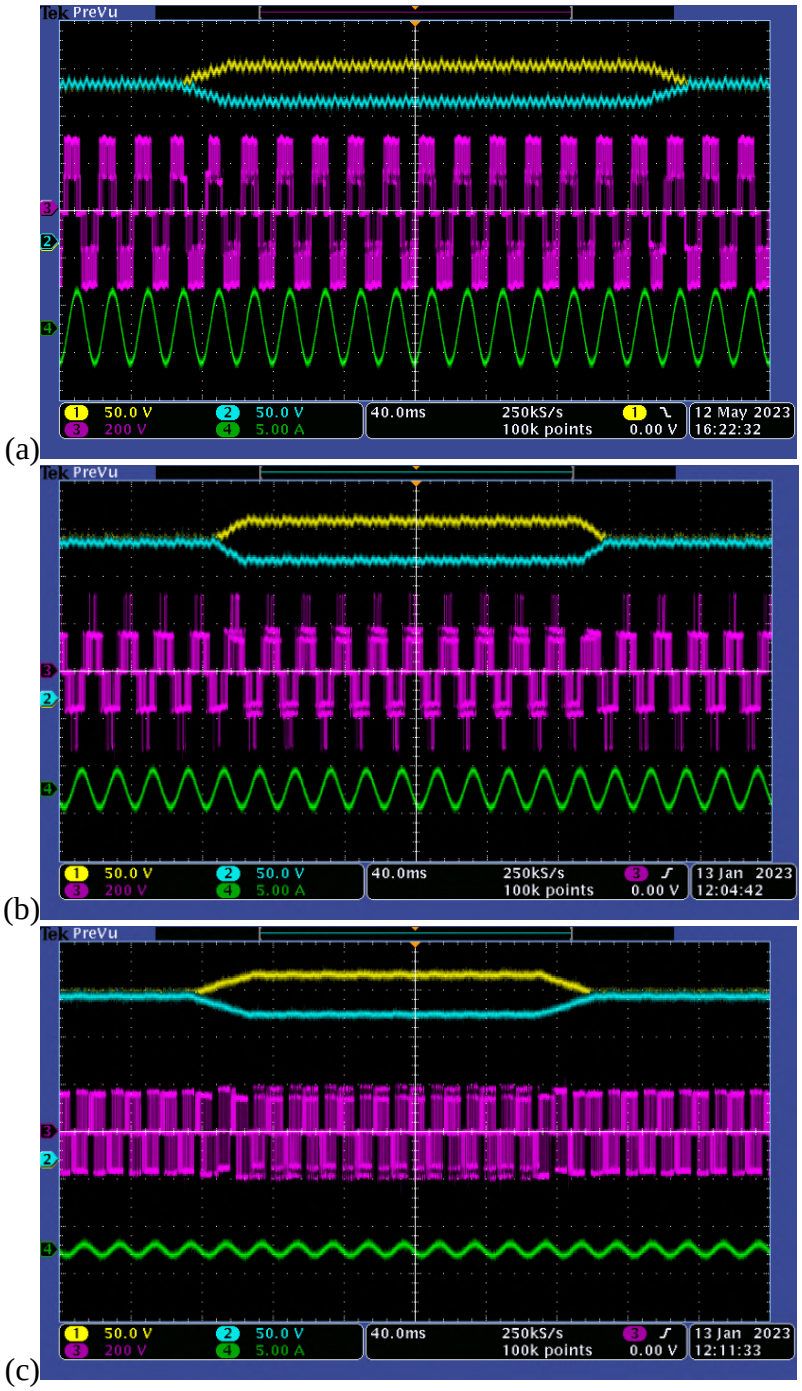


Fig. 6.23. Dynamic response of the three-phase NPC inverter for the forced unbalance in the DC-link voltages, when the modulation index is equal to: (a) 1.15; (b) 0.6; (c) 0.2. The line voltage v_{ab} (3), output current i_a (4) and DC-link capacitor voltages v_{dC1} (1), v_{dC2} (2).

The initial zero-vector duration decides the dynamics of the balancing process, as shown in Fig. 6.6. The experimental validation was done for various values of the initial zero-vector duration. Figures 6.24. show the zoomed view of the DC-link voltages, when the zero-vector duration was set to: $0.01 \cdot Ts$, $0.1 \cdot Ts$, $0.2 \cdot Ts$, in Fig. 6.24. (a), (b) and (c) respectively. The summarized results of the balancing time investigation are given in Fig. 6.25, where the

balancing-time dependencies on the modulation index, for different initial zero vector durations, are shown.

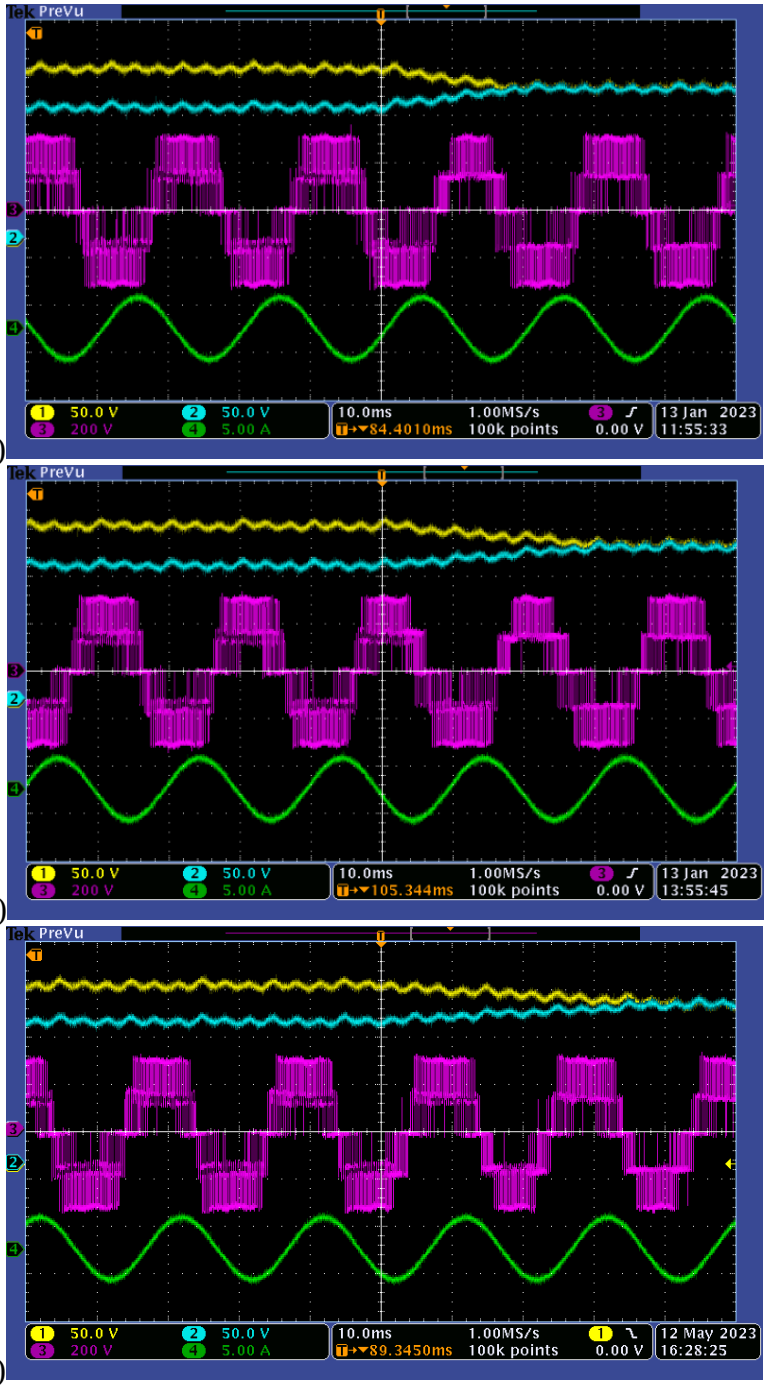


Fig. 6.24. DC-link capacitor voltages balancing in three-phase inverter, when the modulation index is equal to 1 and the initial duration of the zero vector is: (a) 0.01·*Ts*; (b) 0.1·*Ts*; (c) 0.2·*Ts*. The line voltage v_{ab} (3), output current i_a (4) and DC-link capacitor voltages v_{dC1} (1), v_{dC2} (2) waveforms.

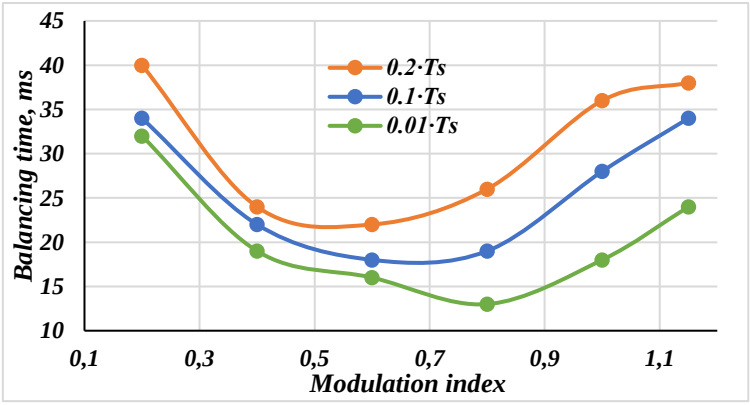


Fig. 6.25 The balancing time dependencies on the initial zero vector duration.

The FFT analysis of the line voltage is given in Fig. 6.26.; line voltage THD values are indicated therein. Line voltage, output current waveform and DC-link voltages were shown, additionally in Fig. 6.26. Results shown in Fig. 6.26. were obtained when the initial zero-vector duration was equal to 0.01·*Ts*. The provided FFT analyses were done for modulation index range of 1.15 to 0.2. Obtained results were summarized in Fig. 6.27., where the line voltage THD dependencies, for same values of initial zero-vector duration of the (0.01·*Ts*, 0.1·*Ts*, 0.2·*Ts*), are given.

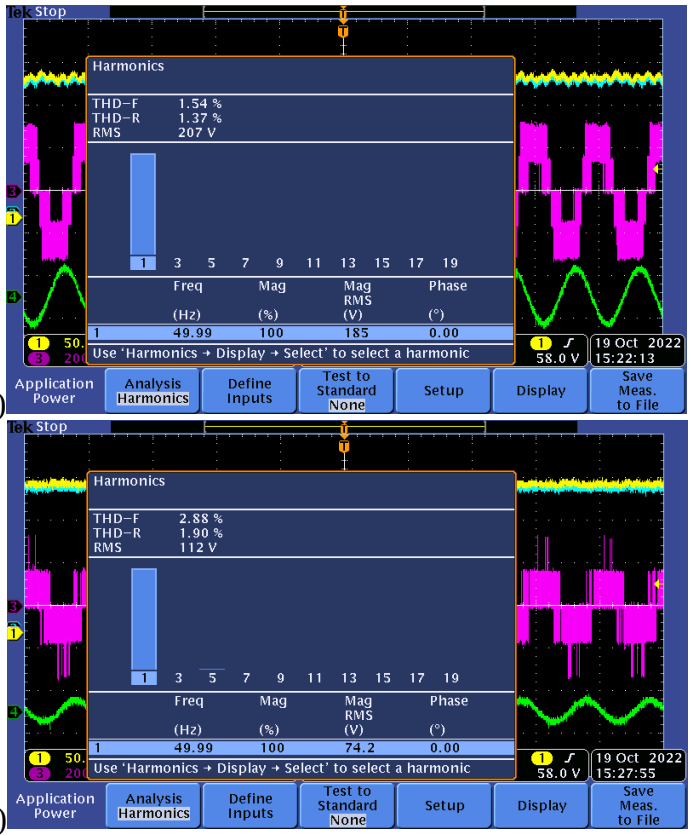


Fig. 6.26. The FFT analysis of the line voltage and obtained THD value in three-phase inverter, when the modulation index is equal to: (a) 1; (b) 0.4.

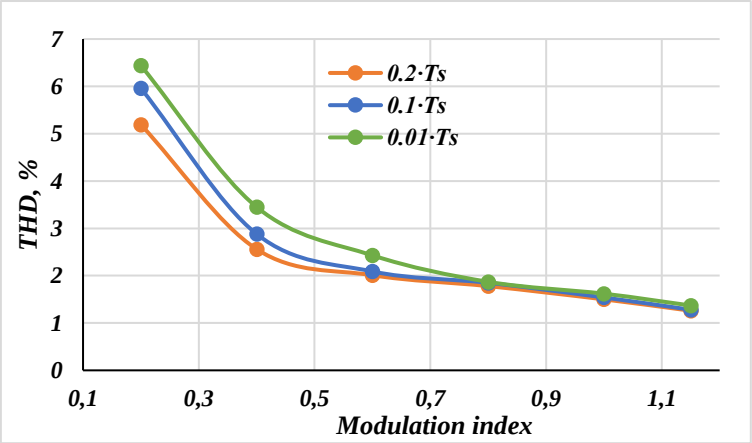
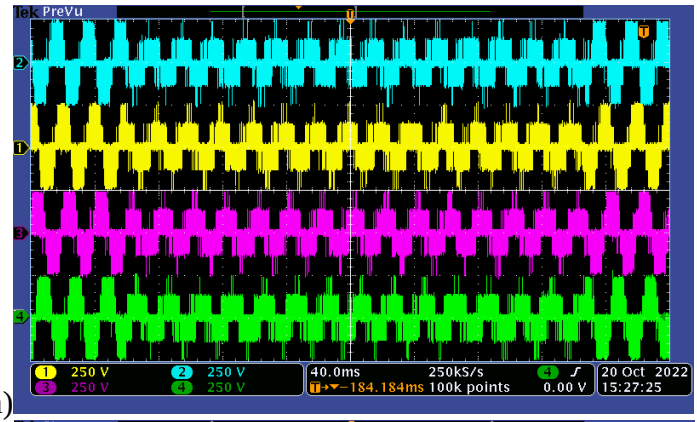


Fig. 6.27. The line voltage THD dependencies on the initial zero-vector duration.

The balancing speed increases as the zero-vector duration decreases; however, the THD value slightly increases for modulation indexes m<0.8. So, the optimal value of the initial zero-vector duration should be chosen depending on the application characteristics. This feature of the modulation technique was obtained during the simulation studies and was previously shown in Fig. 6.6.; this proves the validity of the simulation model.

The proposed SVPWM technique was implemented on five-phase three-level NPC inverter. Figure 6.28. – 6.38. shows the experimental results obtained on a five-phase inverter prototype. The line voltages are shown in Fig. 6.28. (a) and (b), the THD value of the line voltage is given in Fig. 6.28. (b), additionally to the line voltage waveforms. Figure 6.28. (a) shows the system dynamic response on the step change in modulation index of fundamental harmonic voltage, from 1 to 0.5, and back to 1, the additional (fourth) harmonic voltage was set to 0.

(a)



(b)

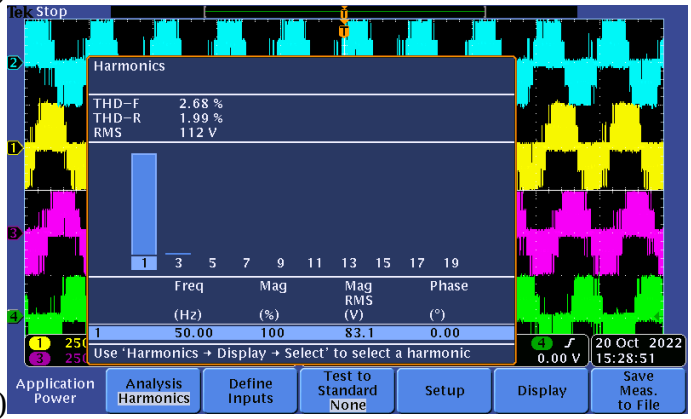
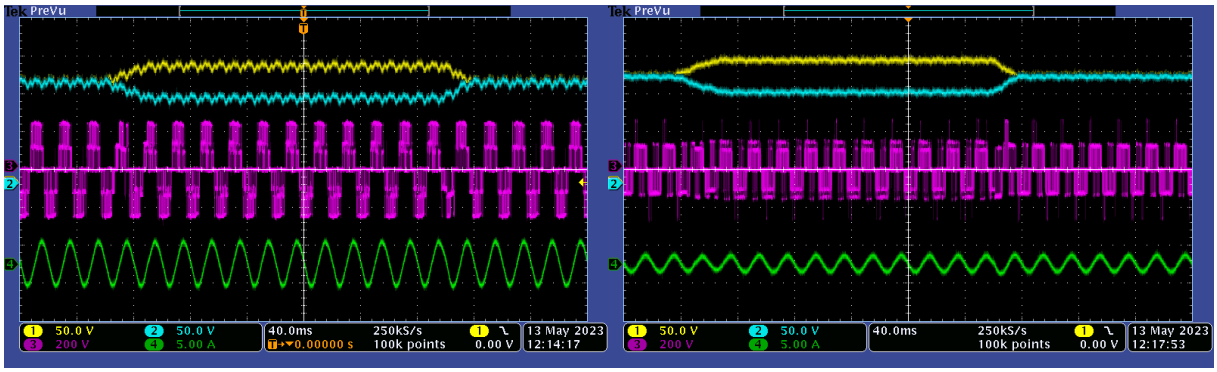


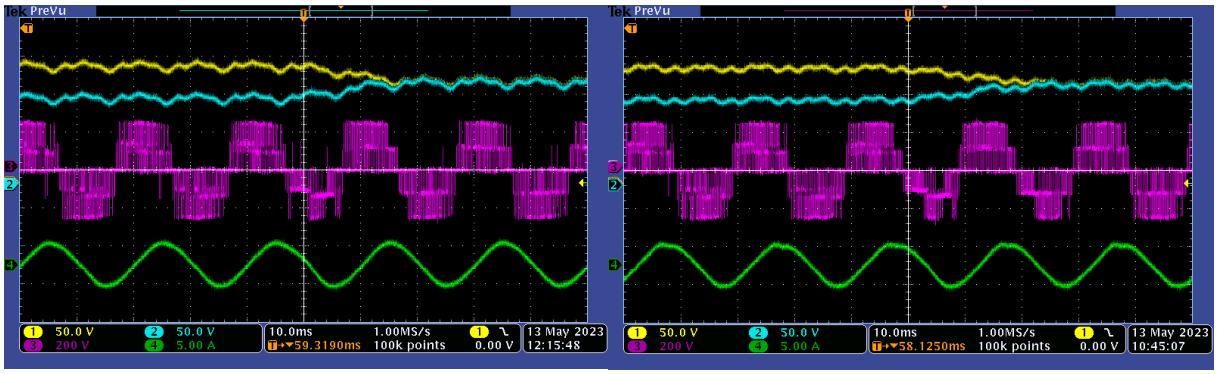
Fig. 6.28. Five-phase inverter: (a) the line voltages v_{ab} (1), v_{bc} (2), v_{cd} (3), v_{de} (4) waveforms under the change on modulation index of the fundamental harmonic voltage, from 1 to 0.5, and back to 1; (b) the FFT – analysis of the line voltage and obtained THD value, modulation index is 1.

Next, the effectiveness of the DC-link capacitor voltages balancing algorithm was verified. Firstly, only fundamental harmonic voltage was generated, in Fig. 6.29. – Fig. 6.30, and corresponding line voltage FFT-analysis with calculated THD values were given in Fig. 6.31. and Fig. 6.33. Line voltage, output current and DC-link capacitor voltages are shown in all the figures. The modulation index was chosen from 1.05 to 0.2. During the first stage of the experimental studies, the initial zero-vector duration was set to $0.01 \cdot Ts$. Next, Fig. 6.30 shows the zoomed view of the DC-link capacitor voltages under the balancing algorithm test, when the initial zero-vector duration are $0.01 \cdot Ts$ and $0.1 \cdot Ts$.

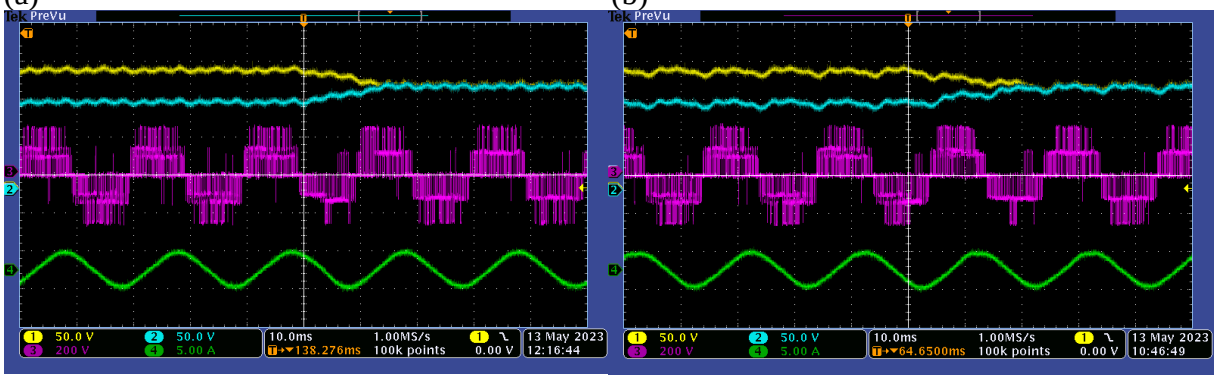


(a) (b)

Fig. 6.29. The line voltage v_{ab} (3), output current i_a (4) and DC-link capacitor voltages v_{dC1} (1), v_{dC2} (2) waveforms of the five-phase NPC inverter for the forced unbalance in the DC-link voltages, when the modulation index is equal to: (a) 1.05; (b) 0.4.



(a) (b)



(c) (d)

Fig. 6.30. The line voltage v_{ab} (3), output current i_a (4) and DC-link capacitor voltages v_{dC1} (1), v_{dC2} (2) waveforms during the balancing process in five-phase inverter, when the modulation index is equal to: (a, b) 1; (c, d) 0.8. The initial duration of the zero vector is: (a, c) 0.01·*Ts*; (b, d) 0.1·*Ts*.

The FFT analysis, with calculated THD value from Fig. 6.31 was obtained when the initial zero vector duration is equal 0.01·*Ts*. The obtained data for different modulation indices are shown in Fig. 6.32. Figure. 6.33. shows the FFT analytical results when the initial zero-vector duration is equal 0.1·*Ts*. The THD values, for a range of the modulation index (1.05 to 0.2), are shown in Fig. 6.34.

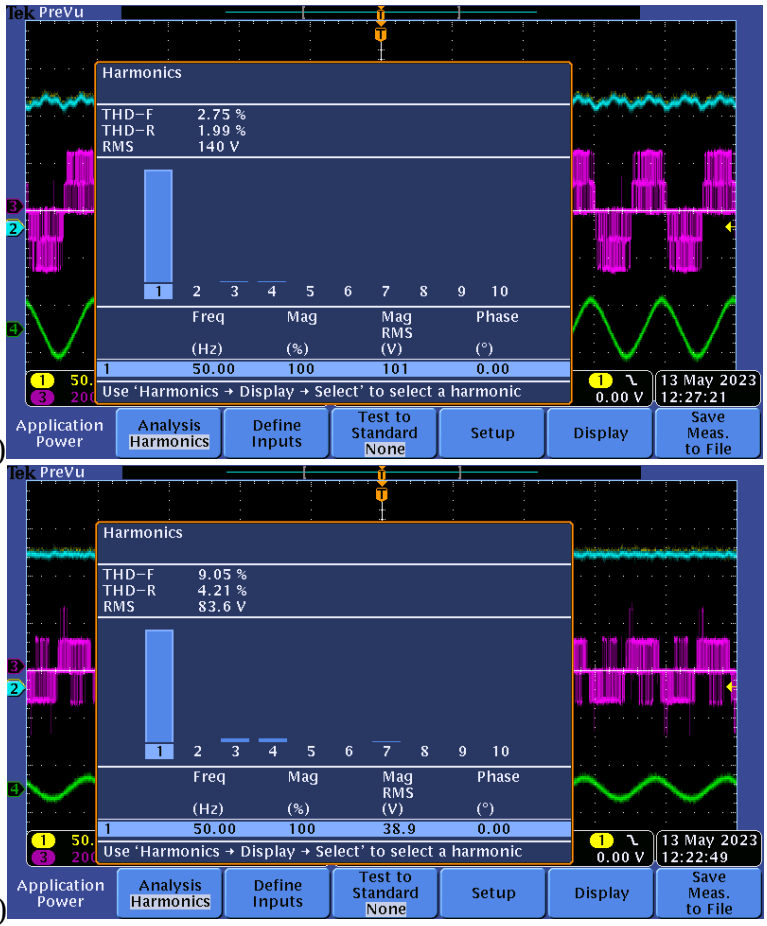


Fig. 6.31. The FFT analysis of the line voltage and obtained THD value in five-phase inverter, when the modulation index is equal to: (a) 1.05; (b) 0.4.

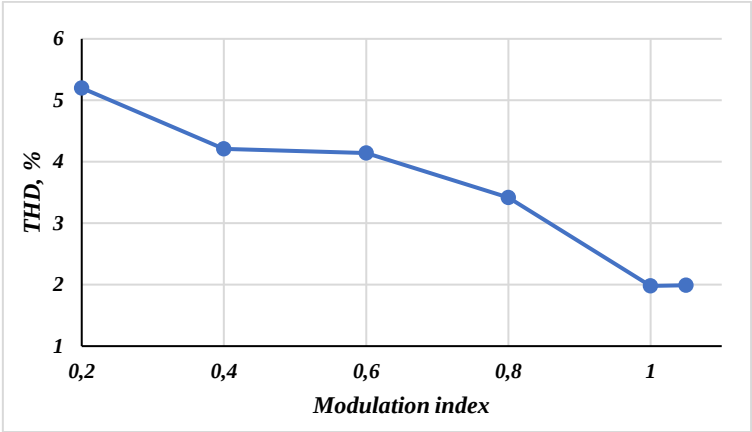


Fig. 6.32. The line voltage THD dependencies on the modulation index for five-phase NPC inverter.

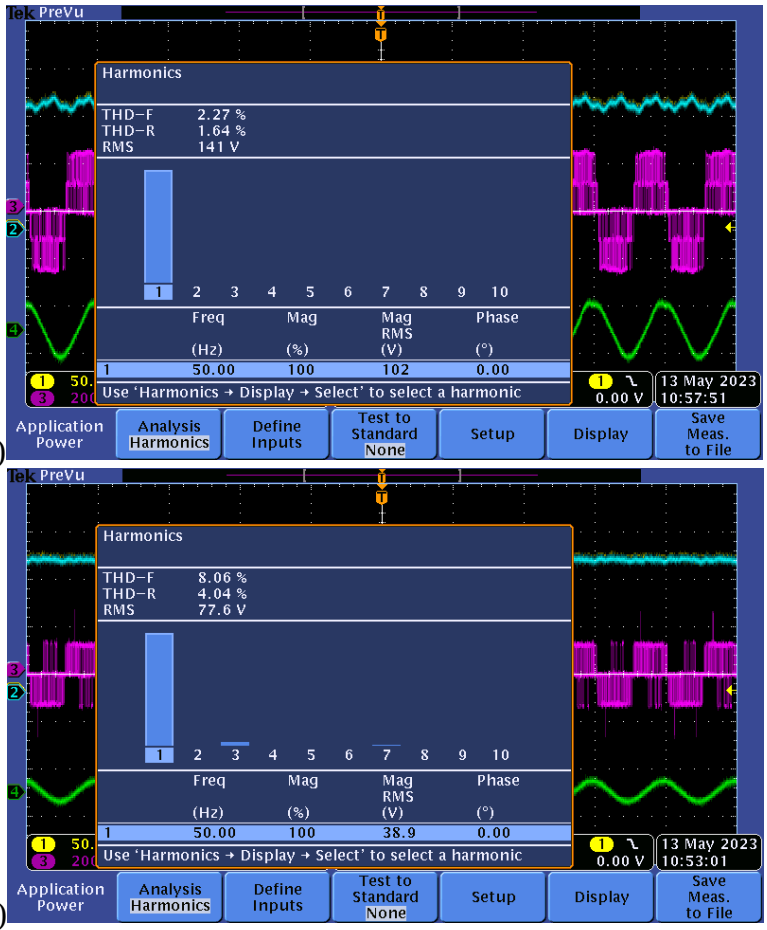


Fig. 6.33. The FFT analysis of the line voltage and obtained THD value in five-phase inverter, when the modulation index is equal to: (a) 1.05; (b) 0.4.

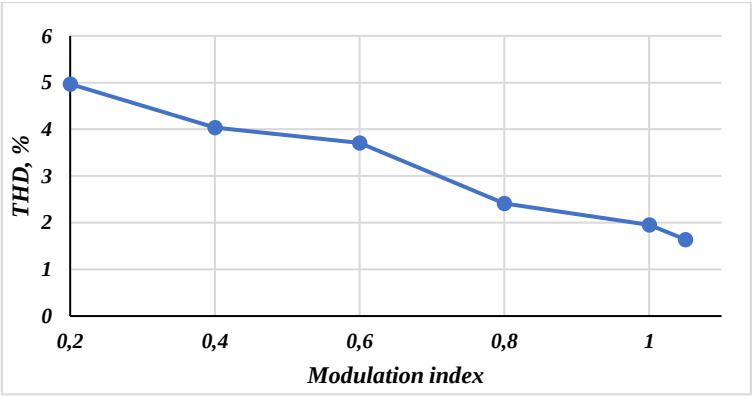
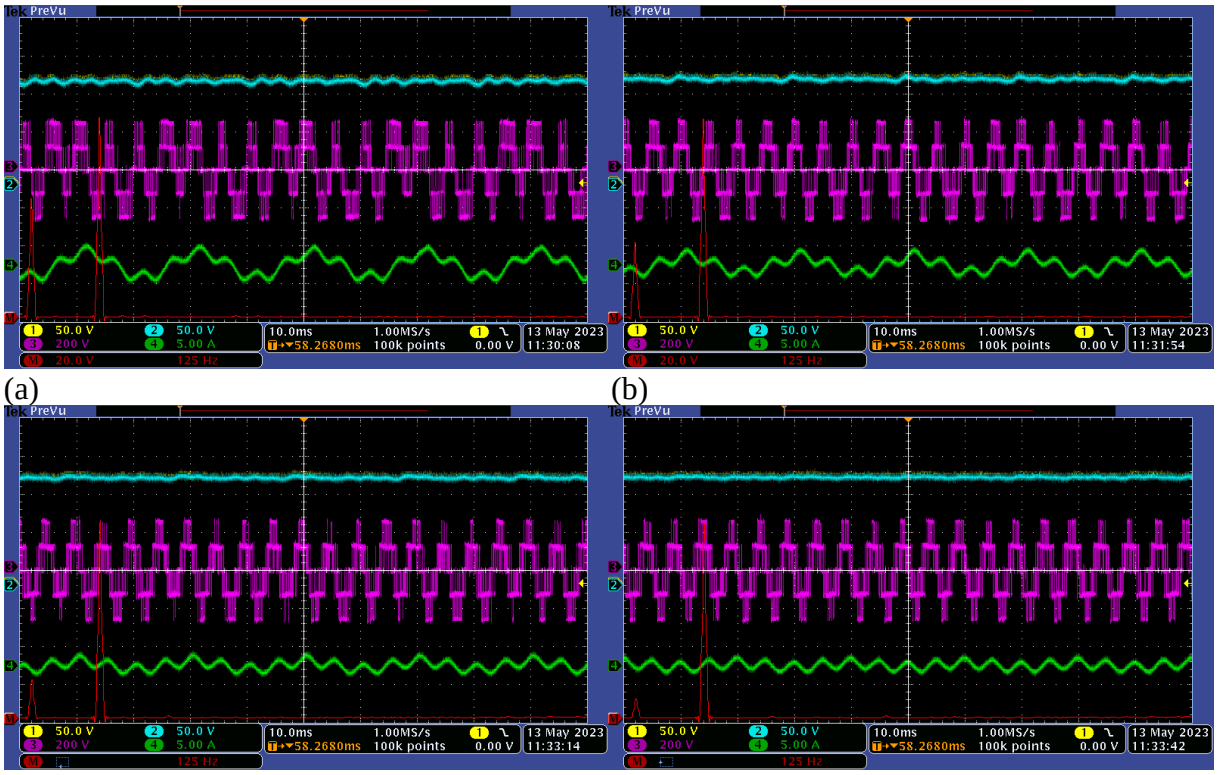


Fig. 6.34. The line voltage THD dependencies on the modulation index for five-phase NPC inverter

The second stage of the experimental studies is to investigate the possibility of independent harmonic generations; and to verify the performance of the balancing algorithm when two independent harmonics are generated. During the experimental studies first (fundamental) and fourth harmonic output voltages are generated. Figure 6.35. shows the FFT analysis of the line voltage when the modulation index of the fourth harmonic voltage is 0.6485; and modulation index of fundamental harmonic voltage is in range: 0.6485 – 0.1.



(a) (b)

(c) (d)

Fig. 6.35. Line voltage FFT – analysis in five-phase inverter, when the modulation index of the 4th harmonic voltage is 0.6485 and of the 1st harmonic voltage: (a) 0.6485; (b) 0.4; (c) 0.2; (d) 0.1. The line voltage v_{ab} (3), output current i_a (4) and DC-link capacitor voltages v_{dC1} (1), v_{dC2} (2) waveforms.

The performance of the balancing algorithm, when two harmonics were generated, is shown in Fig. 6.36. Figure 6.36. (a) and (c) were obtain when the initial zero-vector duration was set to 0.01·*Ts*; while in Fig. 6.36. (b) and (d) the initial duration was 0.1·*Ts*. The zoomed view of the DC-link voltages, output line voltage and current are shown in Fig. 6.36.

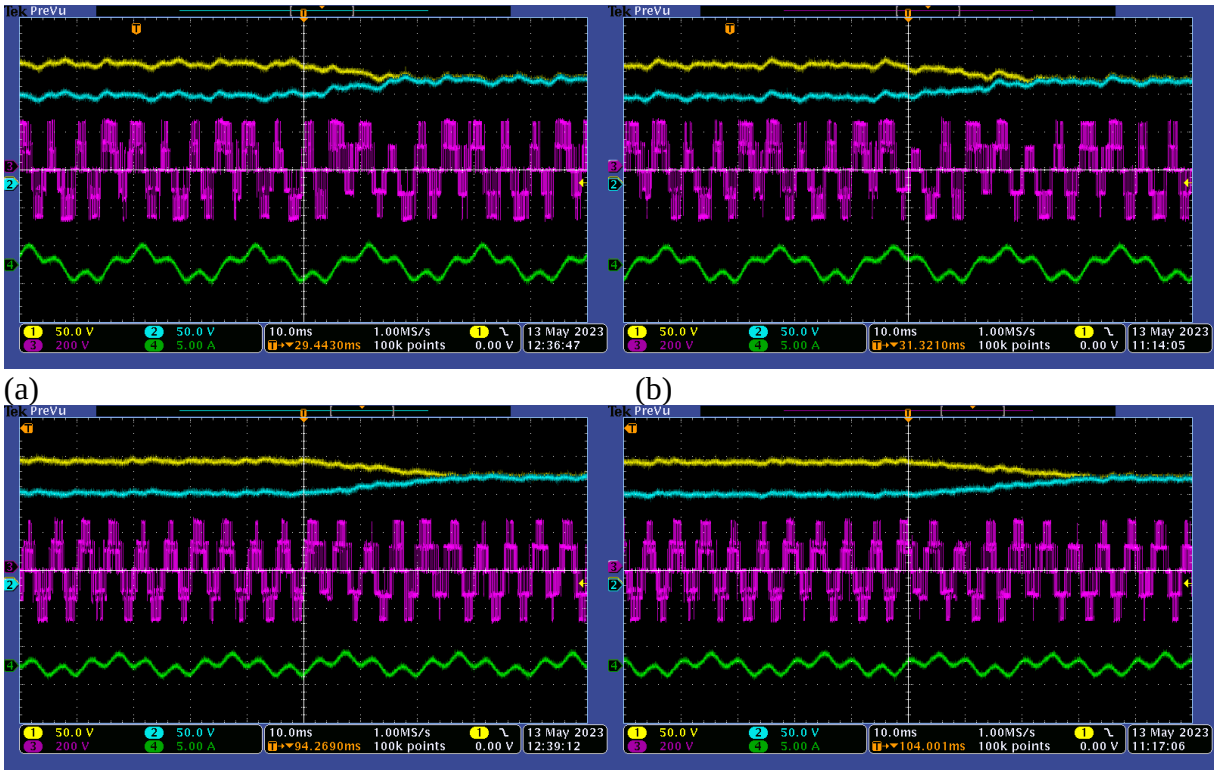
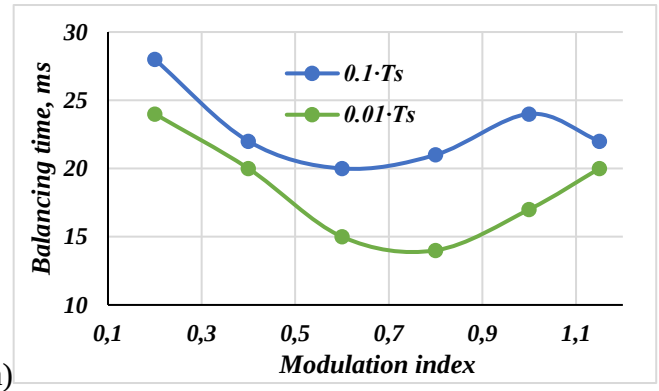
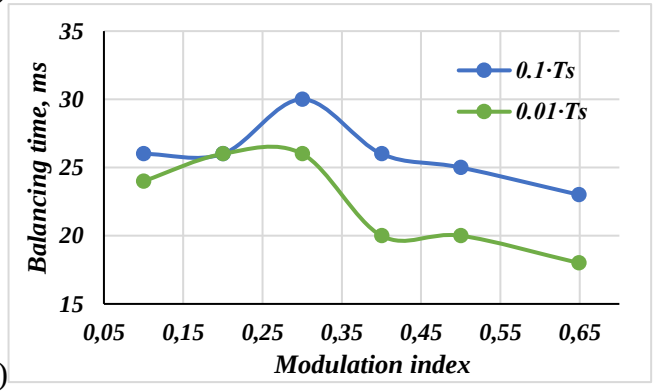


Fig. 6.36. The line voltage v_{ab} (3), output current i_a (4) and DC-link capacitor voltages v_{dC1} (1), v_{dC2} (2) waveforms during the balancing process, when the modulation index of the 4th harmonic voltage is 0.6485 and of the 1st harmonic voltage is: (a, b) 0.6485; (c, d) 0.3. The initial zero-vector duration are: (a, c) 0.01·*Ts*; (b, d) 0.1·*Ts*.

The obtained results are summarized in Fig. 6.37. and Fig. 6.38. Figure 6.37. shows the balancing time versus the modulation index of fundamental harmonic voltage for different initial zero-vector durations. The line voltage THD dependencies are given in Fig. 6.38 for same values of the zero-vector durations, (0.01·*Ts*, 0.1·*Ts*), when the fundamental harmonic was generated.



(a)



(b)

Fig. 6.37. The balancing time dependencies on the modulation index of fundamental harmonic voltage for various initial zero vector durations, (a) fundamental harmonic generation; (b) fundamental and fourth harmonics generation.

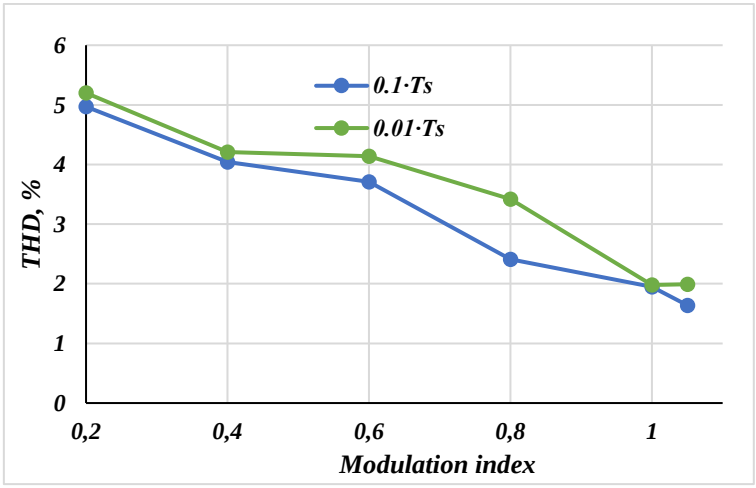


Fig. 6.38. The line voltage THD value versus the modulation index of the fundamental harmonic voltage for various initial zero vector durations, fundamental harmonic generation.

The obtained experimental results prove the effectiveness of the proposed modulation technique. As expected, low initial zero-vector duration allows for better balancing performance; however, the THD value become slightly higher. The FFT analysis of the line voltage, obtained during the experimental studies, shows that the results are the same as obtained under simulation investigation. Thus, effectiveness in independent voltage generation was proven. The comparison studies are carried out, and their results are given in section 6.4. to show the advantage of the proposed approach.

6.4. Comparison of the proposed and conventional modulation strategies

Carrier-based PWMs are the natural competitors to the space-vector methods. Here, the CBPWM technique, proposed in [72], was chosen for comparison studies. This CBPWM technique bases on zero voltage injection, depending on the utilized different switching mode (single-step, multi-step or two-level). The performances of both modulation techniques were investigated. Two main parameters were taking into account: the balancing algorithm performance, and line voltage THD. Additionally, the algorithm execution time on the experimental setup was compared for both methods. The experimental comparisons are given in subsection 6.4.1.

6.4.1. Experimental comparison of analyzed strategies

The CBPWM technique was deployed in the control of the laboratory setup. The same set of tests used in SVPWM control were rerun. Figure 6.39. shows the dynamic response for modulation index change (from 1 to 0.5, and back to 1). Line voltage, output current and DC-link capacitor voltages are shown.

(a)

(b)

Fig. 6.39. The line voltage v_{ab} (3), output current i_a (4) and DC-link capacitor voltages v_{dC1} (1), v_{dC2} (2) waveforms of the three-phase inverter under: (a) CBPWM control and (b) SVPWM control for step changes in the modulation index, from 1 to 0.5 and back to 1 again.

The system behavior under the modulation index change is similar, as shown in Fig. 6.39. However, the proposed algorithm has additional commutations in the third level of the waveform generation. It can be explained by more precise DC-link voltage balancing, and will be investigated below (Fig. 6.43.).

Next, the performance of balancing algorithm was investigated. Figure 6.40. shows the dynamic system response, when an imbalance in DC-link was forced. The zoomed view of the DC-link capacitor voltages balancing process is given in Fig. 6.41. Line voltage, output current waveforms and DC-link capacitor voltages are shown in Fig. 6.40. and Fig. 6.41. The applied imbalanced is 40*V*. The summarized results of the balancing algorithm investigation are given in Fig. 6.42. Therein, where the balancing time dependency on the modulation index for CBPWM and SVPWM techniques are shown.

(a)

(b)

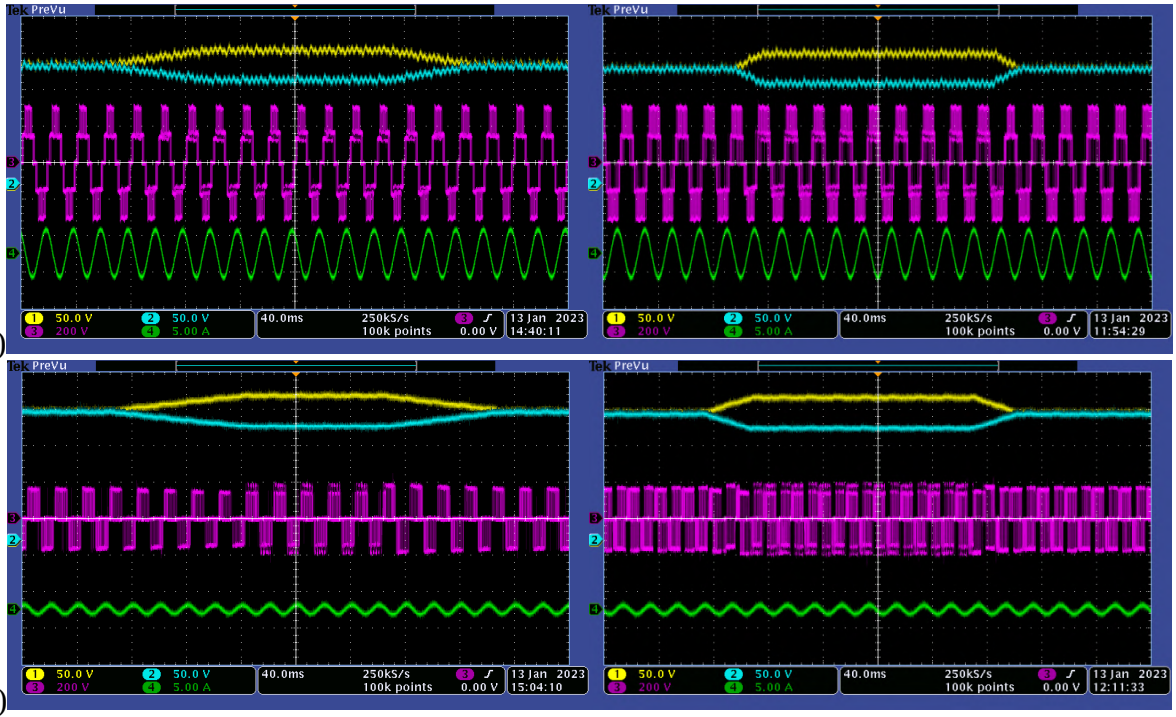


Fig. 6.40. Dynamic response of the three-phase NPC inverter under CBPWM control (on the left) and SVPWM control (on the right) for the forced unbalance in the DC-link voltages, when the modulation index: (a) 1; (b) 0.2. The line voltage v_{ab} (3), output current i_a (4) and DC-link capacitor voltages v_{dC1} (1), v_{dC2} (2) waveforms.

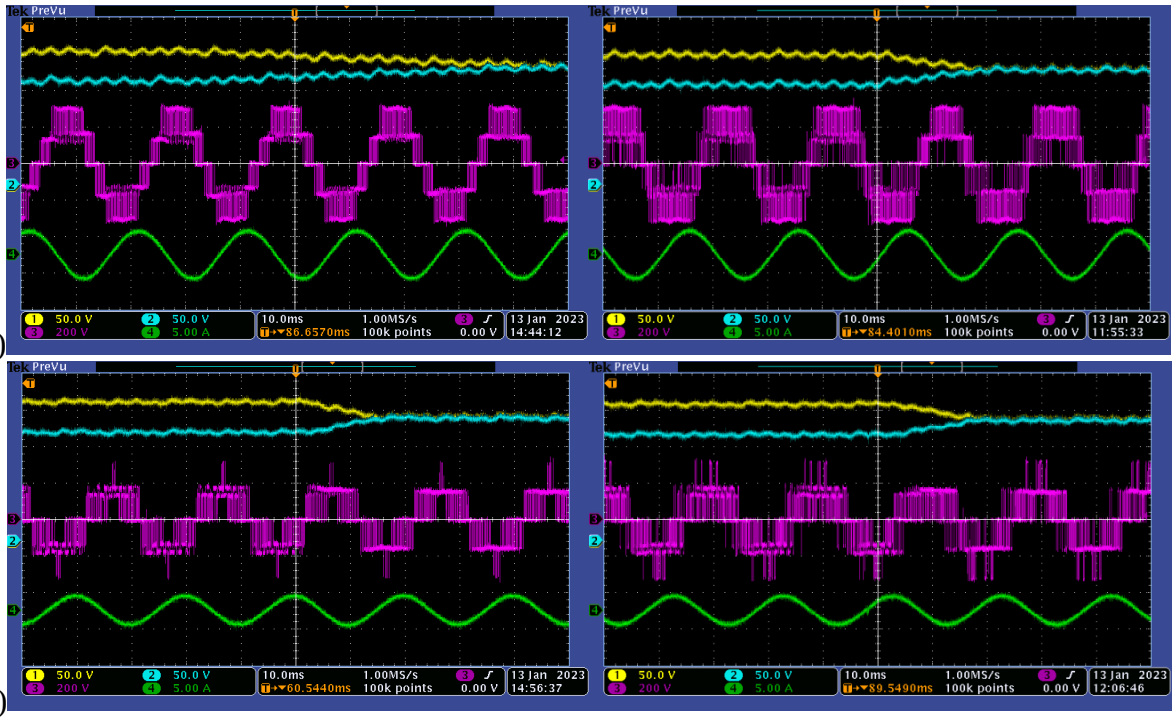


Fig. 6.41. DC-link capacitor voltages balancing in three-phase inverter under CBPWM control (on the left) and SVPWM control (on the right), when the modulation index is equal to: (a) 1; (b) 0.6. The line voltage v_{ab} (3), output current i_a (4) and DC-link capacitor voltages v_{dC1} (1), v_{dC2} (2) waveforms.

Figure 6.42. summarized the balancing algorithm performances. Balancing times for both methods are comparable for modulation index range 0.4 – 0.8. However, for other modulation indices, the difference is significant, e.g. three times higher for CBPWM, when modulation index is equal to 1.

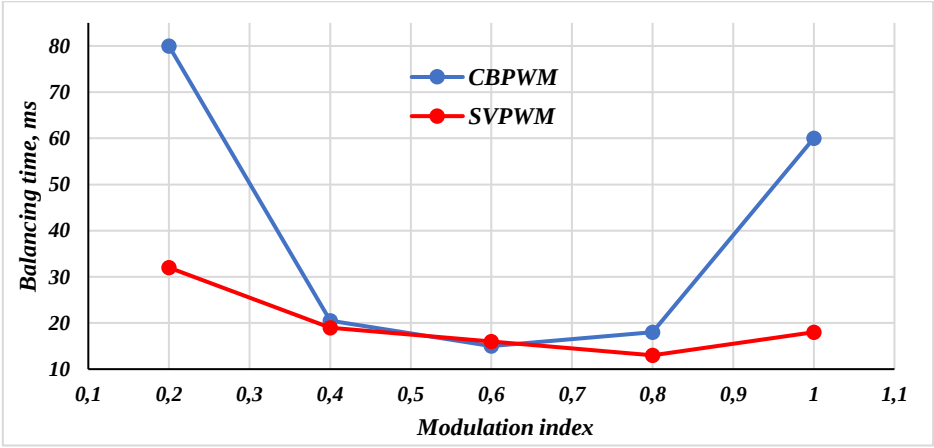


Fig. 6.42. The balancing time versus the modulation index for CBPWM and SVPWM.

The balancing algorithm behavior under the deep asymmetry in DC-link voltages was investigated, for the proposed and reference algorithms. Both capacitors in the DC-link were initially balanced and their voltages were equal to 175*V*. Then the imbalance was forced (the applied unbalanced is equal to 150*V*), and the DC-link voltages were balanced once again.

Figure 6.43. (a, b) shows the line voltage, output current and DC-link capacitor voltages; while Fig. 6.43. (c, d) shows the AC components of balanced DC-link voltages from Fig. 6.43. (a, b).

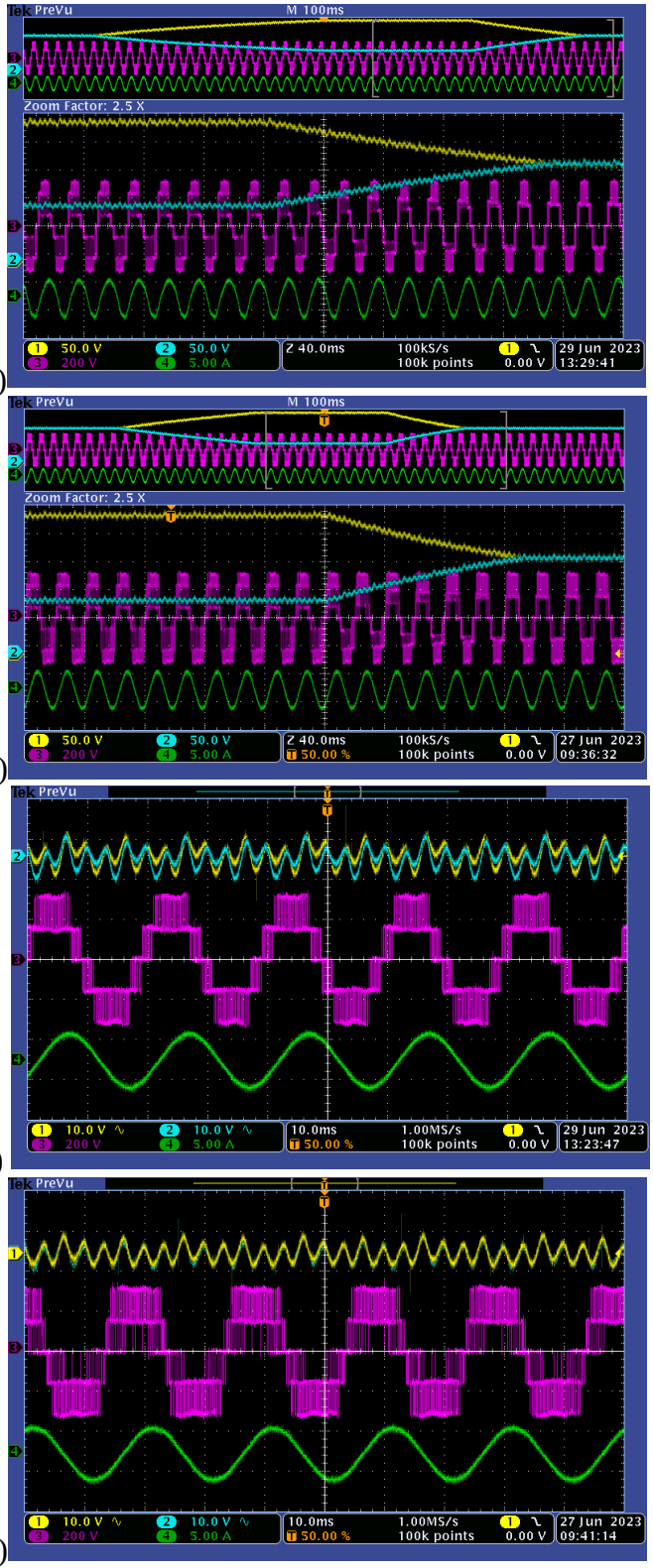


Fig. 6.43. The line voltage v_{ab} (3), output current i_a (4) and DC-link capacitor voltages v_{dC1} (1), v_{dC2} (2) waveforms in three-phase inverter under CBPWM control (a, c) and SVPWM control (b, d), when the modulation index is equal to 1. (a,b) The deep asymmetry in the DC-link; (c, d) the waveforms of AC components of both DC-link voltages.

As could be seen in Fig. 6.39. and Fig. 6.43., the proposed modulation algorithm has the additional levels in the line voltage waveform. These levels are the effect of precise balancing of DC-link voltages, as shown in Fig. 6.43 (d), where the DC-link voltages overlap each other. Even small difference in the DC-link voltages results in direct duration change of the potential 'O'. When the DC-link voltages are close to be balanced, small charge is required to be delivered to the capacitors. As a result, only small duration changes of 'O' potential in the phases with the appropriate current directions are required. Thus, the switching patters contains all the states 'N', 'O', and 'P'.

The quality of the generated output line voltages was verified using FFT analysis for various modulation index, from 1 to 0.2. Figure 6.44. shows the results of FFT analysis of the line voltage, with THD calculation up to 50 harmonics (up to 2500Hz). The current harmonics above this frequency range can be easily filtered by the load. Line voltage, output current waveform and DC-link voltages were shown in Fig. 6.44. The summarized results are shown in Fig. 6.45. Figure 6.45. (a) shows the THD results up to 50th harmonics and Fig. 6.45. (b) shows the THD comparisons up to 100th harmonics.

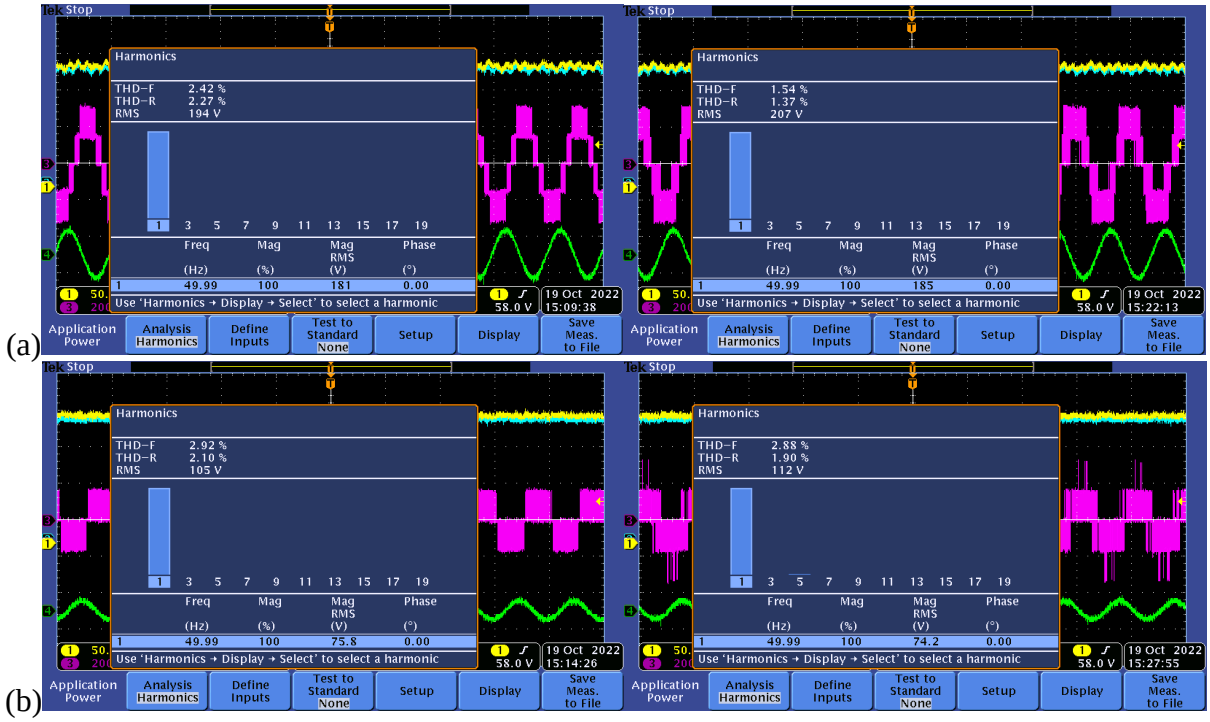
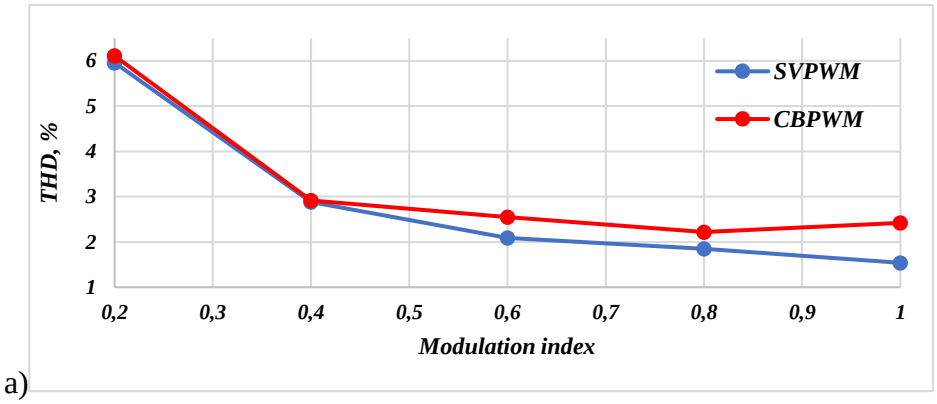
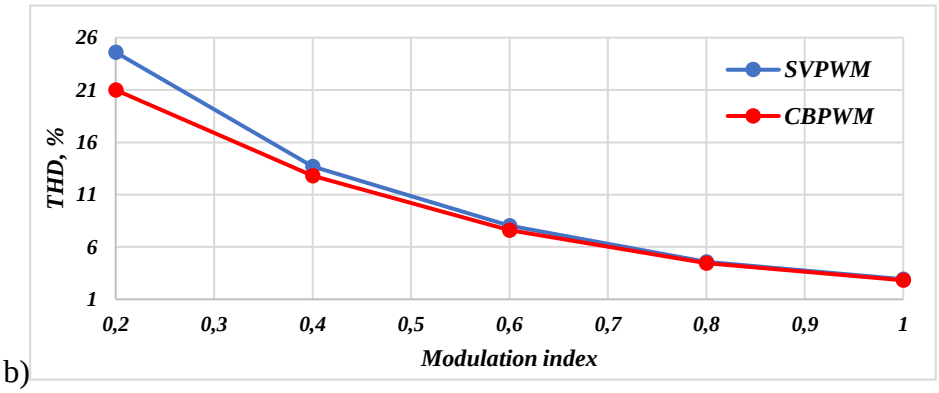


Fig. 6.44. The FFT – analysis of the line voltage and obtained THD value in three-phase inverter under CBPWM control (on the left) and SVPWM control (on the right), when the modulation index is equal to: (a) 1; (b) 0.4.



a)



b)

Fig. 6.45. The THD value versus the modulation index for CBPWM and SVPWM, (a) up to 50th harmonic; (b) up to 100th harmonic.

The harmonic spectra obtained during the FFT analysis of the line voltage for both methods were shown in Fig. 6.46. Proposed modulation technique has higher harmonic's peak near switching frequency, but lower peak at the rest of the spectrum. To summarize, the difference in THD values is small, so the obtained results are comparable and similar for all modulation indexes.

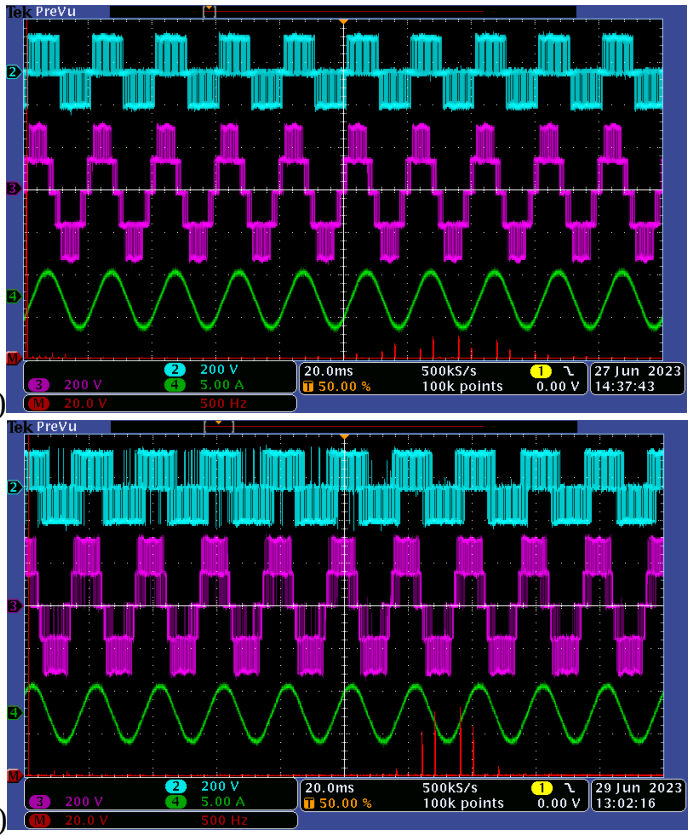


Fig. 6.46. Line voltage FFT – analysis in the three-phase inverter, when the modulation index is equal to 1, under: (a) CBPWM control; (b) SVPWM control. The line voltage v_{ab} (3), output current i_a (4) and DC-link voltage v_{DC} (2) waveforms.

The simulation and experimental results were presented in this Chapter. The FFT-analysis of the line voltage was provided for three- and five-phase configurations of the NPC inverter. Simultaneously, the comparison studies show the superiority of the proposed SVPWM technique. This superiority is confirmed by the performance of the DC-link voltages balancing algorithm. The quality of the generated output waveforms is similar to the existing solutions. FFT-analysis of the line voltage for the first 50 harmonics proves that for the proposed SVPWM technique, it is possible to obtain lower THD values, compared to the CBPWM. For instance, for m=0.8, the THD is 1.85% and 2.22% for proposed and carrier-based modulation, respectively. When the switching frequency was included to the FFT analysis, the obtained results become similar for both techniques (for m=0.8, the THD is 4.58 % and 4.46% for SVPWM and CBPWM). It proves that the waveforms' qualities are at par in both techniques. Nevertheless, the computational complexity of the proposed algorithm is significantly lower than in conventional SVPWM techniques; and is similar as of CBPWM techniques. The measured execution times of the modulation algorithms are comparable and equal to 1.65*ms* and 1.79*ms* for the proposed SVPWM, and conventional CBPWM technique, respectively.

7. Summary

This thesis presented the PWM techniques that can be utilized in three- and multi- phase drive systems with three-level VSIs. Such PWM techniques can generate two independent output voltage vectors, preserving the output waveforms with proper shape and harmonic contents and control the DC-link voltages.

The thesis focused on three-phase, as well as five-phase, three-level inverter structures. Additionally, the proposed modulation algorithm is presented in a general form so that it can be applied to inverter of any number of phases. The research primarily concentrates on space vector approach. However, in order to improve the algorithm, the dependencies applicable to individual phases of the inverter (usually used in SPWM approaches) were used. The obtained method was compared with carrier-based algorithm. It should be noted, that the carrier-based algorithms are commonly considered being universal and easily extendable to the require number of phases. The comparison between these two techniques was based on two characteristics: balancing speed (which represents the balancing algorithm performance), and THD value to compare the distortions under different operating conditions. The balancing quality was also compared. The obtained results proved that the proposed modulation algorithm ensure precise DC-link capacitor voltage balancing for wide range of the modulation indices; in dynamic- and steady-states. The superiority of the proposed technique is visible for high and low modulation indices, compared to the sinusoidal PWM. In the computation complexity of the proposed algorithm is similar to the sinusoidal technique and much simpler than conventional SVPWM for three-level inverters; especially for multiphase inverters.

The functionality of the developed modulation strategy has been tested in F-type and NPC inverter topologies through simulation and experimental tests on three and five phase three level NPC inverters. The obtained results proves that it is possible to generate several output voltage vectors independently, as well as ensure balancing the DC-link voltages. This was declared in the hypothesis of this PhD dissertation.

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9. List of papers published during the PhD education cycle

1. A. Lewicki, **D. Kondratenko** and C. I. Odeh, "Hybridized PWM Strategy for Three- and Multiphase Three-Level NPC Inverters," *IEEE Trans. on Industrial Electron.*, (early access), doi: 10.1109/TIE.2023.3321999.

2. A. Lewicki, C. I. Odeh, **D. Kondratenko**, and M. Morawiec, "Hybridized Space-Vector Pulsewidth Modulation for Multiphase Two-Level Voltage Source Inverter," *IEEE Trans. Power Electron.*, vol. 37, no. 7, pp. 7663–7674, Jul. 2022, doi: 10.1109/TPEL.2022.3145161.

3. C. Odeh, A. Lewicki, M. Morawiec, and **D. Kondratenko**, "Three-Level F-Type Inverter," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11265–11275, Oct. 2021, doi: 10.1109/TPEL.2021.3071359.

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6. C. Odeh, **D. Kondratenko**, A. Lewicki, M. Morawiec, A. Jąderko, and J. Baran, "Pulse-Width Modulation Template for Five-Level Switch-Clamped H-Bridge-Based Cascaded Multilevel Inverter," *Energies*, vol. 14, no. 22, p. 7726, Feb. 2021, doi: 10.3390/en14041198.

7. C. Odeh, **D. Kondratenko**, A. Lewicki, and A. Jąderko, "Modified SPWM Technique with Zero-Sequence Voltage Injection for a Five-Phase, Three-Level NPC Inverter," *Energies*, vol. 14, no. 4, p. 1198, Feb. 2021, doi: 10.3390/en14041198.

8. **D. Kondratenko**, A. Lewicki, "A Simplified SVPWM Technique for Five-leg Inverter with Dual Three-phase Output," 2023 3rd International Conference on Electrical, Computer, Communications and Mechatronics Engineering (ICECCME), Tenerife, Spain, 2023, pp. 1-6, doi: 10.1109/ICECCME57830.2023.10252832.

9. **D. Kondratenko**, A. Lewicki and C. Odeh, "Increasing the Utilization of dc-link Voltage of a Five-Leg VSI Based on Rotor Angle Control of Dual Induction Motors," 2023 IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 2023, pp. 2825-2830, doi: 10.1109/APEC43580.2023.10131536.

10. **D. Kondratenko**, A. Lewicki and C. Odeh, "Single-phase, Five-level Inverter with SPWM-Based Neutral Point Voltage Balancing Scheme," 2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), Hanover, Germany, 2022, pp. 1-8, doi: 10.34808/5gk4-jj85.