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BUILT-IN TEST SCHEME FOR DETECTION, CLASSIFICATION AND EVALUATION OF NONLINEARITIES

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Abstract

This paper presents a Built-In Test (BIT) scheme intended for detection of nonlinearities, classification of the form of nonlinearity and evaluation of the total harmonic distortion (THD) of the signal under test, without using expensive automatic test equipment (ATE). The tester is based on a sigma-delta modulator located on a board and artificial neural networks implemented in an attached personal computer. The proposition is verified by simulation in a Matlab/Simulink environment for three classes of nonlinearities – clipping effect, crossover distortion and rate limiting. The model of the Van der Pol oscillator is used as a programmable reference source of nonlinear oscillation.

Keywords: built-in test, oscillation-based test, evaluation of nonlinearities, sigma-delta modulator, neural networks.

1. Introduction

The increasing complexity of mixed signal electronic systems and the reduced access to internal nodes has made it very difficult to test analog parts of these systems. A way to decrease test cost is to move some or all of the test instrumentation functions into the chip itself or onto the board. This concept, which is known as Built-In Test, has received considerable attention [1].

In this context, a new test technique, called the Oscillation-Based Test (OBT), has been introduced recently [2]. Basically, when this technique is used, the Circuit Under Test (CUT) is converted into a system that oscillates. A nonlinear feedback loop is added to the CUT and activated in the test mode to produce robust oscillations. Oscillation frequency and other parameters are closely related to the behaviour of the circuit and can be used to detect faults.

Many published works are related to one of the crucial issues concerning how to extract diagnostic information from the signal under test. The idea of using the Sigma-Delta (SD) modulator as the means of extracting and compressing of analog

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responses has been explored by a few authors [3-9]. The important advantage of a SD modulator is its relatively high tolerance to manufacturing process variation. Because of this advantage of the SD technique it is frequently embedded within most mixed-signal ICs.

The aim of this work is to extend the above approach and develop a low-cost, simple mechanism for detection, classification and evaluation of nonlinearities in the test signal by using the SD technique on board and artificial neural networks (ANN) in an attached computer system.

The paper is structured as follows; Section 2 describes the proposed approach; in Section 3 the theoretical foundations are presented; Section 4 presents the simulation results to demonstrate feasibility of the fusion of the two techniques – SD and ANN.

2. The proposed approach

For analysis of the signal under test a scheme is proposed which works in the time domain (Fig. 1). A sigma-delta modulator is employed to digitize the tested signal into a high-speed, 1-bit stream. The reference bit stream is subtracted from the tested one to leave only the distortion and noise. The bit stream, used as a reference, is a high purity signal synthesized by software. A method to generate the reference signal consists of recording the bit stream from the output of a simulated SD modulator and reproducing them with some memory on the board [10]. An up/down digital counter performs averaging of the difference over a fixed period of time to obtain a finite set of values called “the fault signature”.

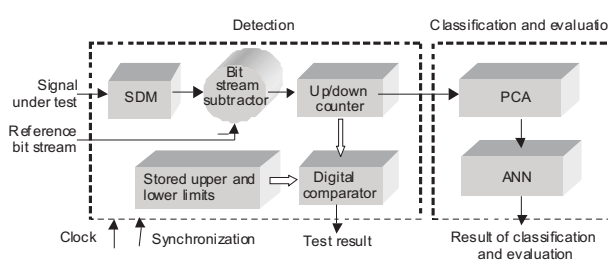

Fig. 1. BIT architecture based on Sigma-Delta modulator (SDM).

In the case of a fault-free circuit, which generates a distortion-free signal with proper frequency and amplitude, the average value of the counter output sequence is near zero. In the case where the tested waveform is different from the reference pattern, the average value differs from zero. The digital comparator compares the signature produced by the counter over the duration of one period with the upper and lower limits stored in a ROM. If the result of comparison is positive, then the circuit is passed, otherwise it is failed. In the case of failure, the output bit stream can be

processed externally by an ANN, implemented in the computer system for classification and evaluation of the nonlinear phenomenon.

3. Theoretical foundations

A sigma-delta modulator is the basic building block in the testing circuit. The ideal SD modulator should have a wide input bandwidth, high resolution and high input level without overloading.

We will assume the presence of a limited number of significant harmonics in the tested signal. Usually, during distortion measurements, the power in the harmonics is considered up to the ninth harmonic [11].

The modulator resolution depends on factors like the oversampling ratio (OSR) and the order of the modulator. Assuming the quantization noise to be a random process with a uniform distribution and a white noise spectrum, the theoretical maximal resolution (the number of bits N) of the modulator with a single-bit quantizer can be calculated as

$$N = \frac{1}{6.02}\left[(20L + 10)\log(OSR) - 20\log\left(\frac{\pi^L}{\sqrt{2L+1}}\right)\right], \tag{1}$$

where L – the order of the modulator, $OSR = \frac{f_s}{2f_B}$ – the oversampling ratio, f_s – the sampling rate, and f_B – the signal bandwidth [12]. The first-order modulator requires rather large OSR for accurate data conversion. For example, the maximal resolution of the first-order modulator with OSR = 64 is N = 8 bits. The equation (1) shows that there are two methods to increase the resolution. The first method is to use a higher order modulator ($L > 1$) and obtain better noise-shaping capability. The second method is to increase the sampling rate. The resolution increases by L+ 0.5 bits for every doubling in the sampling rate, but higher f_s results in higher power consumption and technological difficulties. It is advantageous to reduce the sampling rate in practical applications, so higher-order modulators are more attractive. In addition, higher-order modulators overcome the disadvantages of the first-order modulator, particularly an inclination to limit cycles (idle-tone generation). Unwanted tones limit the Spurious Free Dynamic Range (SFDR) [13].

Our simulations are based on the CIFB (cascade of integrators, feedback) second-order modulator structure. The discrete-time model of the modulator (Fig. 2) consists of two integrators, a quantizer and the coefficient multipliers. The optimum values of the coefficients fulfill the relationships $a_1 = b_1$ and $a_2 = 2a_1c_1$. We have chosen feed-back coefficients $a_1 = a_2 = 0.25$, feed-in coefficient $b_1 = 0.25$, interstage coefficients $c_1 = 0.5$, $c_2 = 5.04$ following the guidelines from [14] and $g = 9.1710^{-6}$, according to the design methodology described in [13].

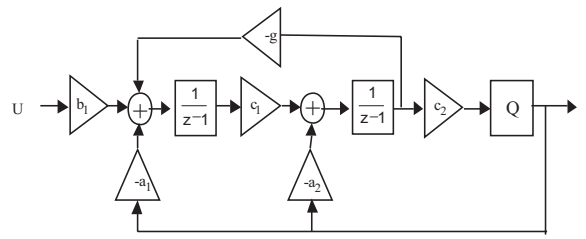

Fig. 2. A discrete-time model of the CIFB second-order modulator.

The I/O relationship of the designed second-order SD modulator can be expressed as

$$V(z) = STF(z)U(z) + NTF(z)E(z), \tag{2}$$

where $STF(z)$ – the signal transfer function, $NTF(z)$ – the noise transfer function, and $E(z)$ – the additive quantization noise.

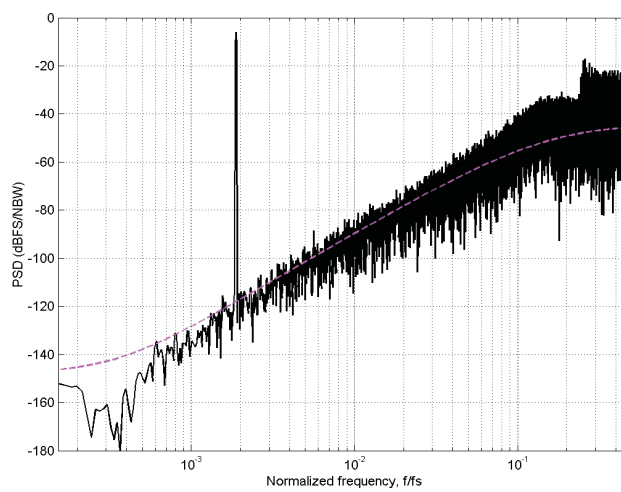

Fig. 3. Output spectrum of the designed second-order modulator with a half-scale input.

Figure 3 shows the output spectrum of the designed modulator for OSR = 128. The amplitude of the signal under test is set to half of the modulator's input range to ensure its stable operation. The 40 dB/decade noise shaping is clearly visible. The bandwidth expressed in normalized frequency f/f_s is 3.9 10^{-3}. A simple antialiasing filter to limit the bandwidht of the processed signal must precede the SD modulator. The theoretical resolution calculated from (1) exceeds 15 bits. Since the reference

bit stream is generated using software, a high-order modulator can be used, because an increase in order does not increase the complexity of the generation. Hence, the 5th-order modulator has been implemented.

The applied method of subtraction of two bit streams employs their interleaving into a single stream at doubled clock frequency. In order to perform this, the two bit streams are upsampled by a factor of two like in [15]. The bit streams can be supplied into and extracted out of the board, using the IEEE Standard 1149.1 Test Access Port and Boundary-Scan Architecture.

The signatures are synthesized by averaging of the subtractor output sequence. To remove the phase impact on the signature, the reference signal, as well as the beginning of the averaging, need to be synchronized with the zero crossing point of the signal under test. With a simple digital averager, realized with an up/down counter and a register, the modulation noise in the bit stream will not be entirely filtered out. However it is not a problem for the ANN owing to its generalization capabilities, as the behavioral simulation will reveal in the next section.

4. Simulation results

The proposed scheme has been implemented and validated by simulation using the Matlab/Simulink programming environment. For experimentation we chose three sources of static distortion which results from the basic device nonlinearity, and one source of nonlinear oscillations. The principal characteristic of the last source is that the presence of harmonic terms in its waveform causes deviation of the oscillation frequency.

The Neural Network Toolbox of Matlab was used in order to verify the ability of the proposed scheme to classify and evaluate of nonlinearities with the aid of an ANN.

4.1. Detection

If the signal under test obtained from a distortion-free oscillator and the reference signal are equivalent in frequency, amplitude and phase, the one-period signature contains only the noise (Fig. 4a). If any form of nonlinearity arises in the signal, the shape of the signature is quite different (*e.g.* presented in Fig. 4b). Let us consider the following examples.

The first example (Fig. 5a) shows a common distortion mechanism known as the clipping effect. This mechanism produces a trapezium-like signature (Fig. 5b), whose magnitude depends on the clip level.

The second example shows a significant discontinuity at the zero crossing (crossover distortion), presented in Fig. 5c, that results in the triangular-like signature (Fig. 5d).

The third example (Fig. 5e and 5f) concerns the case when the device under test reaches its maximum output rate of change. It is said to be slew-limited.

In all cases, detection of nonlinearity can be realized with the aid of a digital comparator.

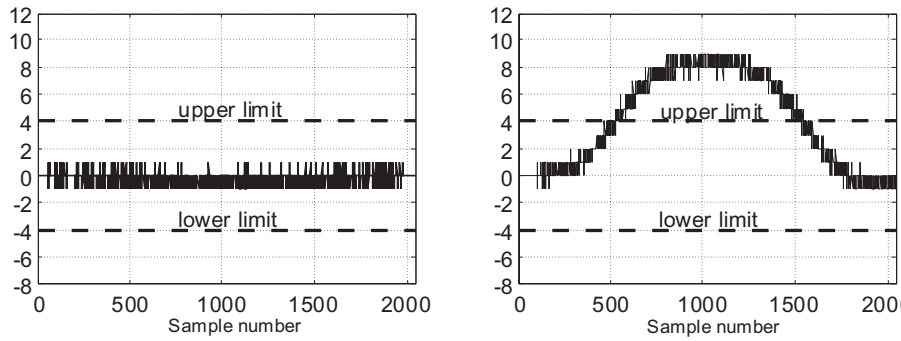

Fig. 4. An example of signatures: a) for fault-free circuit, b) for nonlinear behaviour of the circuit under test.

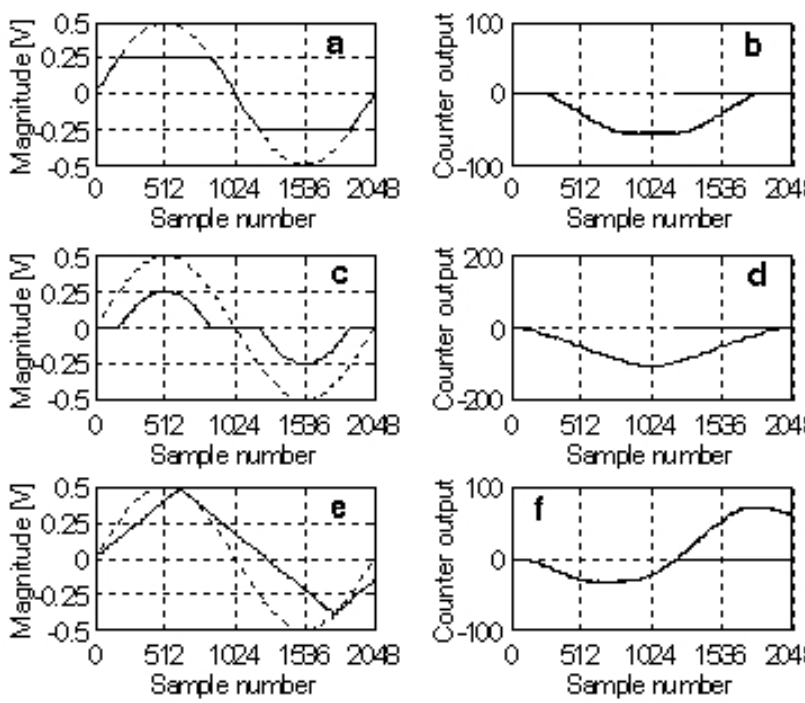

Fig. 5. Static distortions and corresponding one-period signatures: a), b) clipping effect, c), d) crossover distortion, e), f) rate limiting.

4.2. Classification

The next simulation experiments were performed to ensure that the signature synthesizer in connection with ANN is efficient in classification and evaluation of nonlinear phenomena.

A two-layer sigmoid neural network was used to classify (distinguish) different forms of nonlinear distortion: clipping, crossover distortion and rate limiting. There was a need to minimize the signature length by decimation of the counter output in order to simplify the neural network architecture and shorten its training time. Decimation was used to store only 32 integer values in the signature.

Simulation for the deviations of parameters of nonlinear phenomena was performed. In Table 1 the parameters are listed together with their ranges. During simulation of distorted signals 100 values of each parameter were used with randomly chosen amplitude and frequency, which gave 300 signatures in the overall data set. Signatures contained in the data set were divided into three classes. The target output vectors have "1" in the position corresponding to the correct class and "0s" elsewhere.

Table 1. Simulated forms of nonlinear distortion and their parameters.

Form of distortion	Parameter	Range V
Clipping	clip level	0.44 - 0.25
Crossover distortion	dead zone	0.01 - 0.25
Rate-limiting	slew rate	0.25 - 0.45

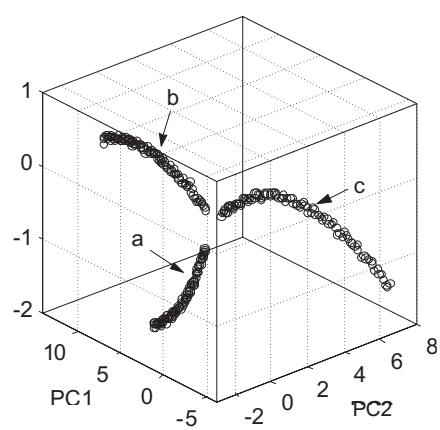

Fig. 6. Clusters of reduced data in the three-dimensional principal component space: a) clipping effect, b) crossover distortion, c) rate limiting.

The Principal Component Analysis (PCA) was applied as an extraction technique of diagnostically relevant features. Its main advantage is effective data compression and in consequence a significant reduction of the neural network's size. In our case a 10-fold reduction of signature dimensionality was obtained. Fig.6 presents the clusters of reduced data in the three-dimensional principal component space. The compressed signatures are grouped in three clusters. All clusters are perfectly separable in the three-dimensional space. Hence, a simple ANN architecture 3-3-3 (3 inputs, 3 neurons in the hidden layer, 3 neurons in the output layer) was applied. The number of inputs coincides with the reduced dimensionality of data. The number of output layer neurons coincides with the number of three classes to be detected. The log-sigmoid transfer function in the output neurons squashes the outputs into the range from 0 to 1 and guarantees lower values of the mean-square training error. An input signature belongs to the class characterized by the largest value of the output neuron. The ANN has been trained with the Levenberg-Marquard algorithm.

The trained neural network manifested very good generalization capabilities. All signatures contained in the testing set were correctly classified.

4.3. Evaluation

The second ANN was used for evaluation of the total harmonic distortion (THD) of a signal generated by the nonlinear oscillator. The Simulink model of the Van der Pol oscillator (Fig. 7) has been used as a programmable source of nonlinear oscillation. It is described by the following equation

$$\ddot{x} + \varepsilon(x^2 - 1)\dot{x} + \omega_0^2 x = 0, \tag{3}$$

where ω_0 is the oscillation frequency without considering the nonlinear effects. Parameter ε gives us the possibility of programming the distortion level without influencing the amplitude of oscillation (Fig. 8).

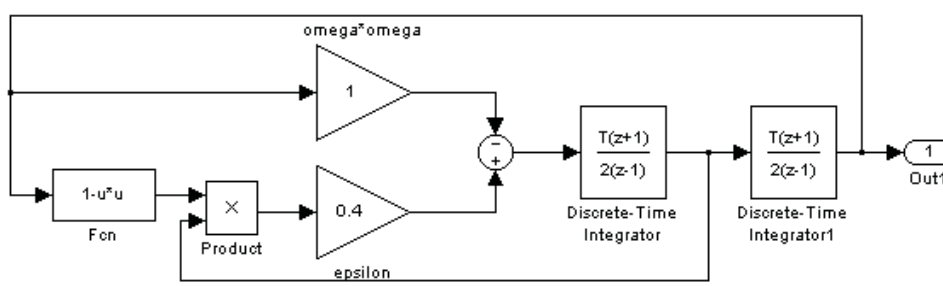

Fig. 7. Simulink model of the Van der Pol oscillator.

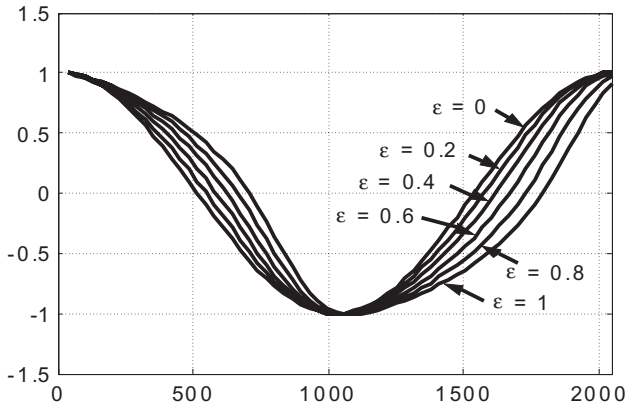

Fig. 8. Nonlinear oscillations obtained from the model of the Van der Pol oscillator.

In terms of the dimensionless time variable $\tau = \omega t$ the above equation becomes

$$\omega^2 x'' + \varepsilon\omega\left(x^2 - 1\right)x' + \omega_0^2 x = 0, \tag{4}$$

where the primes indicate derivative with respect to τ.

We have calculated the response of the oscillator using the Lindstedt-Poincare method [16].

$$x(\tau) = \left(2 - \frac{\varepsilon^2}{8\omega_0^2}\right)\cos\tau + \frac{3\varepsilon}{4\omega_0}\sin\tau - \frac{\varepsilon}{4\omega_0}\sin 3\tau + \\ + \frac{3\varepsilon^2}{16\omega_0^2}\cos 3\tau - \frac{5\varepsilon^2}{96\omega_0^2}\cos 5\tau + ... \tag{5}$$

$$\omega = \omega_0\left(1 - \frac{\varepsilon^2}{16\omega_0^2}\right) + ... \tag{6}$$

From the oscillator response (5) the THD can be calculated as the ratio of the RMS voltage of the harmonics to that of the fundamental component. In Table 2 the THD in dB and angular oscillation frequency ω in rad/s are specified as a function of parameter ε for its variability from 0 to 1. The last column consists of values of the oscillation frequency (denoted as ω') evaluated by comparison of the signal from the model of Van der Pol oscillator with the signal from the reference source, using the three-period signature (Fig. 11). The discrepancy between ω and ω' results from the truncation error in Eq. (6).

Table 2. The total harmonic distortion (THD) and the angular oscillation frequency (ω) versus parameter ε of the Van der Pol oscillator.

ε	THD dB	ω rad/s	ω' rad/s
0	Noise	1	1
0.01	-57.7	0.9999	0.9999
0.02	-52.0	0.9999	0.9999
0.03	-48.4	0.9999	0.9999
0.04	-46.0	0.9999	0.9999
0.05	-44.0	0.9998	0.9998
0.06	-42.5	0.9997	0.9998
0.07	-41.1	0.9996	0.9997
0.08	-40.0	0.9996	0.9996
0.09	-38.9	0.9994	0.9995
0.1	-38.0	0.9993	0.9994
0.2	-31.9	0.9975	0.9975
0.3	-28.3	0.9943	0.9944
0.4	-25.6	0.9900	0.9901
0.5	-23.5	0.9843	0.9847
0.6	-21.6	0.9775	0.9782
0.7	-20.0	0.9693	0.9707
0.8	-18.6	0.9600	0.9622
0.9	-17.2	0.9493	0.9530
1	-16.0	0.9375	0.9429

It is seen from Table 2 that the nonlinear oscillation causes a frequency deviation of the Van der Pol oscillator. Due to this phenomenon the final state of the counter at the end of an evaluation period is not zero but is related to the frequency deviation (Fig. 9).

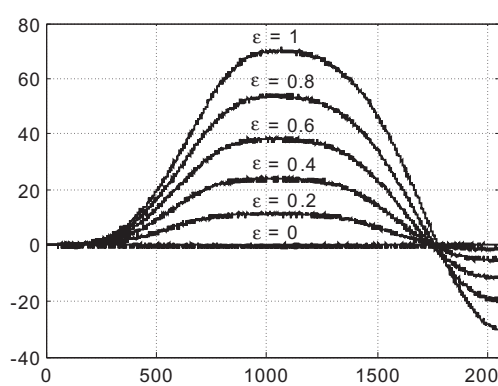

Fig. 9. A family of one-period signatures related to nonlinear oscillations of the Van der Pol oscillator.

The data set containing 200 signatures obtained for ε logarithmically spaced in the range of <0, 1> with randomly chosen amplitude, frequency and phase, was equally divided into two subsets: the training set and the test set. In this case, after the application of PCA, the network architecture was simplified to 3-3-1 (three inputs, 3 neurons in the hidden layer and one neuron with tan-sigmoid transfer function in the output layer). Network targets < −60 dB, -15 dB > were scaled so that they fall in the range of <−1, 1>. The accuracy of evaluation of the THD with the aid of artificial neural network was measured by performing a regression analysis between the ANN responses and the corresponding targets contained in the test set. The identified values exhibit close agreement with the targets and all the identified data lie in the vicinity of the straight line, which represents the best linear fit. The calculated correlation coefficient R = 0,9992 indicates a very good fit. Errors in the THD evaluation depend on the oversampling ratio. Two error plots for different values of OSR are shown in Fig. 10a and 10b. For OSR = 128 the neural network is able to evaluate the THD down to – 40 dB with an error of ± 1 dB. For OSR = 1024 the measuring range is extended to – 60 dB with the same error of ± 1 dB.

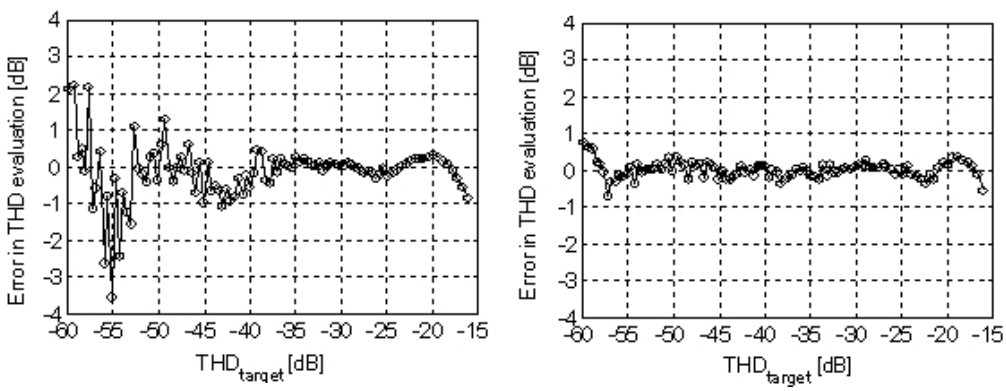

Fig. 10. Errors in THD evaluation with the aid of ANN for oversampling ratio: a) OSR = 128, b) OSR=1024.

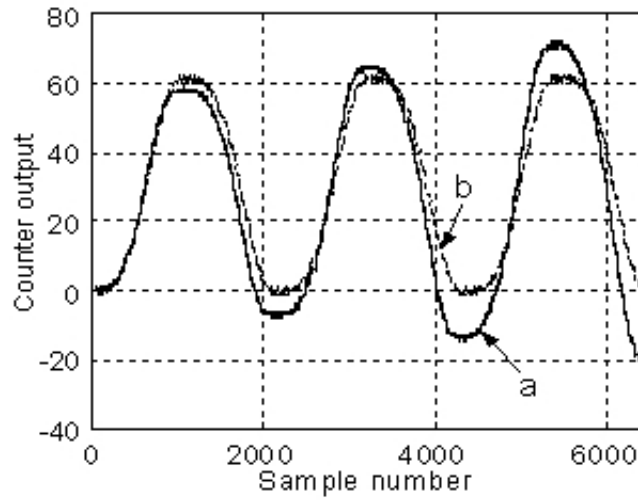

Fig. 11. Three-period signatures for nonlinear oscillation (ε = 1): a) the frequency of the reference signal is greater then the frequency of he signal under test (ω_{ref} = 0.955 > ω' = 0.943), b) the frequency of the reference signal is equivalent to the frequency of the signal under test.

Fine-tuning of the reference frequency to the frequency of signal under test is not necessary for THD evaluation with the aid of ANN. However, it is the way for precise determination of the oscillation frequency. Fig. 11 presents three-period signatures for nonlinear oscillation (ε = 1). Signature (a) corresponds to the case that the frequency of reference signal is greater then the frequency of signal under test (ω_{ref} = 0.955 rad/s > ω' = 0.943 rad/s). Signature (b) refers to the case that the reference frequency is adjusted to the oscillation frequency (ω_{ref} = ω' = 0.943 rad/s). Such a regular shape of signature is characteristic for the frequency equivalence and can be used for the determination of the oscillation frequency ω'.

5. Conclusions

The novelty of the presented BIT scheme is the fusion of two techniques – sigma-delta modulation and artificial neural networks. We have shown that a combination of these techniques gives a simple method for detection, classification and evaluation of nonlinearities, which is a candidate for built-in test strategy. The presented approach has a few advantages, primarily a short measurement time equivalent to one period of the signal under test and low cost, which is an implication of the realization of many tester components by software. In a conventional instrument setup, the analog signal, which has to travel in the long path between the CUT and the tester or measurement instrument, is corrupted by disturbances and the problem of impedance matching. The proposition reduces the distance between the CUT and the

measurement instrument. Placing the tester close to the CUT completely avoids the interface problems. The method can be implemented with dedicated hardware or can make use of the resources available on chip or on board, reconfigured for a test mode. Hence, it is particularly useful for mixed-signal programmable systems on chip (PSoC).

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