IMPLEMENTATION OF THE DIGITAL RECEIVER IN MULTIBEAM LONG-RANGE SONAR

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The article presents the implementation of a digital receiver in multibeam long-range sonar. Developed by the authors of the article, the implementation was part of sonar modernisation on large Polish Navy ships. The article explains the structure of the receiver, its design details and requirements affecting the architecture. The technical solutions regarding the equipment and signal processing algorithms for determining receiving beams for the active and passive mode are discussed. Key to the receiver design is the signal processing module responsible for determining the multibeam spatial filter (beamformer). Aspects of modern data transmission as used in the device are also discussed.

INTRODUCTION

Deployed on Polish Navy ships, multibeam long-range sonars with cylindrical arrays are some of the most complex hydroacoustic systems. In recent years the Department of Marine Electronics Systems has modernised two types of such sonar: ASW keel sonar MG322 on board ORP "Kaszub" corvette and ASW keel sonar SQS56 on board ORP "Kościuszko" frigate, both with a range of about thirty kilometres and powerful transmitting capacity [1]. While the purpose of the upgrade was to improve reliability and simplify the operation, its main objective was to apply modern methods for signal processing. Ultimately, the methods were to improve submarine detection and tracking capacity. To that end, advanced equipment and software was used. The term "modernisation" usually implies the exchange of the majority of sonar units for new ones. The hydroacoustic array unit, however, remains unchanged. Sonars of this type are operated in the active and passive mode. Figure 1 presents a simplified block diagram of sonar identifying the main units of its design.

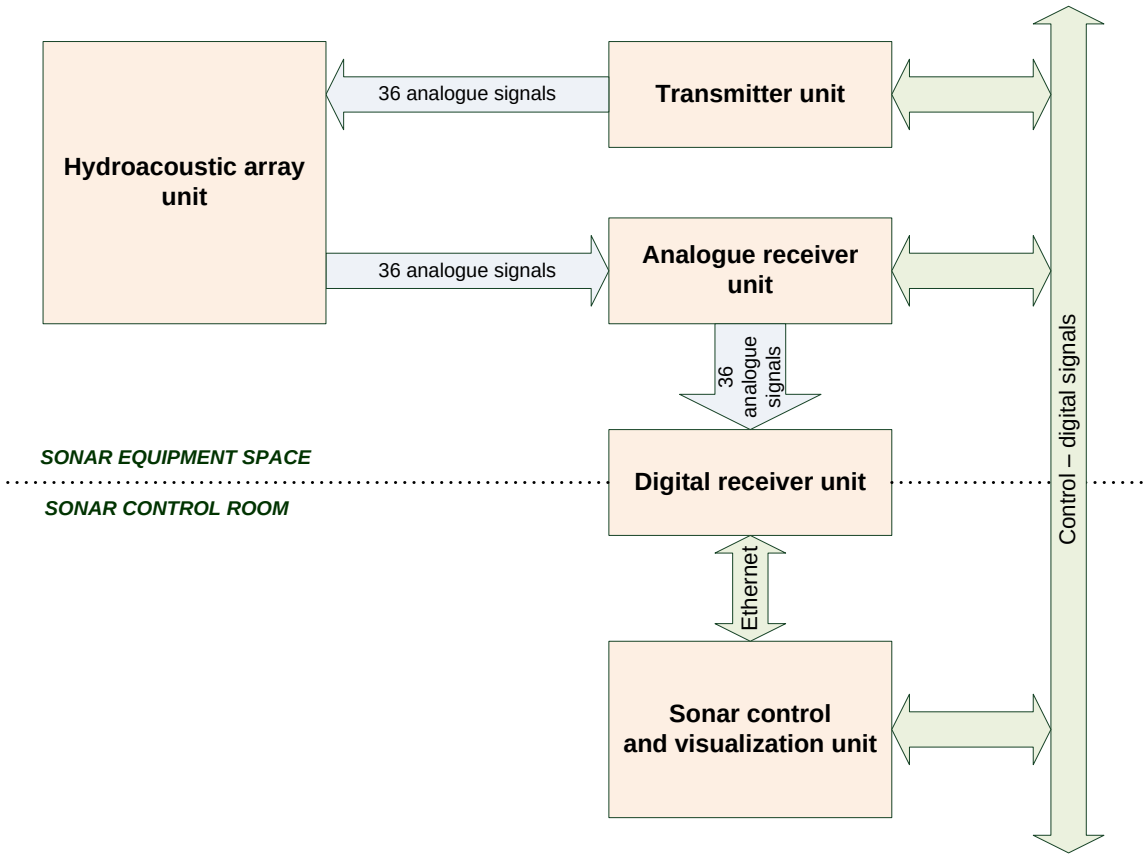

Fig.1. Simplified sonar block diagram.

Array unit comprising a cylindrical 36 column array with each column consisting of several ultrasonic transducers of a specific resonance frequency. Its function is to emit acoustic sounding signals and receive acoustic echo signals. Depending on the design, it may include a block for stabilising array position.

Transmitter unit responsible for producing electric sounding signals. For all types of pulses (PING, LFM - linear frequency modulation, HFM - hyperbolic frequency modulation), low level pulses are fed to power amplifier inputs to be subsequently transferred via transducer compensation systems to all transducers of the hydroacoustic array.

Analogue receiver unit responsible for analogue processing of echo signals. Each signal received from the hydroacoustic array undergoes band filtration and signal gain (TVG - time variable gain).

Sonar control and visualization unit responsible for managing all sonar units and visualizing echo signals. It ensures communications with on-board navigation systems and sound velocity distribution meter. A user interface is used to determine all parameters of sonar operation such as: mode of operation (active/passive/test mode), range, type of pulse, gain, target management, etc. [2].

Digital receiver unit responsible for analogue to digital processing of echo signals and the subsequent generation of receiving beams by using a multibeam spatial filter (beamformer).

The authors of this article and the digital receiver implementation are going to present how the receiver was developed along with its design details and requirements that have determined the final architecture.

The digital receiver unit is divided into two sub-units: one for acquisition and transmission and one for data processing. The reason for this split is that the array, transmitter and analogue receiver units together with the acquisition and transmission sub-unit are close to one another. In addition, they are about 100 metres away from the sonar control and imaging room which also includes the digital receiver data processing sub-unit.

1. ACQUISITION AND TRANSMISSION SUB-UNIT OF THE DIGITAL RECEIVER

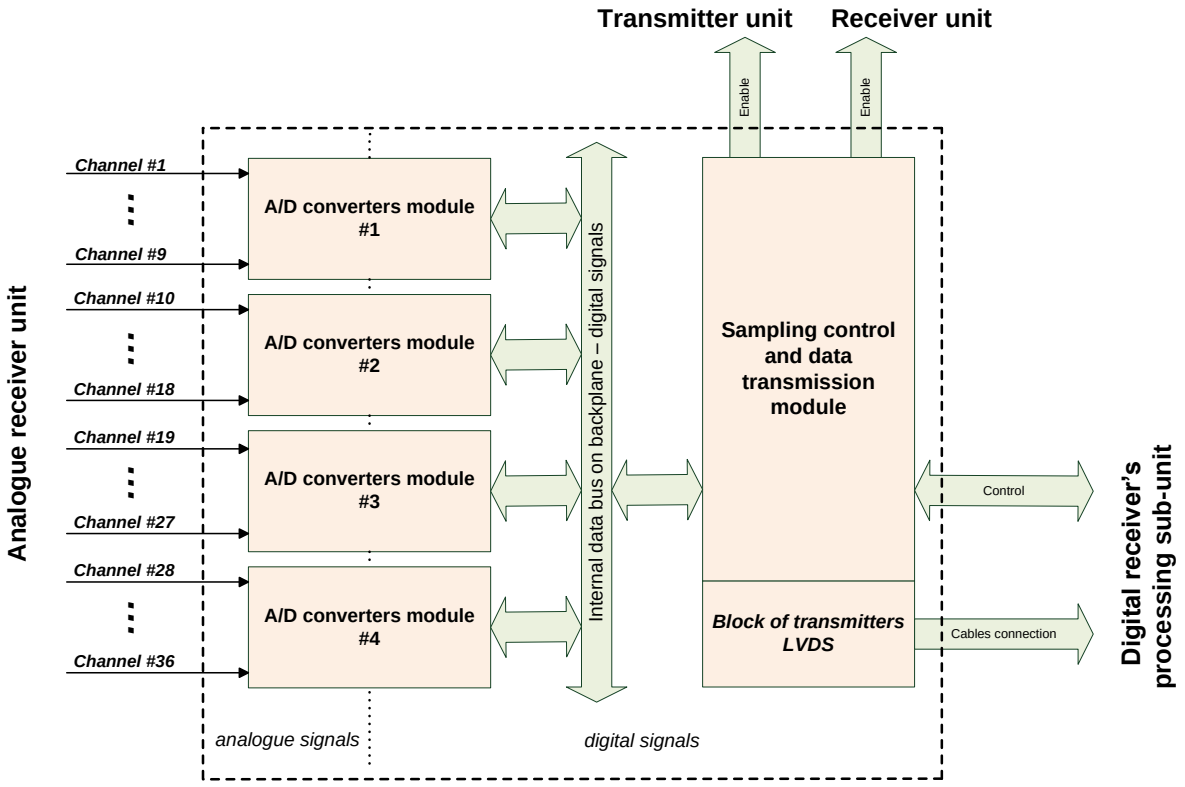

Fig.2. Block diagram of the digital receiver's acquisition and transmission sub-unit.

Analogue signals from ultrasonic transducers, from all of the hydroacoustic array's columns undergo analogue processing in the analogue receiver. They are then sent to the digital receiver, i.e. to analogue to digital converter inputs. The signals are sampled following an agreed procedure and the specific sampling frequency, depending on the sonar's mode of operation, i.e. active, passive or test mode. The signals are sampled simultaneously in all analogue to digital conversion channels.

The sub-unit's subrack contains four modules of analogue to digital converters and a module for controlling sampling and data transmission. In addition, it includes adequate power supply unit (PSU) to power the separate analog and digital blocks. All modules are made in the 6U format and run on a common dedicated base plate.

The converters module contains 9 analogue to digital converters with 16 bit resolution and maximal sampling speed of 1 Msps *(Million samples per second).* The signal

for releasing conversion is transmitted at exactly the same moment to all transducers via the base plate. The result of the conversion is available on the base plate's interface. All digital signals which connect the module are opto-isolated.

The sampling control and data transmission module has a 16-bit MSP430F149 processor, responsible for ensuring communications between the data acquisition and transmission sub-unit and the sonar's control and visualization unit. It also initiates the measurement cycle by signalling the transmitter and receiver to start operation and by starting the data acquisition system. The modules receives samples from converters modules and sends them to the processing sub-unit, as shown in Fig. 3. The condition for the proper send a single frame of sampled measurement data is as follows: $37 * \Delta t \leq t_s$. Where, Δt is the time necessary to send a single data and $t_s=1/f_s$ is sampling time used by the a/d converters.

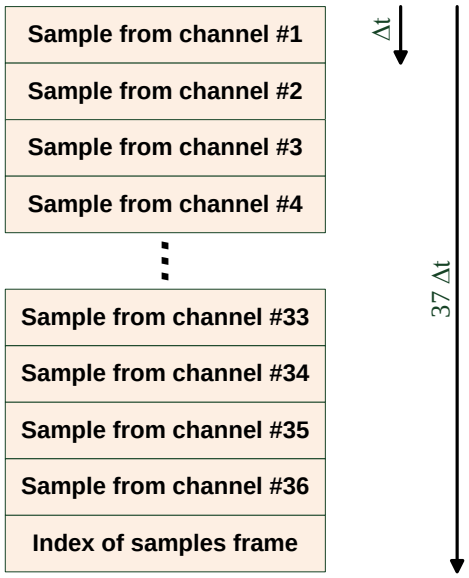

Fig.3. Diagram of sampled measurement data transmission's single frame.

In the active mode and operating frequency of *fc=7500 Hz*, the resulting frequency for quadrature sampling is *fs=4*fc=30000 Hz*. 36 conversion channels are sampled simultaneously at frequency *fs*, and the results undergo quadrature sampling decimation (i.e. in a single channel one quadrature sample is sent for processing and the next e.g. 3 quadrature samples are left out and the process is repeated). As a result, our range resolution is about 20 cm, which for sonar designed for submarine detection is a very satisfying value.

In the passive mode sonar receives acoustic signals emitted by underwater and water surface objects in the frequency band of *3000Hz-10000Hz*. Analogue signals are sampled following Nyquist criterion at a sampling frequency of *fs=32768 Hz*.

The test operation mode is used both for testing the quality of the interface for transmitting data to the processing sub-unit and for understanding the efficiency of the sampling block. To test the transmission interface, we send several different data models known at the receiving end. This tells us the condition of cable connections and how the transmission electronic systems are working. A comprehensive test of the sampling block is conducted using test analogue signals to identify the efficiency of all available sampling channels. Finally, we are informed about the details of sampling channels efficiency which

is also useful for maintenance purposes. If detected, one or more faulty channel both analogue and digital, does not cause a breakdown of the entire sub-unit because the information is sent to the processing sub-unit. The sub-unit takes account of this fact when running beam producing algorithms.

The data transmission interface used for the digital receiver's processing sub-unit connection is based on the LVDS technology *(Low-Voltage Differential Signalling).* This makes sure that data from all analogue to digital channels are sent together with additional information and synchronising signals. LVDS is a technology for sending electric signals using a low voltage differential signal in symmetric copper cables. The speed for a single cable is hundreds of Mbps *(Megabits per second).*

2. PROCESSING SUB-UNIT OF THE DIGITAL RECEIVER

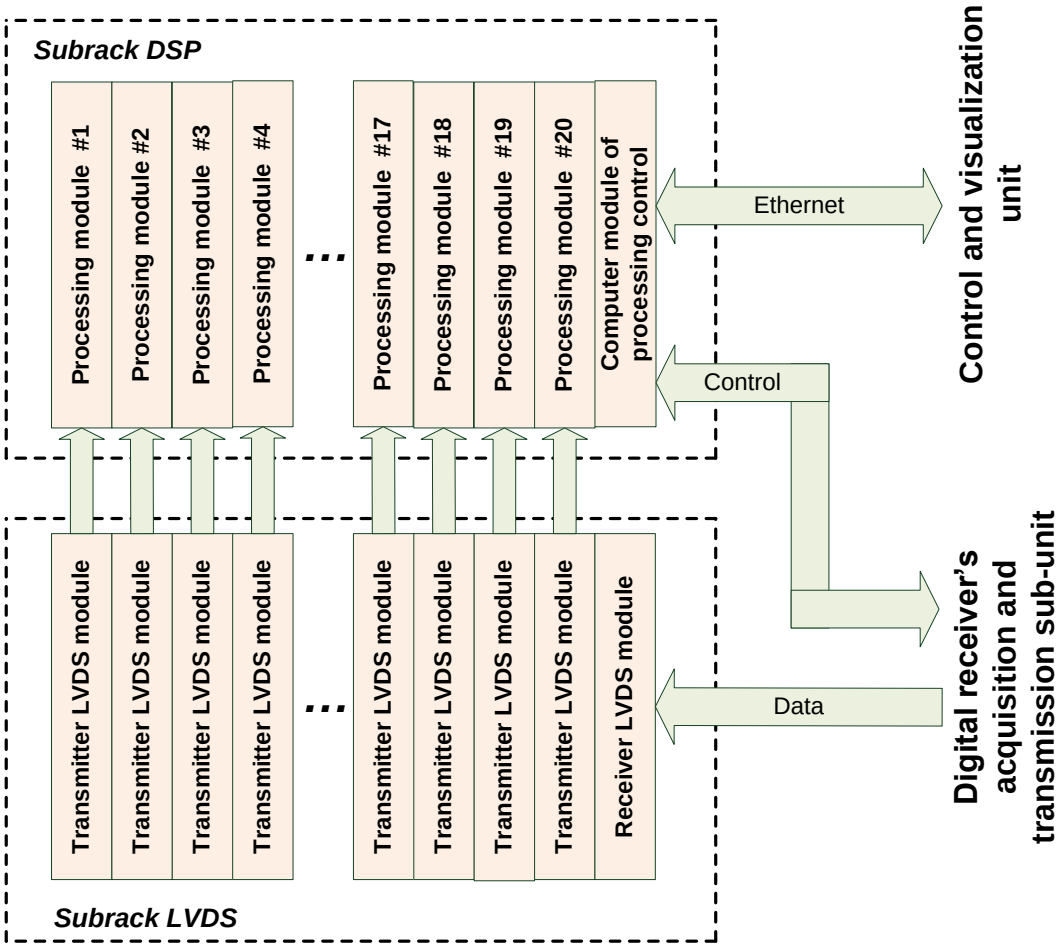

Fig.4. Block diagram of the digital receiver's processing sub-unit.

Responsible for generating receiving beams, this sub-unit uses the multibeam spatial filter (beamformer) in the active and passive mode. Fig. 4 shows a block diagram of the sub-unit. Data from the acquisition and transmission sub-unit are sent to the LVDS subrack, where single channel is multiplied so that the data will reach each of processing modules in the DSP subrack. The objective of processing modules is to process the measurement data; the process

is supervised by an industrial computer. Its function is to control data processing. All modules in the DSP subrack communicate via a CompactPCI interface, an industrial version of the PCI interface. Operating at a resolution of 64 bits and speed of 32 MHz, the interface's maximal capacity is 266 MB/s.

Processing results are consecutively sent from processing modules to the computer in charge of processing control. It then organises the data and sends them to control and visualization computers using the Ethernet network interface with a transmission speed of 1Gb. The other modules in the DSP subrack and all modules in the LVDS subrack are the design of the authors of the article. All modules are made in the 6U format. The LVDS subrack run on a common dedicated base plate. The entire set fits into a 19" subrack. Both subrack contain adequate power supply unit (PSU) to power the digital blocks.

Fig. 5 shows the block diagram of the processing module. Its design ensures an optimal flow of signals and computation performance. The input of the module includes the receiving system of the LVDS interface for receiving measurement data. Behind it are two computational paths. Each path begins with a 64k x 16 bit and 166 MHz timing frequency FIFO. Data from the memory are supplied in successive blocks to be received and then processed by the computational processor. The actual processor used was the most efficient processor at the time of the module design, i.e. a 32-bit, floating-point signal processor by Texas Instruments TMS320C6713B with 300 MHz timing frequency. It has a 256k x 32 bit internal fast static memory, 256k x 32 bit external static memory and a 64MB dynamic memory. While the processor's peak performance is 1800 MFLOPS (*Million Floating Point Operations Per Second*), it can only be used fully if the programme uses all of the available eight streams. This usually implies a labour intensive process to optimise the programme code. The computer in control of data processing via the CompactPCI interface can access the resources of each module. Access to each of the 2 signal processors on the module is convenient through the use of a parallel HPI interface (Host Port Interface). Using this mechanism we can gain unconstrained access to resulting data from each completed processing process and more. In addition, this form of communication is used for loading the programme for the particular signal processors. As a result, the designation of the modules may be changed while they are in operation.

Beams are determined by 18 processing modules, adding up to 36 computational paths. There are additional modules for auxiliary functions such as underwater object tracking and target speed measurement, but first and foremost they are redundant modules. They can be used in case of a breakdown of one of the 18 modules responsible for the sonar's basic task, which is receiving beam determination. The mechanism described above supports this function, which is key to the sonar's purpose.

In the active mode, the processing module produces 72 receiving beams. Each of the available 18 modules receives in-phase and quadrature samples from the array's 36 columns, which were originally used for quadrature detection (two consecutive samples are selected and the next six are omitted). Each of the module's computational paths produces 2 deflected beams. They are generated using 12 consecutive columns forming one sector. The deflection of both axes of neighbouring beams (left and right) versus the straight line cutting through the sector is by -2.5^0 and $+2.5^0$. Beam formation occurs in the multibeam spatial filter by compensating the phases of the signals received. Phase compensation occurs when in-phase and quadrature samples are multiplied by numerical factors. The resulting samples are summed up giving real and imaginary parts of 72 digital signals corresponding to the sonar's 72 receiving beams per a single portion of data. The above mentioned numerical factors are specifically selected to ensure that signal sample multiplication provides

phase shifts and amplitude weighing to reduce the level of side lobes horizontally. In-phase and quadrature signals from 72 outputs of the multibeam spatial filter undergo digital detection. In the case of LFM and HFM signals, correlational detection is used, equivalent to matched filtration. Once processed, the signal is compressed over time. In the case of a PING type signal, envelope detection is used using low-pass digital filters. Both the correlational detection and envelope detection processing based on data in the time domain. In contrast to the processing of data in the frequency domain, where the data must first be collected from all over the range to then make the appropriate calculations, we can partial results obtained to date sent to visualization computers. For such a long range sonar it gives the effect of an almost smooth sweep range.

Because the filter's algorithm is computationally complex, each of the processing module's computational paths is responsible for producing only 2 receiving beams. It gives the possibility to sonar operate in real time.

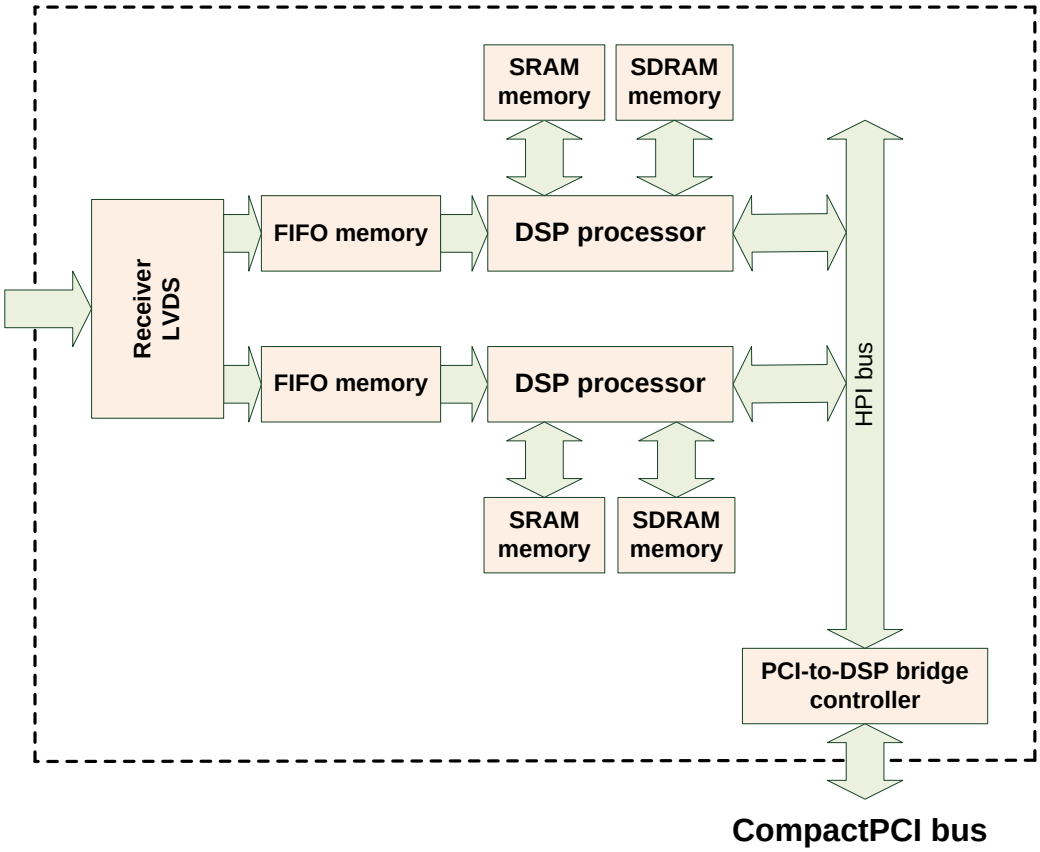

Fig.5. Block diagram of the digital receiver's processing module.

In the passive mode 36 sequences of real samples undergo band filtration in the processing modules. Each channel includes 6 band-pass filters. Their characteristics must be a line and phase characteristics for proper beamformer operation. The 3000Hz-10000Hz operating band is divided into 6 sub-bands. Beam generation occurs in 6 multibeam spatial filters. Each of the spatial filters produces 72 beams covering the round angle in one of the six sub-bands. 72 outputs of each filter have 72 signals positioned in the same way as for the active mode because the principle of filter operation is in fact the same in both modes.

Spatial filters produce a visualisation that tells us about sound emission in a given sub-band from a specific direction.

The objective of signal detection is to determine the right periodogram in each receiving beam. Using samples collected during 1s, 2s or 4s, sequences are made containing 32768, 65536 or 131072 samples respectively. Periodograms are determined by computing the discrete Fourier transform from the set number of samples and computing the square from its module. By using the FFT procedure (Fast Fourier Transform) we can significantly reduce the number of operations to be performed by signal processors. Spectral lines for each beam are sent to imaging computers which select maximal line values from a segment of a data sequence for a subsequent display on the computer screen.

3. CONCLUSION

The digital receiver presented in the article has been successfully implemented in Polish Navy on-board sonars. It is in operation now. The project used cutting-edge technologies available at the time of the modernisation. It has been one of the biggest and most complicated projects we have completed in recent years. It has been an excellent learning experience that added to our understanding of running complex projects both on the hardware and software side. The next step will involve the use of the latest generation of multicore signal processors.

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