BULLETIN OF THE POLISH ACADEMY OF SCIENCES
TECHNICAL SCIENCES, Vol. 62, No. 1, 2014
DOI: 10.2478/bpasts-2014-0009

Bulk linearized CMOS differential pair transconductor for continuous-time OTA-C filter design

B. PANKIEWICZ*, S. SZCZEPAŃSKI, and M. WÓJCIKOWSKI

Department of Microelectronic Systems, Gdańsk University of Technology, 11/12 Narutowicza St., 80-233 Gdańsk, Poland

Abstract. In this paper, the MOS differential pair driven simultaneously from gates and bulk terminals is described. An approximated analytical solution of the voltage to current transfer function has been found for the proposed circuit. Four possible combinations of gate and bulk connections of the input signal are presented. Basing on the configuration giving the best linearity, the operational transconductance amplifier (OTA) has been designed and compared, by computer simulations, to the amplifier utilizing the gate driven classic MOS pair. 3^{rd} order filters using the OTAs with linearized and simple MOS pair have been designed and the resulting parameters have been compared. Linearization through the presented simultaneous use of gate and bulk terminals seems to be useful for low voltage applications.

Key words: transconductance amplifier, OTA, bulk-driven amplifier, OTA-C filter.

1. Introduction

Linear CMOS operational transconductance amplifiers (OTAs) are useful building blocks in the design of analog signal processing systems. The transconductance-capacitor (OTA-C) approach is often used for continuous-time filter design [1–6]. For high frequency applications, numerous circuit techniques to design OTA-C filters have been developed, using the gate-driven differential pair transconductors as input stages of the OTAs [7–13]. On the contrary, the transconductors with bulk-driven differential pair have been proposed for low frequency OTA-C filter applications [14–21].

This paper presents the differential MOS pair, simultaneously driven from gate and bulk terminals. The use of both terminals gives a possibility to change the V-I converter's transconductance in the range of about 60%. Connecting the signal to the bulk terminal requires that the polarization of the bulk-source junction would not enter the conducting state. To fulfill this requirement, input signal buffers in source follower configuration can be used.

The layout of the paper is as follows: in Sec. 2, the authors present the differential MOS transistor pair simultaneously driven from the bulk and the gate terminals, Sec. 3 describes the proposed differential pair together with the source followers and four possible connection combinations. The details about the realization of the OTA amplifier with the linearization achieved by the proper voltage bulk control of MOS pair are given in Sec. 4. An example of 3^{rd} order elliptic filter and the conclusions are presented in Secs. 5 and 6, respectively.

2. Gate and bulk driven MOS pair

There are many papers describing gate driven [7–13] and bulk driven MOS pairs [14–21]. A simple gate driven MOS pair unfortunately has poor linearity of voltage to current conversion, therefore the other voltage to current converters are often used when the linearity is important [7]. On the other hand, the same pair driven from bulk terminals has a much wider linear region of operation, but its transconductance parameter is few times lower [13]. Figure 1 presents the circuit with the MOS pair driven simultaneously from gate and bulk terminals. Differential input voltage v_{ID} is delivered to the gate terminals in such a way, that its common mode value is equal to V_{CMG} and the differential part of v_{ID} is delivered with the gain a. Unfortunately, due to the bulk-source junction, the common mode voltage level of the bulk terminals cannot be the same as for the gates. For the NMOS pair, the common mode level of the bulk terminals should be lower than for the gates. In this paper, the common mode level for the bulk terminals is designated as V_{CMB}. Additionally, it is assumed, that the signal which arrives to the bulk is attenuated and the resulting differential voltage is equal to bv_{ID}. The coefficients a and b for the differential voltages reaching the inputs of NMOS pair are introduced for further investigations of different configurations in connection to a common mode level shifter.

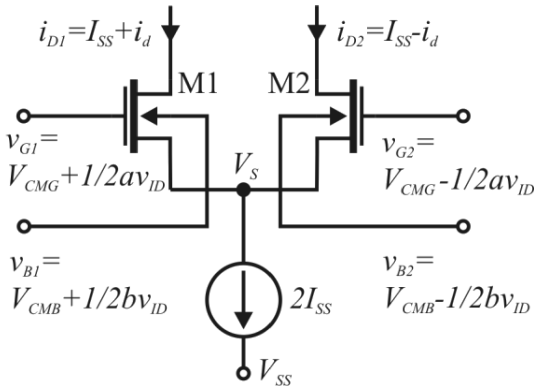

Fig. 1. NMOS differential pair driven both from gate and bulk terminals

*e-mail: bpa@ue.eti.pg.gda.pl

Using the standard square-law model for two identical NMOS devices M1 and M2, their drain currents can be described as:

$$\begin{aligned} i_{D1} &= I_{SS} + i_d = K(V_{GS1} - V_{T1})^2 \\ &= K(V_{CMG} + 0.5av_{ID} - V_S - V_{T1})^2 \end{aligned} \tag{1}$$

and

$$\begin{aligned} i_{D2} &= I_{SS} - i_d = K(V_{GS2} - V_{T2})^2 \\ &= K(V_{CMG} - 0.5av_{ID} - V_S - V_{T2})^2, \end{aligned} \tag{2}$$

where

$$K = 0.5\mu_n C_{OX} W/L,$$

$$V_{T1,2} = V_{T0} + \gamma_n \left(\sqrt{PHI + V_{SB1,2}} - \sqrt{PHI} \right),$$

W and L are the width and the length of MOS devices, respectively, μ_n is the mobility of carriers, C_{OX} is the oxide capacitance by unit area, V_{T0} is the threshold for V_{BS}=0, *PHI* is the surface potential (about 0.6V), V_{SB} is the source-bulk potential and γ_n is the bulk effect parameter. Taking into the account the bulk voltages, which alter the threshold voltages of MOS devices, the drain currents i_{D1} and i_{D2} can be rewritten as:

$$\begin{aligned} i_{D1} &= I_{SS} + i_d = K(V_{CMG} + 0.5av_{ID} - V_S - V_{T1})^2 \\ &= K\Big[V_{CMG} + 0.5av_{ID} - V_S \\ &\quad - \gamma_n \left(\sqrt{PHI + V_S - V_{B1}} - \sqrt{PHI} \right) \Big]^2 \\ &= K\Big[V_{CMG} + 0.5av_{ID} - V_S \\ &\quad - \gamma_n \left(\sqrt{PHI + V_S - V_{CMB} - 1/2bv_{ID}} - \sqrt{PHI} \right) \Big]^2 \end{aligned} \tag{3}$$

and

$$\begin{aligned} i_{D2} &= I_{SS} - i_d = K(V_{CMG} - 0.5av_{ID} - V_S - V_{T2})^2 \\ &= K\Big[V_{CMG} - 0.5av_{ID} - V_S \\ &\quad - \gamma_n \left(\sqrt{PHI + V_S - V_{B2}} - \sqrt{PHI} \right) \Big]^2 \\ &= K\Big[V_{CMG} - 0.5av_{ID} - V_S \\ &\quad - \gamma_n \left(\sqrt{PHI + V_S - V_{CMB} + 1/2bv_{ID}} - \sqrt{PHI} \right) \Big]^2. \end{aligned} \tag{4}$$

After the square root of both sides of (3) and (4) and the subtraction of the resulting equation, one can obtain the following equation:

$$\begin{aligned} &\frac{\sqrt{I_{SS} + i_d} - \sqrt{I_{SS} - i_d}}{\sqrt{K}} \\ &= av_{ID} + \gamma_n \Big(\sqrt{PHI + V_S - V_{CMB} + 1/2bv_{ID}} \\ &\quad - \sqrt{PHI + V_S - V_{CMB} - 1/2bv_{ID}} \Big). \end{aligned} \tag{5}$$

Unfortunately, Eq. (5) cannot be solved against i_d, as it can be done for the standard gate driven pair. However, it is possible to make an estimation using the Taylor expansion of the square root term. The part of the right side term of Eq. (5) can be approximated as:

$$\begin{aligned} &\sqrt{PHI + V_S - V_{CMB} + 1/2bv_{ID}} \\ &- \sqrt{PHI + V_S - V_{CMB} - 1/2bv_{ID}} \\ &= 2\frac{\sqrt{PHI + V_{S0} - V_{CMB}}}{(4PHI + 4V_{S0} - 4V_{CMB})} bv_{ID} \\ &+ \frac{\sqrt{PHI + V_{S0} - V_{CMB}}}{(4PHI + 4V_{S0} - 4V_{CMB})^3} b^3 v_{ID}^3 \\ &+ \frac{7}{4}\frac{\sqrt{PHI + V_{S0} - V_{CMB}}}{(4PHI + 4V_{S0} - 4V_{CMB})^5} b^5 v_{ID}^5 + ..., \end{aligned} \tag{6}$$

where: V_{S0} is the constant value of the voltage seen at V_S for $v_{ID} = 0$, this voltage can be obtained by the calculation of the operating point. Unfortunately, taking into the account the bulk effect, there is no analytical solution for V_{S0}, but neglecting the bulk effect only for the operating point calculations, the voltage V_{S0} can be approximated as:

$$V_{S0} \approx V_{CMG} - V_{T0} - \sqrt{I_{SS}/K}. \tag{7}$$

As (6) is an odd function of v_{ID}, all even terms of Taylor expansions are equal to 0. Taking only the first order coefficient, Eq. (5) can be approximated by:

$$\begin{aligned} &\frac{\sqrt{I_{SS} + i_d} - \sqrt{I_{SS} - i_d}}{\sqrt{K}} \\ &\approx av_{ID} + \frac{b\gamma_n}{2\sqrt{PHI + V_{S0} - V_{CMB}}} v_{ID} \\ &= v_{ID} \left(a + \frac{b\gamma_n}{2\sqrt{PHI + V_{S0} - V_{CMB}}} \right). \end{aligned} \tag{8}$$

Finally, the output current i_d of gate and bulk driven differential pair can be approximated by (9):

$$\begin{aligned} i_d &\approx \left(a + \frac{b\gamma_n}{2\sqrt{PHI + V_{S0} - V_{CMB}}} \right) \sqrt{I_{SS}K} v_{ID} \\ &\cdot \sqrt{1 - \left(a + \frac{b\gamma_n}{2\sqrt{PHI + V_{S0} - V_{CMB}}} \right)^2 \frac{K}{4I_{SS}} v_{ID}^2}. \end{aligned} \tag{9}$$

Similarly, as for the gate driven pair, Eq. (9) is valid only for the limited range of the input voltage:

$$|v_{ID}| \leq \left(a + \frac{b\gamma_n}{2\sqrt{PHI + V_{S0} - V_{CMB}}} \right)^{-1} \sqrt{\frac{2I_{SS}}{K}}. \tag{10}$$

Defining the term in the first parenthesis of (9) as gain factor *GF*:

$$GF = \left(a + \frac{b\gamma_n}{2\sqrt{PHI + V_{S0} - V_{CMB}}} \right). \tag{11}$$

Equations (9) and (10) can be rewritten as:

$$i_d \approx GF\sqrt{I_{SS}K} v_{ID} \sqrt{1 - GF^2 \frac{K}{4I_{SS}} v_{ID}^2}, \tag{12}$$

$$|v_{ID}| \leq \frac{1}{GF}\sqrt{\frac{2I_{SS}}{K}} = V_{IDMAX}. \tag{13}$$

The *GF* term has the physical meaning of the transconductance gain in respect to the simple gate only driven MOS pair's transconductance. Additionally, in order to prevent from significant bulk currents, the bulk-source junction should be reversely biased and this condition can be more difficult to meet than (13).

3. Gate and bulk driven MOS pair with level shifter

Due to the bulk-source semiconductor junction, the simultaneously driven from gate and bulk terminals differential MOS pair from Fig. 1 must have different common mode input voltage levels V_{CMG} and V_{CMB}. The simplest way to obtain such a shift is to use the MOS device in a source follower (CD) configuration. Figure 2(a) presents such a circuit. Using the standard square-law models for MOS device, the voltage shift between the input and the output can be estimated as:

$$\begin{aligned} V_{SHIFT} &= \sqrt{I_B/K_1} + V_{T1} \\ &= \sqrt{I_B/K_1} + V_{T0} + \gamma_n\left(\sqrt{PHI + V_{SB1}} - \sqrt{PHI}\right) \\ &\approx \sqrt{I_B/K_1} + V_{T0}. \end{aligned} \tag{14}$$

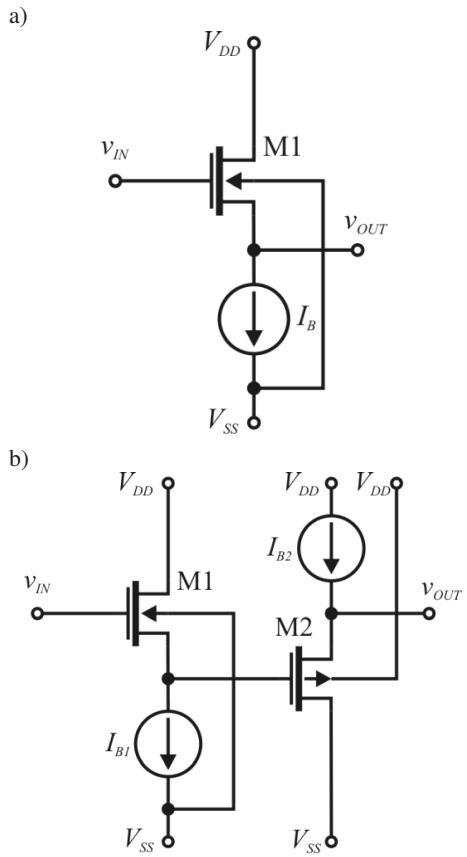

Fig. 2. Signal level shifters (a) source follower, (b) twin source follower

For a single MOS voltage follower, the voltage shift cannot be lower than the threshold voltage of the MOS device. If the reverse shift is required, the PMOS device should be used instead of the NMOS one. The changes of the shift voltage can be made by the change of the bias current I_B. If smaller shifts than the threshold voltage of MOS device are required, double NMOS and PMOS source followers can be used. For such a circuit, the voltage shift can be estimated using (15).

$$\begin{aligned} V_{SHIFT} &= \sqrt{I_{B1}/K_1} + V_{T1} - \sqrt{I_{B2}/K_2} + V_{T2} \\ &= \sqrt{I_{B1}/K_1} + V_{T0n} + \gamma_n\left(\sqrt{PHI + V_{SB1}} - \sqrt{PHI}\right) \\ &- \sqrt{I_{B2}/K_2} + V_{T0p} + \gamma_p\left(\sqrt{PHI + V_{BS2}} - \sqrt{PHI}\right) \\ &\approx \sqrt{I_{B1}/K_1} + V_{T0n} - \sqrt{I_{B2}/K_2} + V_{T0p}. \end{aligned} \tag{15}$$

For the twin source follower, both positive and negative voltage shifts can be generated.

The source followers from Fig. 2 have its bulk terminals tied to the power supply lines V_{SS} and V_{DD}, accordingly. Due to this, a small signal gain A_{SH} for circuit from Fig. 2(a) is much lower than ideal 1 and it can be expressed as:

$$A_{SH} = \frac{v_{out}}{v_{in}} = \frac{r_o g_m}{1 + r_o g_m + r_o g_{mb}}, \tag{16}$$

where r_o is the internal resistance of the bias current source I_B, $g_m = 2\sqrt{K_1 I_B}$ is the gate small-signal transconductance, $g_{mb} = \sqrt{K_1 I_B}\gamma_n / \left(\sqrt{PHI + V_{SB1}}\right)$ is the bulk small-signal transconductance and V_{SB1} is the constant bulk-source voltage in the operating point of the source follower. Assuming that r_o is high comparing to $1/g_m$ and using the equations for both small-signal transconductances, the final source follower gain A_{SH} can be expressed as:

$$\begin{aligned} A_{SH} &= \frac{v_{out}}{v_{in}} \approx \frac{g_m}{g_m + g_{mb}} \\ &= \frac{2\sqrt{PHI + V_{SB1}}}{\gamma_n + 2\sqrt{PHI + V_{SB1}}}. \end{aligned} \tag{17}$$

For the real source followers, the gain expressed by (17) is in the range 0.65–0.85, depending on the MOS devices' dimensions and the bias current used. Twin source follower has its gain more dumped and it can be estimated using:

$$\begin{aligned} A_{SH} = \frac{v_{out}}{v_{in}} &= \frac{2\sqrt{PHI + V_{SB1}}}{\gamma_n + 2\sqrt{PHI + V_{SB1}}} \\ &\cdot \frac{2\sqrt{PHI + V_{BS2}}}{|\gamma_p| + 2\sqrt{PHI + V_{BS2}}}. \end{aligned} \tag{18}$$

As stated before, the MOS pair driven simultaneously from gate and bulk terminals has to use signal level shifters. To preserve the proper bulk terminal polarization of the NMOS pair, the gates' common level should be shifted up

or the bulks' common level should be shifted down, in respect to the input common mode level. Additionally, the bulk terminals can be connected straight or crossed in respect to the gates, realizing the positive and the negative values of the bulk gain b, respectively. Summing all the combinations for one MOS pair with two source followers, four combinations of the resulting amplifier have been proposed, as shown in Table 1. Plot of the transconductance g_m, which is defined as the current's i_d derivative in respect to the input voltage v_{ID}, is plotted in Fig. 3 for all four configurations. According to Eq. (12), the output cur rent is scaled proportionally to *GF* and the nonlinear term under the square root is squared. In this way, when *GF* is smaller than one, the linearity of the circuit is improved. The shifter gain A_{SH} is always smaller than 1, so the best linearity is obtained when the shifters-followers are connected to gates, while bulk terminals are crossed (fourth row in Table 1). Such a circuit configuration is presented in Fig. 4.

The input voltage at which the amplifier saturation occurs can be calculated from (13). Similarly, one can calculate the input voltage level $v_{IDError}$ at which the output current i_d reaches the relative error equal to E from the expression (19).

$$GF\sqrt{I_{SS}K}v_{ID}\sqrt{1-GF^2\frac{K}{4I_{SS}}v_{ID}^2} \geq (1-E)\,GF\sqrt{KI_{SS}}v_{ID}. \tag{19}$$

Solving (19) for v_{ID}, denoted as the boundary condition $v_{IDError}$, the following result has been obtained:

$$v_{IDError} = \sqrt{\frac{4I_{SS}}{K}}\frac{1}{GF}\sqrt{1-(1-E)^2} = \sqrt{2}V_{IDMAX}\sqrt{1-(1-E)^2}. \tag{20}$$

From (20) it is obvious, that for the higher linearity, a higher current I_{SS} and a lower factor K is required. Unfortunately, such a change needs the higher values of the gate to source voltages for the MOS devices, what requires the increased power supply voltage. Alternatively, one can lower the *GF* factor and the increased linearity can be obtained without a need of the increased power supply voltages.

Table 1
Possible connections of the level shifters to the NMOS gate and bulk driven pair

No.	Connection of the source follower of gain A_{SH}	Resulting value of gain factor
1	followers to the bulks, bulks straight	$GF = \left(1 + \frac{A_{SH}\gamma_n}{2\sqrt{PHI + V_{S0} - V_{CMB}}}\right)$
2	followers to the bulks, bulks crossed	$GF = \left(1 - \frac{A_{SH}\gamma_n}{2\sqrt{PHI + V_{S0} - V_{CMB}}}\right)$
3	followers to the gates, bulks straight	$GF = \left(A_{SH} + \frac{\gamma_n}{2\sqrt{PHI + V_{S0} - V_{CMB}}}\right)$
4	followers to the gates, bulks crossed	$GF = \left(A_{SH} - \frac{\gamma_n}{2\sqrt{PHI + V_{S0} - V_{CMB}}}\right)$

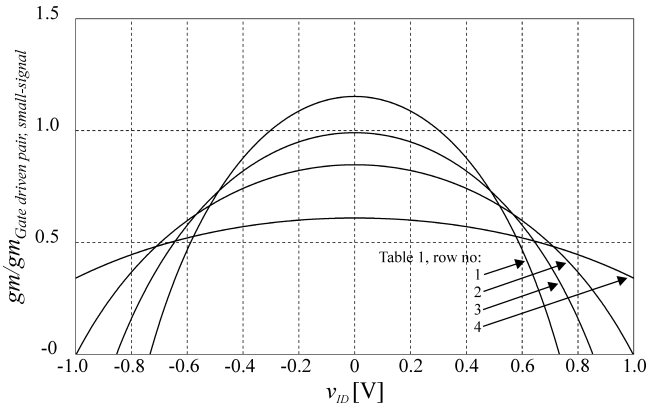

Fig. 3. The plot of the transconductance (12) versus input voltage for all four configurations shown in Table 1. The presented transconductance is normalized to small-signal transconductance of a simple gate driven MOS pair. The plot is made for the following values of the parameters: $I_{SS} = 10$ μA, $K = 28$ μA/V^2, $A_{SH} = 0.8$, $\gamma_n = 0.4$, $V_{S0} - V_{CMB} = 0.5$ V and $PHI = 0.6$ V

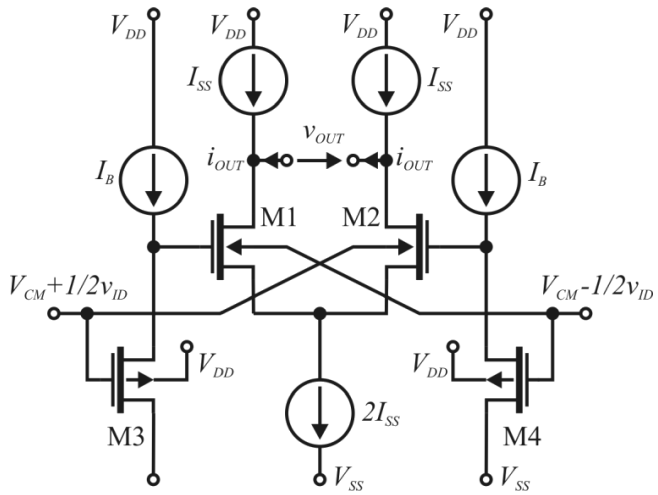

Fig. 4. NMOS pair driven simultaneously through gate and bulk terminals with the gates connected to voltage shifters and with the crossed bulks. It refers to the row 4 in Table 1

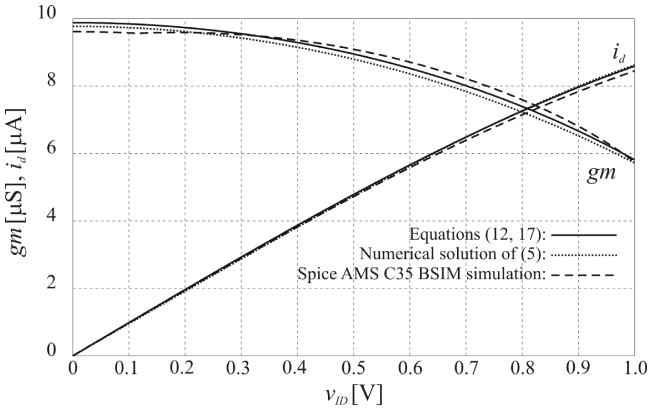

Fig. 5. The output current and the transconductance for the circuit from Fig. 4, using Eqs. (12), (17), with the numerical solution of the expression (5) and simulated using SPICE and AMS C35 BSIM MOS models. The plots have been made for the following values of parameters: $K_N = 56\ \mu A/V^2$, $K_P = -20.7\ \mu A/V^2$, $(W/L)_{M1,2} = 1/2$, $(W/L)_{M3,4} = 2.5/1$, $V_{T0n} = 0.4979$ V, $V_{T0np} = -0.6915$ V, $PHI = 0.6$ V, $\gamma_n = 0.4$, $\gamma_p = -0.4$, $V_{DD} - V_{SS} = 3.3$ V, $I_{SS} = 10\ \mu$A and $I_B = 5\ \mu$A

To confirm the assumptions and the analyses, the computer simulations were done. Figure 5 presents the comparison of the output current for the circuit of Fig. 4 calculated using Eqs. (12), (17) with numerical calculations of (5) and with SPICE simulations using BSIM AMS C5 models. As it can be observed, Eqs. (12), (17) give a reasonable accuracy comparing to SPICE simulations.

4. Design of the linearized Bulk-driven CMOS OTA

As an example, a fully differential operational transconductance amplifier has been designed and simulated, using AMS C35 CMOS technology. As it is n-well process, only the PMOS devices can be designed with bulk terminals not connected to the highest positive voltage. Due to this, PMOS pair is used in the input stage. All other PMOS and NMOS devices have their bulk terminals connected to V_{DD} or V_{SS} terminals, respectively. The schematic diagram of the OTA is presented in Fig. 6. The transistors M1-M2 form the differential pair with the bulk terminals used for linearization, similarly as in Fig. 4. The devices M3 and M4 are the source followers, with the current sources built with Mb6 and Mb7. The transistors Mb1-Mb4 are the current mirrors with the devices Mb1b-Mb4b, which form CMFB working in deep ohmic region. The current source I_{BIAS} is copied to the input pair as well as to the source followers and the output stage. The devices M5-M8 form the output current mirror. Small capacitors C_{C1} and C_{C2} are used for frequency compensation.

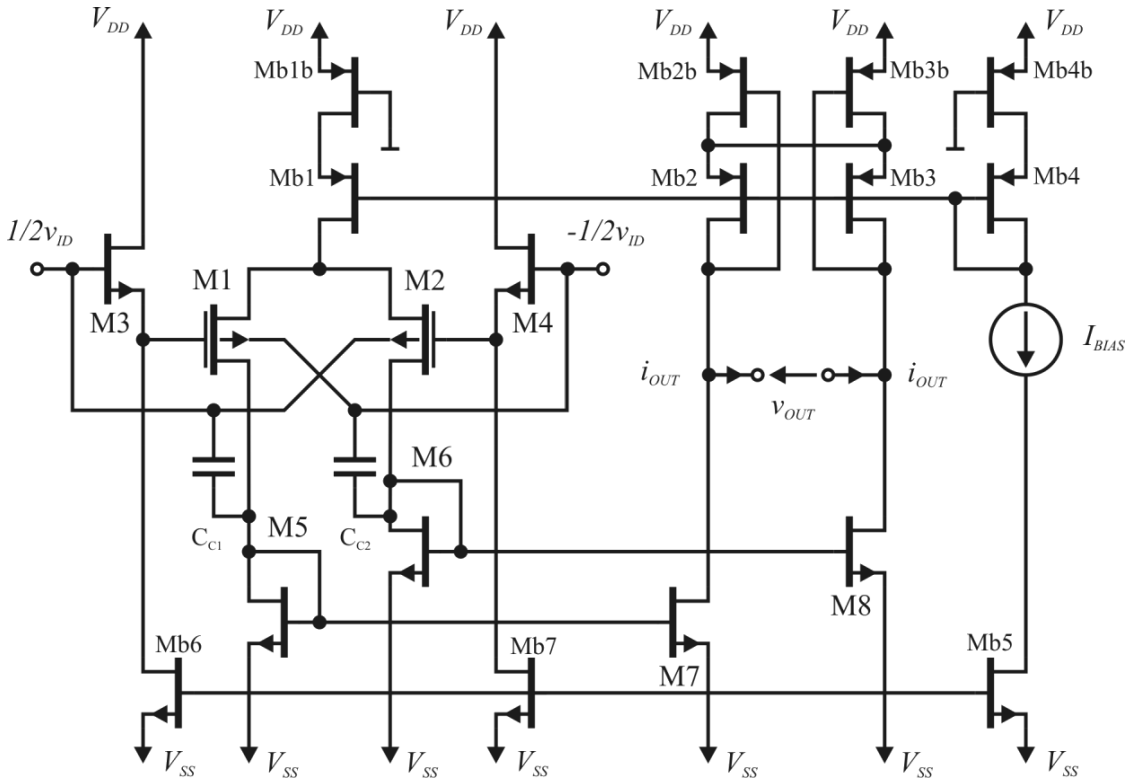

Fig. 6. Schematic diagram of the proposed OTA

Table 2
The simulation results of the OTAs

	OTA designed according to Table 1 row 4	OTA designed using single MOS pair
Supply voltage	3.3 V	3.3 V
Power consumption	58 μW	32.9 μW
Transcounductance	3.914 μS	7.301 μS
Transconductane change for $I_{BIAS} = 2$ μA-3 μA	3.54 μS – 4.24 μS 17.8% change	6.62 μS – 7.81 μS 16.3% change
Open loop voltage gain	40.1 dB	45.7 dB
3 dB frequency of output current (for uncompensated OTA)	68.4 MHz	135.7 MHz
Integrated input referred noise (0.001–10 MHz)	700.5 μV_{RMS}	313.7 μV_{RMS}
THD (@ 100 kHz)	-40 dB @ $V_{ID} = 0.43$ V	-40 dB @ $V_{ID} = 0.18$ V
Dynamic range (@ THD = -40 dB)	52.8 dB	52.2 dB
CMRR (WC @100 MC @ 0.5% V_T and K)	58 dB	53.3 dB
PSRR$^+$ (WC @100 MC @ 0.5% V_T and K)	70.6 dB	51.9 dB
PSRR$^-$ (WC @100 MC @ 0.5% V_T and K)	56 dB	73.2 dB
V_{INOFFSET} (WC @100 MC @ 0.5% V_T and K)	32 mV	14.5 mV
Equivalent differential input capacitance	15.1 fF	15.9 fF
Equivalent differential output capacitance	4.7 fF	4.7 fF
CM dc output voltage change	22 mV	34 mV

The OTA from Fig. 6 and the OTA utilizing only the PMOS pair (without source followers at the input and with bulk terminals tied to V_{DD}), were simulated and compared. The simulation results are summarized in Table 2. It can be observed that the high linearization has been achieved, as compared to a simple MOS pair. Unfortunately, the noise in the linearized OTA is higher, resulting in the same levels of the dynamic range for both realizations of the amplifiers. The 3dB bandwidth of the linearized amplifier is about two times smaller than the reference one, based on MOS pair. While the transconductance is also two times smaller, the linearized amplifier is more suitable for lower frequencies and bandwidth degradation is not really important. Offset currents at the output of the amplifier for both amplifiers have similar values, but it is higher for the amplifier with lower transconductance, when referred to the input. Small capacitors C_{C1} and C_{C2} are used for frequency compensation.

The main advantage of the linearized amplifier, in respect to the single MOS pair, is the possibility to enhance the linearity without the need of increasing the power supply voltage, as it has been explained in Sec. 3, Eq. (20).

5. OTA-C filter design

As an example, a third-order elliptic filter has been designed and simulated using the OTA from Fig. 6. The normalized passive prototype filter is given in Fig. 7 and its active implementation is shown in Fig. 8. Figure 9 presents the obtained simulated amplitude frequency response. Table 3 includes simulated parameters of the filter.

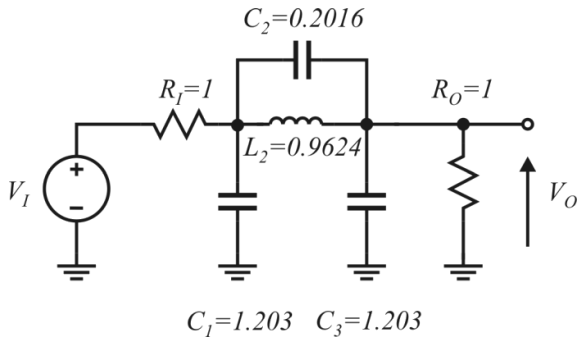

Fig. 7. Normalized passive prototype of the 3^{rd} order elliptic filter

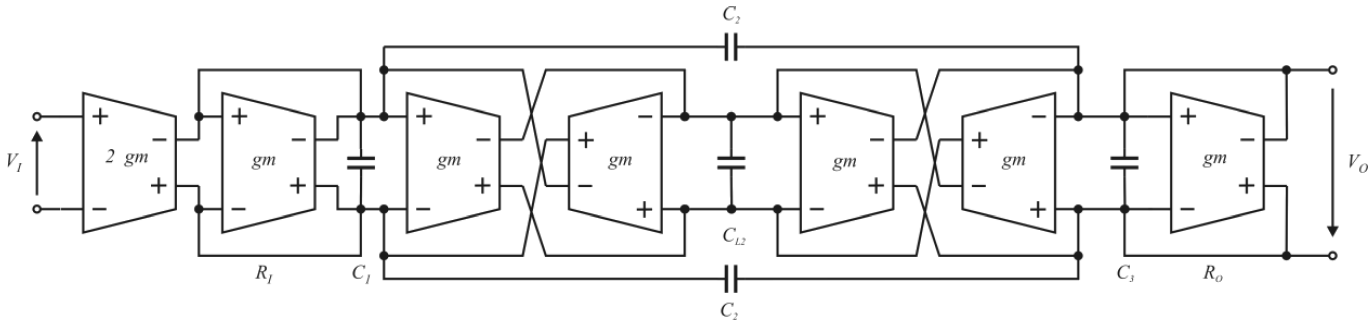

Fig. 8. Active single output OTA implementation of the ladder filter of Fig. 7

Table 3
Simulation results of the filter. The filter type: 3^{rd} order elliptic low-pass with designed 1 MHz cut-off frequency

Parameter	Value	
	Filter implemented with the linearized OTAs of Fig. 6	Filter implemented with classic OTAs using PMOS
Supply voltage	3.3 V	3.3 V
Power consumption	464 mW	321 mW
Simulated cut-off frequency	1.004 MHz	0.993 MHz
Notch depth	−72 dB	−62 dB
DC gain	−0.35 dB	−0.09 dB
Integrated input referred noise (0.01–1 MHz)	362 μV_{RMS}	159 μV_{RMS}
THD (@ 100 kHz)	−40 dB @ $V_{ID} = 0.52$ V	−40 dB @ $V_{ID} = 0.26$ V
Dynamic range (@ THD = −40 dB)	60.1 dB	61.3 dB
DC gain change (@100 MC @ 0.5% V_T and K)	−0.638 – −0.145 dB	−0.38 – +2.2 dB
Cut-off frequency change (@100 MC @ 0.5% V_T and K)	994.5–1015.6 kHz	958–1012 kHz

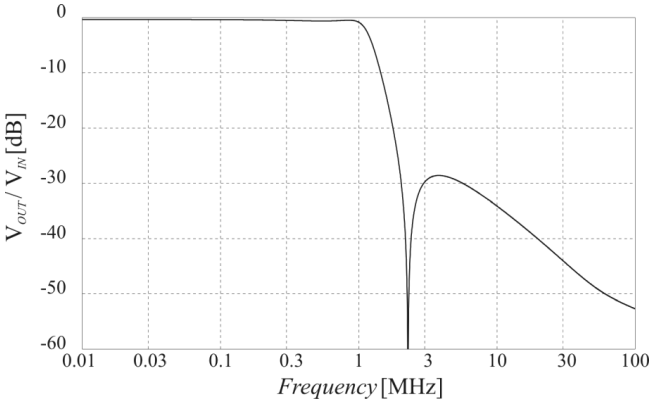

Fig. 9. Simulated response of the filter from Fig. 8 with the OTA from Fig. 6, simulated using SPICE and AMS C35 BSIM MOS models

6. Conclusions

This work presents the MOS transistor pair driven simultaneously from gate and bulk terminals, for which the approximated analytical solution of the V-I transfer function has been found and the configuration of the greatest linearity of the V-I converter has been proposed. For this configuration, fully differential OTA amplifier has been designed and its parameters have been compared with the amplifier using classic differential pair of MOS transistors. Finally, two elliptic 3rd order filters have been designed, using the proposed amplifier and the classic one. Both the amplifiers and the filters have similar signal to noise dynamic ranges, but the proposed linearized amplifier is capable of processing signals of greater values, at the cost of introducing more noise, comparing to the classic MOS pair based amplifier. The linearized MOS pair presented in this paper can be used at lower power supply voltage than the classic differential pair with similar large signal properties. This is particularly important due to the continuous trend of decreasing the power supply voltages in modern CMOS processes.

REFERENCES

[1] S. Koziel and S. Szczepanski, *General Approach to Continuous-Time OTA-C Filters*, WKŁ, Warsaw, 2011.
[2] T. Deliyannis, Y. Sun, and J.K. Fidler, *Continuous – Time Active Filter Design*, CRC Press, USA, 1999.
[3] R. Schaumann, M.S. Ghausi, and K.R. Laker, *Design of Analog Filters: Passive, Active RC and Switched Capacitor*, Engelwood Cliffs, NJ, Prentice-Hall, 1990.
[4] R.L. Geiger and E. Sanchez-Sinencio, "Active filter design using operational transconductance amplifiers: a tutorial", *IEEE Circuits Devices Mag.* 2 (1), 20–32 (1985).
[5] S. Koziel, S. Szczepanski, and R. Schaumann, "A general approach to continuous-time Gm-C filters", *Int. J. Circuit Theory and Applications* 31 (4), 361–383 (2003).
[6] G. Blakiewicz, "Technique to improve CMRR at high frequencies in CMOS OTA-C filters", *Bull. Pol. Ac.: Tech.* 61 (3), 697–703 (2013).
[7] S.T. Dupie and M. Ismail, "High frequency CMOS transconductors", in *Analogue IC Design: The Current-Mode Approach*, eds. C. Toumazou, F.J. Lidgey, and D.G. Haigh, Peter Peregrinius, London, 1990.
[8] S. Szczepanski, S. Koziel, and R. Schaumann, "CMOS differential pair transconductor with active – error feedback", *Proc. IEEE Int. Conf. on Electronics, Circuits and Systems (ICECS)* 1, 168–171 (2003).
[9] J. Glinianowicz, J. Jakusz, S. Szczepanski, and Y. Sun, "High-frequency two-input CMOS OTA for continuous-time filter applications", *IEE Proceedings Circuits, Devices and Systems* 147 (1), 13–18 (2000).
[10] B. Nauta, *Analog CMOS Filters for Very High Frequencies*, Kluwer Academic Publishers, London, 1993.
[11] S. Szczepanski, J. Jakusz, and R. Schaumann, "A linear fully balanced CMOS OTA for VHF filtering applications", *IEEE Trans. on Circuits and Systems – II: Analog and Digital Signal Processing* 44 (3), 174–186 (1997).
[12] S. Koziel and S. Szczepanski, "Design of highly linear tunable CMOS OTA for continuos-time filters", *IEEE Trans. on Circuits and Systems – II: Analog and Digital Signal Processing* 49 (2), 110–122 (2002).
[13] A. Guzinski, M. Bialko, and J.C. Matheau, "Body-driven differential amplifier for application in continuous-time active C-

filter", *Proc. Eur. Conf. on Circuit Theory and Design (ECTD)* 1, 315–320 (1987).

[14] T. Kulej, "Low voltage low transconductance OTA in 50 nm CMOS", *Int. Conf. Signal and Electronic Systems (ICSES)* 1, 273–276 (2010).

[15] A. Veeravalli, E. Sanchez-Sinencio, and J. Silva-Martinez, "Transconductance amplifier structures with very small transconductances: a comparative design approach", *IEEE J. Solid-State Circuits* 37 (6), 770–775 (2002).

[16] M.J. Carrillo, G. Torelli, M.A. Dominguez, and J.F. Duque-Carrillo, "On the input common-mode voltage range of CMOS bulk-driven input stages", *Int. J. Circuit Theory and Applications* 39 (6), 649–664 (2011).

[17] G. Raikos and S. Vlassis, "Low-voltage bulk-driven input stage with improved transconductance", *Int. J. Circuit Theory and Applications* 39 (3), 327–339 (2011).

[18] G. Raikos and S. Vlassis, "0.5-V bulk-driven differential amplifier", *Int. J. Circuit Theory and Applications*, online publication, DOI: 10.1002/cta.1820 (2012).

[19] S. Chatterjee, Y. Tsividis, and P. Kinget, "0.5-V analog circuit techniques and their application in ota and filter design", *IEEE J. Solid-State Circuits* 40 (12), 2373–2387 (2005).

[20] R. Fried and C.C. Enz, "Bulk-driven MOS transconductor with extended linear range", *Electronics Letters* 32, 638–640 (1996).

[21] B. Pankiewicz and S. Szczepanski, "Body-tunable CMOS OTA for continuous-time analog filter applications", *Proc. IEEE Int. Conf. Electronics Circuits and Systems (ICECS)* 1, 132–135 (1996).