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A HIGH-EFFICIENT LOW-VOLTAGE RECTIFIER FOR CMOS TECHNOLOGY

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Abstract

A new configuration of rectifier suiting CMOS technology is presented. The rectifier consists of only two n-channel MOS transistors, two capacitors and two resistors; for this reason it is very favourable in manufacturing in CMOS technology. With these features the rectifier is easy to design and cheap in production. Despite its simplicity, the rectifier has relatively good characteristics, the voltage and power efficiency, and bandwidth greater than 89%, 87%, and 1 GHz, respectively. The performed simulations and measurements of a prototype circuit fully confirmed its correct operation and advantages.

Keywords: CMOS rectifier, high frequency rectifier, wireless power transmission.

1. Introduction

In recent years, techniques for wireless power supply of electronic equipment are very popular. Such techniques are often used to power: sensors, biomedical devices, RFID tags, optical detectors, *etc*. [1–6]. In wireless power systems, energy is transferred by means of the alternating electromagnetic field, which induces the AC voltage in a receiving coil. One of the more difficult problems to solve is developing a rectifier capable of highly efficient conversion of a small-amplitude AC voltage to the DC voltage. The literature describes a number of rectifier solutions adapted to the requirements of CMOS technology [7–14]. A characteristic feature of such rectifiers is relatively low efficiency of rectifying small-amplitude voltages. There are several reasons of low efficiency in these circuits, namely: the threshold voltage of MOS transistors working as voltage controlled switches, the resistance of switched-on transistors, and the reverse flow of the leakage current [7]. To reduce the negative influence of a relatively big threshold voltage, a bootstrapping technique was proposed in [9, 10]. Although the method enables increasing the voltage that controls switching on and off the transistors, it has a serious drawback. In order to effectively boost the voltages, additional capacitors with a relatively big capacitance (in the range of hundreds of pF) are necessary, which are very costly in production in CMOS technology. The bad effect of a relatively high on-resistance can be also reduced either by boosting the gate voltage or by increasing the channel width of MOS transistors. However, increasing the channel width results in reduction of the rectifier bandwidth, which limits its application to a low frequency range. The last of the aforementioned problems, the reverse flow of the leakage current, is frequently solved by using complicated circuits for controlling the moments of switching on and off the MOS transistors. Due to the need for using voltage comparators, such solutions have a very limited bandwidth, typically below 20–30 MHz [12, 13].

The rectifier proposed in this paper enables achieving a good trade-off between the power efficiency, bandwidth, circuit complexity, and cost of production in CMOS technology. The

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reminder of this paper contains: in Section 2 – introduction to the principle of the proposed rectifier operation and its properties, in Section 3 – the measurements and comparison of rectifiers, and in Section 4 – the final conclusion.

2. CMOS voltage rectifier

2.1. Principle of operation

The basic configuration of the proposed voltage rectifier is presented in Fig. 1. The rectifier consists of only two n-channel MOS transistors MN_1 and MN_2, capacitors C_1 and C_2, and resistors R_1 and R_2. For proper operation, the rectifier requires a coil (L_2+L_3) with a central tap. In most wireless power supply systems, such a coil configuration can be easily achieved by adding a central tap to the receiving coil.

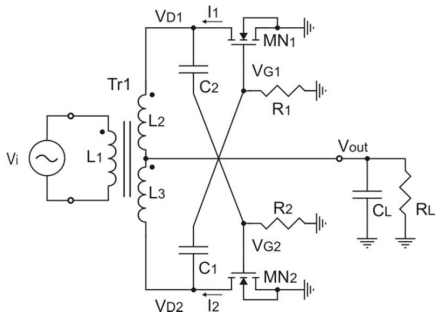

Fig. 1. The basic configuration of rectifier.

The transistors MN_1 and MN_2 act as switches controlled by two out of phase AC voltages V_{G1} and V_{G2}. As a result, MN_1 and MN_2 are alternately switched on and off. Due to the fact that the substrates and sources of these transistors are connected to ground, in contrast to the known rectifier configurations [7, 9, 10, 13], there is no reverse current flow through the p-n junction formed between the source and body. Because both transistors can be completely switched off, power losses can be highly reduced. Another factor that helps to increase the efficiency, is twice reduced effective resistance R_{eff} of the switches in the path of current flow. In all the full-wave rectifiers used so far in CMOS technology [7–14], there were always two switches connected in series, resulting in $R_{eff} = 2 \cdot R_{ON}$, as illustrated in Fig. 2a. In the proposed rectifier solution, shown in Fig. 2b, the resistance is reduced to $R_{eff} = R_{ON}$.

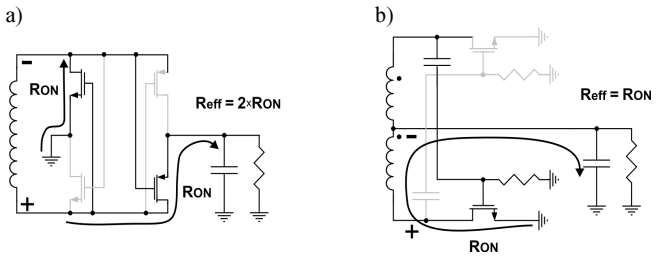

Fig. 2. Comparison of the effective resistance in the current path in the rectifier: a) the bridge; b) the rectifier presented in Fig. 1.

Typical time-domain waveforms of the voltages V_{G1} and V_{G2} controlling the switches MN_1 and MN_2, and the resulting currents flowing through the switches are shown in Fig. 3. Note

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that, due to the circuit simplicity, the controlling voltages V_{G1} and V_{G2} are not precisely shaped, and as a result a small flow of the reverse leakage current can be observed. Although this phenomenon limits the upper limit of achievable power efficiency, it still remains sufficiently high. In addition, the rectifier parameters can be optimized so that a small deterioration of efficiency is assured. This issue will be discussed in the next section.

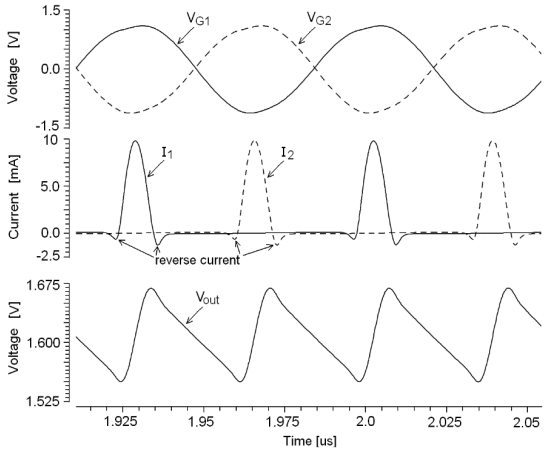

Fig. 3. Typical waveforms of the gate voltages and drain currents of the MOS switches in the rectifier shown in Fig. 1.

2.2. Power efficiency optimization

The maximum power efficiency of the rectifier can be obtained only when the transistors MN_1 and MN_2 are switched on when the drain voltage is lower than the source voltage. The voltage waveforms at the MOS gates, obtained from a Cadence Spectre simulator, are shown in Fig. 4.

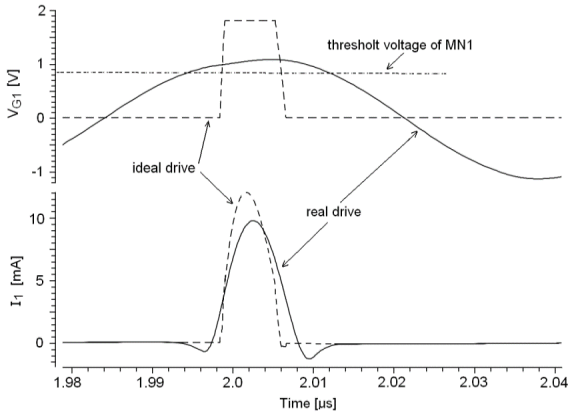

Fig. 4. The voltage controlling the gate of MOS switch in the rectifier shown in Fig. 1.

The dashed line represents the ideal, desirable waveform of the voltage V_{G1} controlling the gate of the transistor MN_1. This waveform was achieved by using an ideal voltage comparator generating a high voltage level at the gate of MN_1 only when $V_{D1} < 0$. In the rectifier presented in Fig. 1, the gate of MN_1 is controlled by a voltage generated by a simple high-pass filter

(R_1, C_1) and therefore the switching-on time of transistor MN_1 is longer then the optimal one, which results in the reverse current flow, illustrated in Fig. 4.

The consequence of that flow is a degradation of the power and voltage efficiencies. The reduction of the switching-on time can be achieved by proper lowering of the V_{G1} amplitude. On the other hand, the optimal amplitude of V_{G1} must also provide a relatively small R_{ON} of the transistor MN_1. Based on the computer simulations, it was found that for achieving the maximum power efficiency the waveform V_{G1} amplitude should be greater by at most 0.15–0.2 V than the threshold voltage of the transistor MN_1. The optimal value of the amplitude can be obtained by proper selection of the capacitance C_1, which forms a voltage divider together with the input capacitance of the transistor MN_1. Taking into account the condition for the optimal amplitude, which is:

$$V_{TH1} < V_{G1} < V_{TH1} + 0.2\text{V}, \tag{1}$$

where V_{TH1} denotes the threshold voltage of MN_1, the required capacitance C_1 can be calculated using:

$$\frac{C_{G1}}{V_{out}/V_{TH1} - 1} < C_1 < \frac{C_{G1}}{V_{out}/(V_{TH1} + 0.2\text{V}) - 1} \quad \text{for} \quad V_{out} > V_{TH1} + 0.2\text{V}, \tag{2a}$$

$$C_{G1} << C_1 \quad \text{for} \quad V_{out} < V_{TH1} + 0.2\text{V}, \tag{2b}$$

where C_{G1} is the input capacitance of the transistor MN_1. An analogous equation can also be derived for C_2. To validate correctness of the (2a) and (2b) formulas, the C_1 capacitances were calculated for several, typical values of the output voltage V_{out} = 0.9, 1.8, 2.7, 3.3 V, assuming that the rectifier was designed using AMS 0.35 µm CMOS technology. In addition, it is assumed that thick oxide MOS transistors were used as the switches. The transistors have the following parameters: the threshold voltage V_{TH} = 0.85 V, the channel width W = 500 µm, and the length L = 0.5 µm. The data in Table 1 show that the expressions (2a) and (2b) enable calculating the optimal values with a good approximation.

Table 1. The optimal values of C_1 for selected rectified voltages[1)].

V_{out}	C_1 from computer simulation	C_1 from (2)	PCE[2)]	VCE[3)]
0.9 V	6 pF	C_1 >> 0.67 pF	89%	87%
1.8 V	0.75 pF	0.6 pF < C_1 < 0.94 pF	90.8%	89%
2.7 V	0.4 pF	0.3 pF < C_1 < 0.42 pF	90.9%	88.9%
3.3 V	0.3 pF	0.23 pF < C_1 < 0.31 pF	90.7%	88.2%

[1)] At the frequency = 13.6 MHz, V_{TH1} = 0.85V, C_{G1} = 0.67 pF, R_1 = 100 kΩ, R_L = 1 kΩ, C_L = 400 pF.
[2)] Power Conversion Efficiency = P_{out}/P_{in}.
[3)] Voltage Conversion Efficiency = $2V_{out}/V_{in,pp}$.

In Fig. 5 the power efficiency of the rectifier designed in 0.35 µm CMOS technology is plotted as a function of the input voltage V_{in} for several values of the capacitance C_1 (C_2). Also, in the figure the power efficiency is plotted for a rectifier with pn diodes inserted instead of MOS transistors. The efficiency of the rectifier with the diodes is below 75% over the whole range of V_{in}, whereas for the rectifier with MOS transistors, ideally controlled, the efficiency is greater than 90% if only the V_{in} amplitude is greater than the threshold voltage of the transistors. For amplitudes below the threshold voltage of the transistors, the efficiency rapidly decreases because the transistors work in the subthreshold region of operation and its on-resistance increases considerably. The power efficiency of the rectifier shown in Fig. 1 can be made as high as 80–90% for a limited range of V_{in} amplitudes by proper selection of the capacitance C_1 (C_2). It should be noted that even with improper selection of C_1 (C_2) the efficiency is always greater than 75% over a wide range of V_{in}.

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The voltage efficiency of the rectifier is related to its power efficiency. However, it is less dependent on the capacitances C_1 and C_2. As shown in Fig. 6, even with improperly selected C_1 (C_2) the voltage efficiency is always greater than 80%. The frequency domain simulation results, presented in Fig. 7, show that the proposed rectifier has a very wide bandwidth. The rectifier designed in 0.35 µm CMOS technology can operate up to 1 GHz without a noticeable loss of performance.

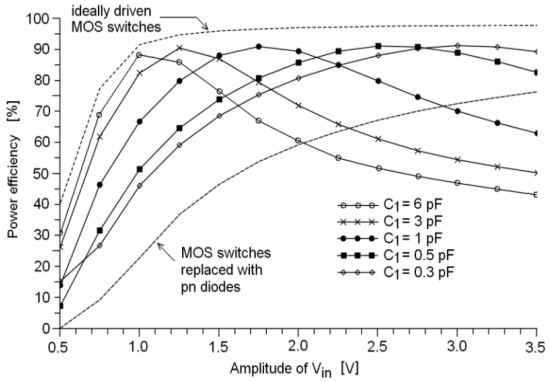

Fig. 5. The simulated power efficiency of the rectifier presented in Fig. 1 designed in 0.35 µm CMOS technology.

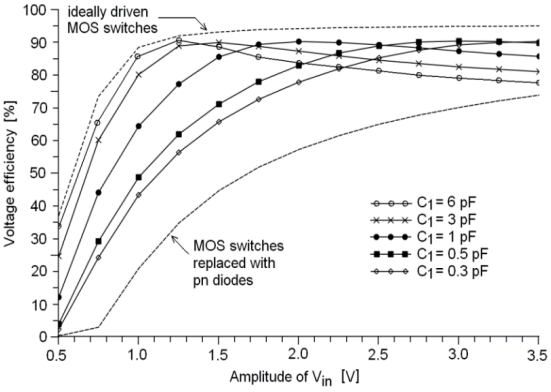

Fig. 6. The simulated voltage efficiency of the rectifier presented in Fig. 1 designed in 0.35 µm CMOS technology.

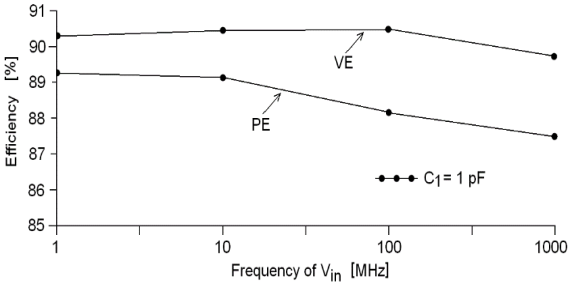

Fig. 7. The simulated power (PE) and voltage (VE) efficiencies of the rectifier versus frequency; $C_1 = 1$ pF, $V_{in} = 2$ V.

3. Rectifier measurements and comparison

Due to the lack of possibility to manufacture an integrated CMOS circuit containing the proposed rectifier, a prototype circuit assembled from discrete components was designed and used for practical verification of its operation. The circuit was assembled from: MOS transistors FDV301N (V_{TH} = 0.85 V, $C_{GS} \approx$ 30 pF), three sets of coupling capacitors $C_1 = C_2$ = 150, 68, 33 pF, and $R_1 = R_2$ = 75 kΩ. The measurements were accomplished using a transformer containing a ferrite pot core, part number 1408, magnetic material type C with the maximum usable frequency < 8 MHz. The primary (L_1 in Fig. 1) and secondary ($L_2 + L_3$ in Fig. 1) windings consist of 2 and 2 × 4 turns made with Litz wire 8 × 0.1 mm. The secondary winding of the transformer forms a resonant circuit together with the input capacitance $C_{in} = (C_1 C_{G1})/(2(C_1 + C_{G1}))$ of the rectifier. The resonant frequency depends on the employed coupling capacitances (C_1 and C_2), and is in the range of 7.5–8.5 MHz. Because measuring the power efficiency of the rectifier is a real challenge due to its nonlinearity (note the short pulses of the drain currents in Fig. 4), a special setup was developed. In the beginning, the power efficiency of the transformer was measured at exactly the same resonant frequencies as those for the complete rectifier, using the measurement setup shown in Fig. 8a. Firstly, the input resistance R_{in} of the transformer was matched to the output resistance R_g of the generator at a proper resonant frequency by selection of R^* and C^*. Finally, by measuring the voltage amplitudes at outputs of the generator V_g and the transformer V_o, the power efficiency of the transformer was determined as $\eta_T = (V_o/V_g)^2(R_g/R^*)$. In the aforementioned frequency range, the achieved efficiency of the transformer was 73–77%. In the next step, the efficiency of the complete rectifier was measured using the setup shown in Fig. 8b.

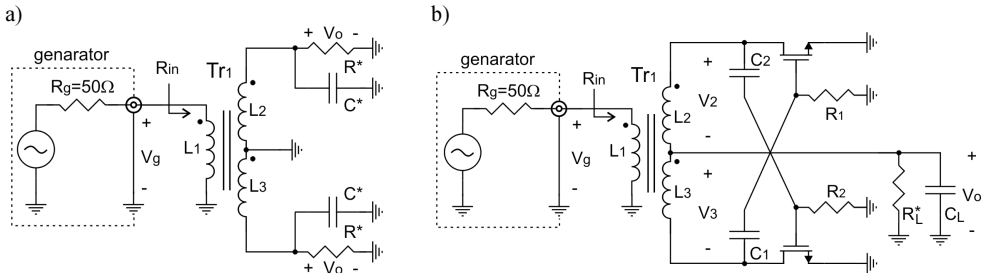

Fig. 8. The setups used for measuring the power efficiency of: a) the transformer; b) the complete rectifier.

During the measurements, the input resistance R_{in} of the complete rectifier was matched to the output resistance of the generator, by proper tuning of the load resistance R_L^*, whenever the input voltage V_g amplitude was changed. Because of the fact that the transformer formed a resonant circuit, the short pulses generated by the rectifier were converted onto the sinusoidal shape, and therefore the power delivered to the rectifier could be calculated as $V_g^2/(2R_g)$. Under these conditions the rectifier power efficiency was evaluated as $\eta_{Rect} = (V_o/V_g)^2(R_g/R^*)(2/\eta_T)$. The rectifier voltage efficiency was determined as $V_o/V_{2(3)}$, where $V_{2(3)}$ represents the voltage amplitude on the secondary winding L_2 (L_3).

The measurement results of the power and voltage efficiencies are presented in Figs. 9 and 10. The plots show that the prototype rectifier has the power efficiency reaching 82% and the voltage efficiency over 92%. Depending on the amplitude of the processed voltage, the rectifier can be optimized by proper selection of the capacitances C_1 and C_2.

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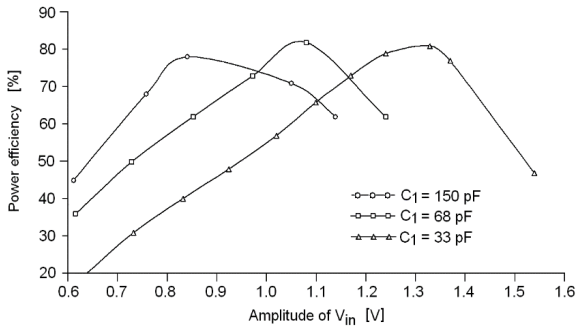

Fig. 9. The measured power efficiency of the rectifier shown in Fig. 8b.

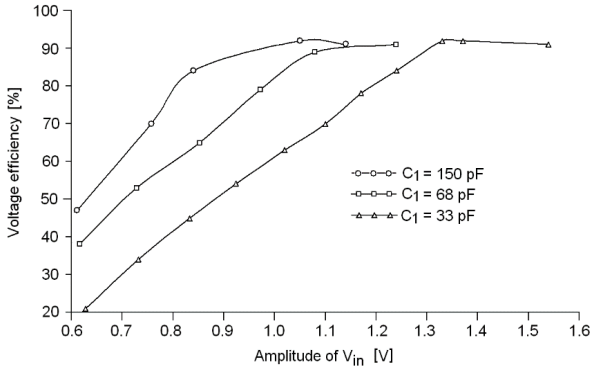

Fig. 10. The measured voltage efficiency of the rectifier shown in Fig. 8b.

It should be noted that the presented measurement results serve only as an illustration proving correct operation of the proposed rectifier. Due to large internal capacitances of the discrete MOS transistors (over 30 pF) and the frequency limitation of the applied ferrite core it was not possible to test operation of the rectifier at higher frequencies. The simulations performed for AMS 0.35 µm CMOS technology show that the rectifier can operate up to 1 GHz without a noticeable loss of performance. For this reason, the comparisons presented in Table 2 refer to the results of simulation of the proposed rectifier. Otherwise, comparing the rectifiers made in the form of integrated circuits with those made from discrete components would be unreliable and unfair.

Looking at Table 2, it is worth to note that the proposed rectifier can work with a reduced input voltage and in such circumstances is characterized by relatively big voltage and power efficiencies. Additionally, the rectifier has a much wider bandwidth.

Table 2. Comparison of characteristics of the most advanced rectifiers.

Parameter	[8]	[11]	[12]	[13]	[14]	This work (simulation)
Frequency [MHz]	0.2–1.5	0.125–1	13.56	13.56	13.56	1–1000
Process CMOS	0.35 µm	0.5 µm	0.35 µm	0.5 µm	0.18 µm	0.35 µm
$\|V_{THP}\|/V_{THN}$ [V]	0.82/0.69	N/A	0.73/0.55	0.92/0.78	0.49/0.42	–/0.85
Input AC amplitude [V]	2.4	5	3.5	3.8	1.5	1.0–3.5
Output DC voltage [V]	2.28	4.36	3.2	3.12	1.33	0.9–3.3
R_L [kΩ]	2	1	1.8	0.1	1	1
Max. VCE [%]	95	87	92	82	89	89
Max. PCE [%]	87	84.8	87	80.2	81.9	91

4. Conclusions

A new configuration of rectifier suiting CMOS technology is presented. The most important advantages of the proposed circuit are: its compactness that enables cheap production, low-voltage operation, wide bandwidth and power efficiency. The results of simulations and measurements of chosen circuits confirmed their correct operation and advantages. The performed simulations showed that a rectifier designed in 0.35 µm CMOS technology was capable to operate with signals of frequencies up to 1 GHz, and voltages as low as 0.7 V. To fully verify the parameters of the proposed rectifier, it is planned to design and produce a prototype integrated circuit in 0.35 µm or 0.18 µm CMOS technology.

Acknowledgements

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