Zbigniew CZAJA, Bogdan BARTOSIŃSKI

Gdansk University of Technology, Faculty of Electronics, Telecommunications and Informatics

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A testing method of analog parts of mixed-signal electronic systems equipped with the IEEE1149.1 test bus

Abstract. *A new solution of the JTAG BIST for testing analog circuits in mixed-signal electronic microsystems controlled by microcontrollers and equipped with the IEEE1149.1 bus is presented. It is based on a new fault diagnosis method in which an analog circuit is stimulated by a buffered signal from the TMS line, and the time response of the circuit to this signal is sampled by the ADC equipped with the JTAG. The method can be used for fault detection and single soft fault localization in an analog tested circuit (A testing method of analog parts of mixed-signal electronic systems equipped with the IEEE1149.1 test bus).*

Streszczenie. *Przedstawiono nowe rozwiązanie testera JTAG BIST przeznaczonego do testowania torów analogowych w mieszanych sygnałowo mikrosystemach elektronicznych sterowanych mikrokontrolerami i wyposażonych w magistralę testującą IEEE1149.1 (JTAG). Bazuje ona na nowej metodzie diagnostycznej, w której tor analogowy pobudzany jest buforowanym sygnałem z linii TMS, a odpowiedź czasowa tego toru na ten sygnał jest próbkowana przez przetwornik A/C wyposażony w interfejs JTAG. Metoda ta pozwala na detekcję i lokalizację pojedynczych uszkodzeń parametrycznych w analogowym układzie badanym* ***(Metoda testowania części analogowych analogowo-cyfrowych systemów elektronicznych wyposażonych w magistralę testującą IEEE1149.1).***

Keywords: IEEE1149.1 test bus, fault diagnosis, microcontrollers, analog circuits.
Słowa kluczowe: magistrala IEEE1149.1, diagnostyka uszkodzeń, mikrokontrolery, układy analogowe.

Introduction

The IEEE 1149.1 standard (JTAG) [1] is recently a commonly used standard for testing digital circuits, packets and systems. That is the reason of implementing the JTAG test bus in more and more nowadays manufactured medium- and large-scale integrated digital circuit. The test bus versatility makes it useful not only for testing, but also for programming and debugging e.g. FPGA and CPLD circuits, as well as microcontrollers. Thus, it can be stated that the JTAG is a universal, commonly used tool, yet employed exclusively in digital applications. So, it cannot fully take its advantages when used for testing mixed-signal systems, i.e. systems containing not only the digital circuits but also the analog ones, e.g. sensors, circuits for conditioning analog signals (amplifiers, anti-aliasing filters), etc.

Taking the above into account, the authors in their papers [2,3] have proposed extending the available JTAG infrastructure, that enables testing digital components of mixed-signal systems, with a new functionality that enables measuring analog components of such systems. As a result, a BIST (Built-In Self Tester) was developed. The tester, called JTAG BIST, consists of a BCT8244A buffer [4] and a 12-bit ADC (Analog-to-Digital Converter) SCANSTA476 [5]. Both devices are controlled by the JTAG interface. The BCT8244A is used to generate a square pulse stimulating the tested analog circuit, whereas the ADC – to measure the parameters of this circuit's time response to this stimulation, e.g. as in [6,7]. Such an approach enables detection of faults as well as localization of a single soft fault of passive components of the tested analog circuit, e.g. one-section [2] or multi-section [3] filters.

It is worth mentioning that the specialized BISTs for analog circuits, e.g. the oscillation OBISTs [8], histogram HBISTs [9], testers for fully differential circuits [10], TBISTs [11], and $\Sigma\Delta$ type testers [12] have to be extended with additional circuits enabling them to communicate with the testing system. The JTAG BISTs are free from that shortcoming, since they are already equipped with the JTAG communication interface.

Nevertheless, the developed JTAG BIST [2,3] introduces hardware redundancy to the system. To reduce it, a new approach consisting in a different way of generating the stimulation pulse is proposed. The BCT8244A circuit, that required its own JTAG bus, was removed from the tester. In the new solution the analog circuit under test (ACUT) is stimulated with a buffered TMS signal. Thus, the TMS signal used for selecting the operation mode of the SCANSTA476 circuit, is simultaneously used to generate the stimulating pulse (Fig. 1). Such an approach imposed a special way of generating the stimulation and, since the TMS signal is strictly determined [5], made it necessary to develop a new fault diagnosis method.

The structure of JTAG BIST

The concept of using a new JTAG BIST is shown in Fig. 1. The tester consists exclusively of an ADC SCANSTA476 and a non-reversing buffer separating the TMS line from the analog part and ensuring appropriate values of the stimulating signal parameters. From the point of view of the testing system that controls the JTAG bus the tester can be an integral part of the whole tested system.

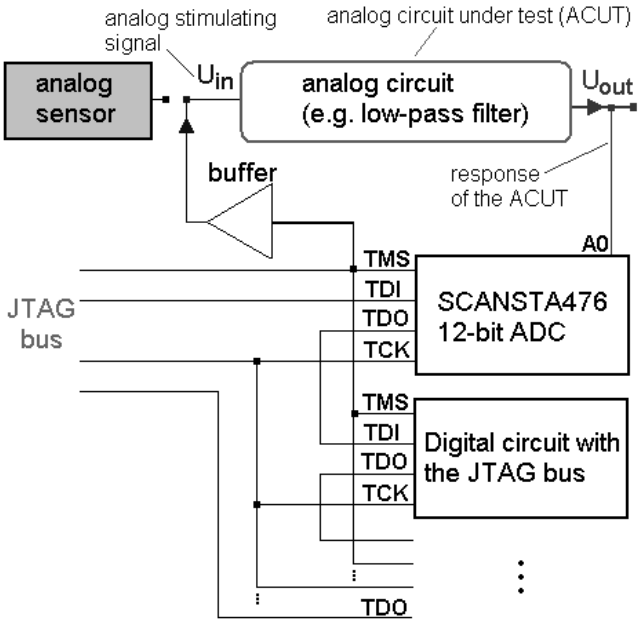

Fig.1. The concept of using the JTAG BIST for testing analog circuits in mixed-signal electronic microsystems

An application of JTAG BIST

A new solution of the JTAG BIST and a fault diagnosis method have been implemented in an example system built of an ATmega32 microcontroller [13] (Fig. 2) controlling – with the JTAG bus emulated on its port lines – the SCANSTA476 circuit, and a non-reversing buffer (Fig. 3) consisting of two IRF7105PBF circuits [14]. The microcontroller is controlled with the UART interface connected via an FT232 circuit to the USB port of a PC computer.

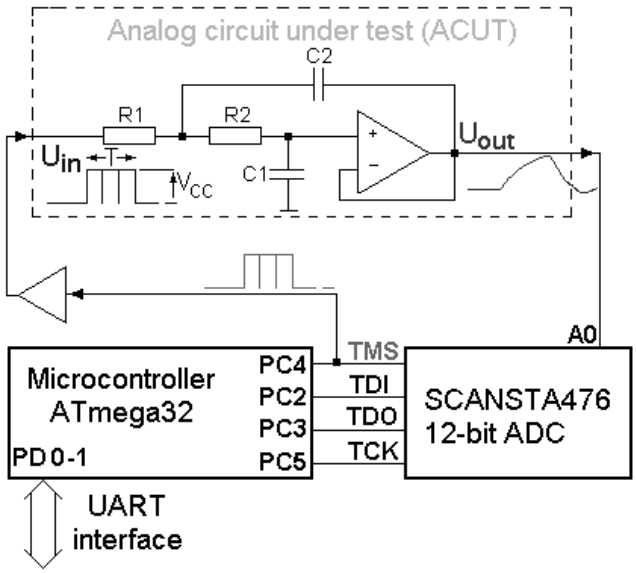

Fig.2. The JTAG BIST working in the test mode of an analog circuit - a low pass second order Sallen-Key filter with the Butherworth's characteristic, where: R1 = R2 = 10 kΩ, C1 = 58.56 nF, C2 = 68.6 nF

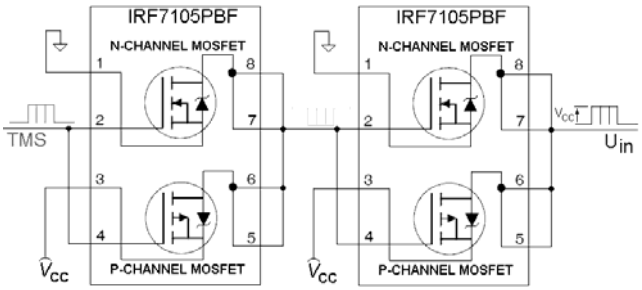

Fig.3. A buffer built of two IRF7105PBF circuits

Controlling the SCANSTA476 circuit consists of selecting an analog input (controlling the analog multiplexer) and triggering the voltage measurement and the readout of the AD conversion result, when the TMS signal is simultaneously used for generation of pulses stimulating the ACUT. Everything is synchronized by Timer 1 of the microcontroller.

The measurement procedure

The way of stimulation of the ACUT and measuring the voltage sample of its time response are imposed *a priori* of the waveform of Data Shift command (A/D Sample) [5] implemented in the *conversionADC* function (Fig. 6). During execution of this command two square pulses appear in the TMS line. The first pulse causes switching from the RTI to SEL DR state, whereas the second one – from the SHIFT DR to UPD DR state. The change of states and data transmission are clocked by the TCK signal; more accurately – by its slopes [1]. Thus, the duration of the clock pulse (and also the TMS signal) may be arbitrary. The only limitation is the minimum value of the clock pulse duration, equal to 25 ns [5].

It is thus possible to increase e.g. the duration of the first pulse in the TMS line to the value required by the fault diagnosis method treating it as the main square pulse stimulating the ACUT, after which sampling the time response occurs, as shown in Fig. 4. The duration of AD (Analog-to-Digital) conversion and read-out of its result from the ADC, as well as the length of the second pulse in the TMS line, are determined by the values of time parameters of the ADC and the computing power of the microcontroller (more precisely: its instruction execution speed). Both times should be as short as possible; therefore, most of the *conversionADC* function code is written in the assembler.

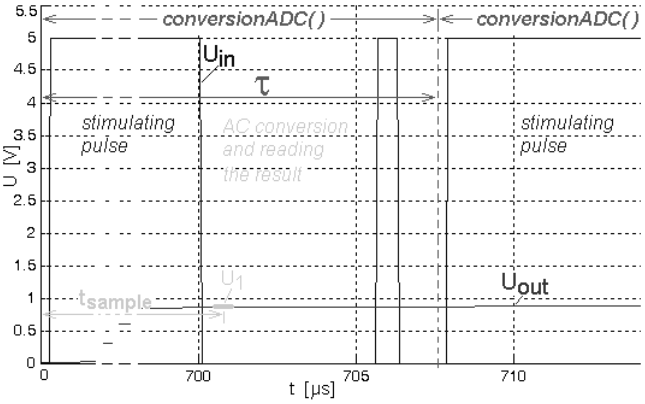

Fig.4. A fragment of the timing of the measurement procedure - the timing of the *conversionADC* function

So, a single measurement of the k-th voltage U_k (where: k = 1, 2, .., K and K – the number of voltage samples) consists of stimulation of the ACUT with a square pulse and – immediately following – sampling the time response of this ACUT to this stimulation (Fig. 4).

To make the fault diagnosis method effective, the number K of voltage samples – assuming the occurrence of single soft faults in the ACUT – should be at least 2 [6]. In order to obtain an optimal localization resolution, at the same time keeping a moderate size of the fault dictionary, K = 3 was chosen.

In this case, the proper stimulating pulse is composed of K basic pulses (Fig. 5).

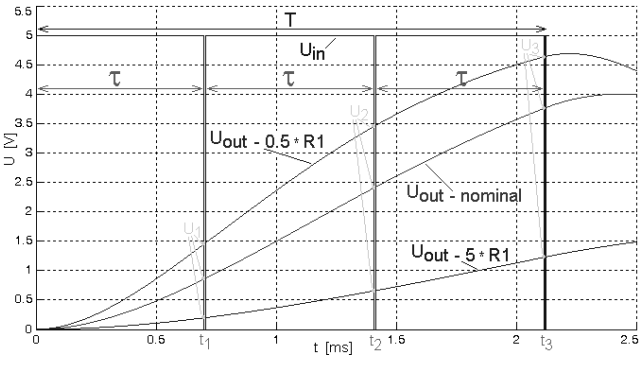

Fig.5. The timing of the testing procedure of an analog circuit

The duration of basic pulses (700 μs) significantly exceeds the intervals between those pulses (about 7 μs) (Fig. 4), and we test the low-pass filter (Fig. 2), thus we can assume for our analyze that the ACUT is stimulated with a single square pulse with the duration $T = K \cdot \tau$, where τ – the

duration of *conversionADC* function, and the response to the stimulation during that pulse is sampled at equal intervals $t_k = k \cdot t_{sample}$, (Fig. 5), t_{sample} – the moment of voltage sampling that is measured in relation to the beginning of *conversionADC* function. Thus, the measurement procedure is executed by K times calling the *conversionADC* function.

As a result, on the completion of the measurement procedure a measurement point is obtained. Its coordinates are the voltage sample values: U_1, U_2, U_3 of the ACUT time response, measured at the moments: t_1, t_2 and t_3, respectively (Fig. 5).

The pulse duration determined with the susceptibility analysis method [6,7] for the ACUT (Fig. 2) is equal to T = 2.1 ms, i.e. τ = 700 μs.

The *conversionADC* function

The flowchart of the *conversionADC* function algorithm is presented in Fig. 6. The algorithm is executed in the main program (the main function) and in the interrupt service (Timer 1 Compare Match Interrupt Service).

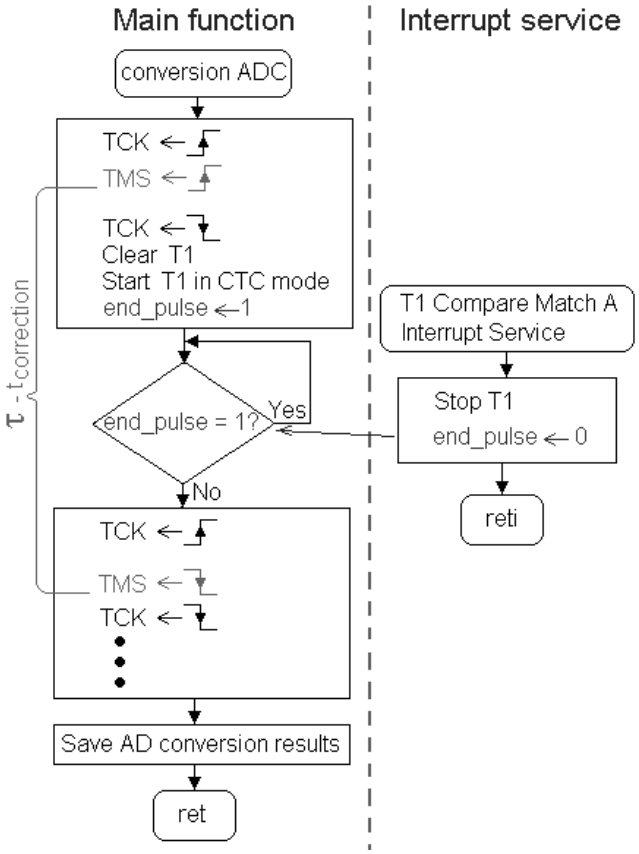

Fig.6. The flowchart of the *conversionADC* function algorithm

Before calling K times the *conversionADC* function, the JTAG BIST is configured. First, a conversion channel (e.g. channel 0 – with the MUSEL 0 command) is chosen. Next, the value corresponding with the time τ decreased by a correction $t_{correction}$ regarding the AD conversion and the read-out of the result from the SCANSTA476 circuit, is written into the OCR1A compare register of Timer 1.

The *conversionADC* function performs step by step the Data Shift waveform (A/D Sample) [5]. The waveform consists of 22 pulses in the TCK line and two pulses synchronized by this waveform – in the TMS line. The TDO line is used for reading out – bit by bit - the conversion result from the ADC. To generate particular signals emulated at the C port of the microcontroller, the assembler commands are used. They are defined as macros in the following way:

```
#define set_TCK_S asm volatile("sbi 0x15, 5" ::)
#define clr_TCK_S asm volatile("cbi 0x15, 5" ::)
#define set_TMS_S asm volatile("sbi 0x15, 4" ::)
#define clr_TMS_S asm volatile("cbi 0x15, 4" ::)
#define set_TDI_S asm volatile("sbi 0x15, 2" ::)
#define clr_TDI_S asm volatile("cbi 0x15, 2" ::)
```

Listing 1. The declarations of macros used for pulse generation in the lines of the JTAG bus

The macros used for reading out bits occurring in the TDO line are defined in a similar way:

```
#define read_TDO_S_Hi asm volatile("sbic 0x13, 3"
"\n\t" "or r19,r18" "\n\t" "lsr r18" "\n\t" ::)
#define read_TDO_S_Lo asm volatile("sbic 0x13, 3"
"\n\t" "or r20,r18" "\n\t" "lsr r18" "\n\t" ::)
```

Listing 2. The declarations of macros used for reading bits from the TDO line of the JTAG bus

The 12-bit AD conversion result from the ADC is stored in two 8-bit register variables placed at r19 and r20 registers. The r18 register contains a mask determining the current position of a bit being read out from the ADC. 0x15 and 0x13 are the addresses of PORTC and PINC registers, respectively.

As shown in Fig. 6, the first pulse in the TMS line (the main pulse stimulating the ACUT) is lengthened only after the falling slope of the first TCK clock signal is reached. It is accomplished by starting Timer1 in the CTC mode and waiting till the contents of both TCNT1 and OCR1A registers become equal. This equaling generates an interrupt. In its service, Timer1 is stopped and the *end_pulse* flag is cleared. That flag is used for synchronizing execution of the main function and the interrupt service codes. Then, during the second clock pulse in the TCK line, the TMS line is cleared (set a low level), what completes generation of the stimulating pulse.

The remaining clock pulses clock both AD conversion and read-out of 12-bit result from the SCANSTA476 circuit. Eventually, the function places the conversion result in the 16-bit variable *result*.

The fault dictionary

The coordinates of the K–dimension (three-dimension) measurement space, in which the family of localization curves is placed (a graphic representation of the fault dictionary of the ACUT presented in Fig. 2), are the voltage sample values of the ACUT time response: U_1, U_2, U_3.

As shown in Fig. 7, the families of the ACUT time responses – generated by the way of simulation for changes of values of particular components (the occurrence of single soft faults was assumed, defined as changes of particular component values from 0.1 to 10 of their nominal values) – do not overlap. Thus, it is possible to distinguish different waveforms and attach them to particular components, i.e. to perform the fault localization.

The conversion of time response families (Fig. 7) onto the family of localization curves, i.e. generation of the fault dictionary, consists in sampling the time response at the moments: t_1, t_2 and t_3, and placing the set of voltage samples in the measurement space with coordinates: U_1, U_2, U_3. Fig. 8 shows the family of localization curves obtained in that way for the ACUT presented in Fig. 2.

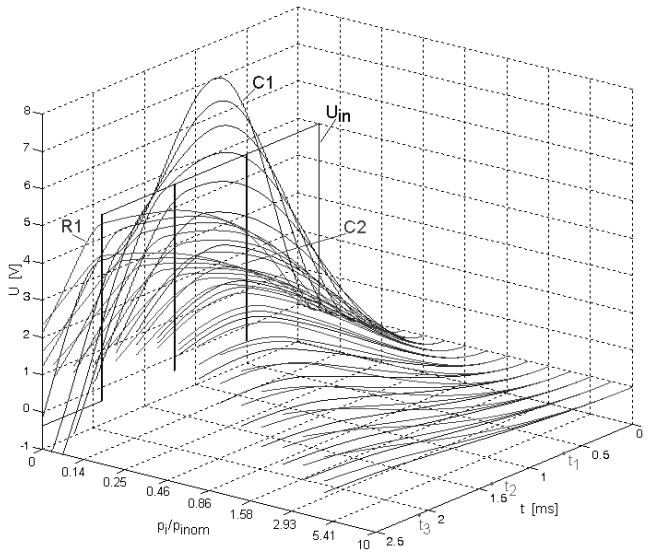

Fig.7 Families of time responses of the ACUT (Fig. 2) for the changes of values of its individual components from 0.1 to 10 of their nominal values

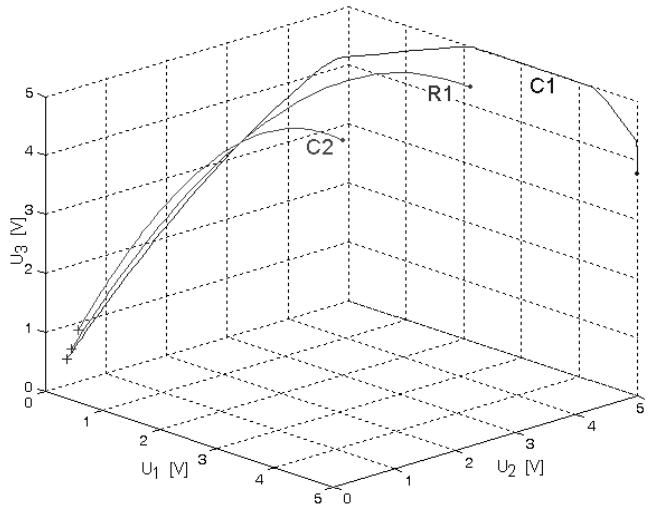

Fig.8. A family of localization curves of the ACUT (Fig. 2)

As it is seen, the localization curves generated according to the rules imposed by the fault diagnosis method (more exactly: by the strictly determined TMS waveform and – related to it – way of sampling the time response to this stimulation [5]) do not mutually overlap, thus making possible the fault detection as well as localization of single soft faults of ACUT passive components.

Similarly to other methods of that class, the fault detection and fault localization consist in placing a measurement point in the measurement space (Fig. 8) and then checking its location in relation to the family of localization curves [6,7].

Conclusions

A new solution of the JTAG BIST proposed in the paper required overcoming new scientific difficulties stemming from the JTAG bus specificity. The developed JTAG BIST consists only of an SCANSTA476 ADC and a non-reversing buffer that separates the TMS line from the analog part and ensures proper parameter values of the signal stimulating it. Thus, to generate the pulse stimulating an ACUT being a part of a mixed-signal electronic system equipped with the JTAG bus, a buffered TMS signal was used for choosing the operation mode of the SCANSTA476 converter.

Owing to our proposal, consisting in adding a JTAG BIST to the existing infrastructure used for testing digital systems and based on the IEEE 1149.1 testing bus (JTAG), the designers of mixed-signal electronic systems obtained the possibility of testing analog parts of these systems, i.e. the possibility of testing not only the digital systems, but also the analog ones. This functionality is particularly useful in high-reliable systems that require continuous monitoring.

Moreover, it should be remembered that monitoring such systems can reduce the cost of their servicing, what in turn reduces their maintenance costs and also lengthens the lifetime.

***Authors**: dr hab. inż. Zbigniew Czaja, dr inż. Bogdan Bartosiński, Politechnika Gdańska, Wydział Elektroniki, Telekomunikacji i Informatyki, Katedra Metrologii i Optoelektroniki, ul. G. Narutowicza 11/12, 80-233 Gdańsk, E-mail: zbczaja@pg.gda.pl; bbart@eti.pg.gda.pl*

REFERENCES

[1] Standard Test Access Port and Boundary-Scan Architeture, *IEEE Std 1149. ™-2001*, (2008)
[2] Czaja Z., Bartosiński B., Using an IEEE1149.1 test bus for fault diagnosis of analog parts of electronic embedded systems, *Proc. of 19th IMEKO TC4 Symposium, Barcelona, Spain*, (2013), 6-11
[3] Czaja Z., Bartosiński B., Diagnostyka analogowych filtrów wielosekcyjnych oparta na magistrali testującej IEEE1149.1, *Pomiary, Automatyka, Kontrola*, 60 (2014), 745-748
[4] Texas Instruments Incorporated, SN54BCT8244A, SN74BCT8244A scan test devices with octal buffers, PDF file available from: www.ti.com, (1996)
[5] Texas Instruments Incorporated, , SCANSTA476 Eight Input IEEE 1149.1 Analog Voltage Monitor, PDF file available from: www.ti.com, (2005)
[6] Czaja Z., A diagnosis method of analog parts of mixed-signal systems controlled by microcontrollers, *Measurement*, 40 (2007), 158-170
[7] Czaja Z., A method of fault diagnosis of analog parts of electronic embedded systems with tolerances, *Measurement*, 42 (2009), 903-915
[8] Toczek W., An oscillation-based built-in test scheme with AGC loop, *Measurement*, 41 (2008), 160-168
[9] Ren J., Ye H., A Novel Linear Histogram BIST for ADC, *Ninth International Conference on Solid-State and Integrated-Circuit Technology*, *Beijing*, (2008), 2099-2102
[10] Toczek W., Self-testing of fully differential multistage circuits using common-mode excitation, *Microelectronics Reliability*, 48 (2008), 1890-1899
[11] Peralta J., Peretti G., Romero E., A New Performance Characterization of Transient Analysis Method, *International Journal of Electronics, Communications and Computer Engineering*, 1 (2009), 12-19
[12] Toczek W., Analog fault signature based on sigma-delta modulation and oscillation test methodology, *Metrology and Measurement Systems*, 9 (2004), 363-375
[13] Atmel Corporation, 8-bit bit AVR microcontroller with 32KBytes In-System Programmable Flash, ATmega32, ATmega32L, PDF file available from: www.atmel.com, (2011)
[14] International Rectifier, IRF7105 HEXFET Power MOSFET, PDF file available from: www.irf.com, (2003)