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PROGRAMMABLE INPUT MODE INSTRUMENTATION AMPLIFIER USING MULTIPLE OUTPUT CURRENT CONVEYORS

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Abstract

In this paper a programmable input mode *instrumentation amplifier* (IA) utilising second generation, multiple output current conveyors and transmission gates is presented. Its main advantage is the ability to choose a voltage or current mode of inputs by setting the voltage of two configuration nodes. The presented IA is prepared as an integrated circuit block to be used alone or as a sub-block in a microcontroller or in a *field programmable gate array* (FPGA), which shall condition analogue signals to be next converted by an *analogue-to-digital converter* (ADC). IA is designed in AMS 0.35 μm CMOS technology and the power supply is 3.3 V; the power consumption is approximately 9.1 mW. A linear input range in the voltage mode reaches ± 1.68 V or ± 250 μA in current mode. A passband of the IA is above 11 MHz. The amplifier works in class A, so its current supply is almost constant and does not cause noise disturbing nearby working precision analogue circuits.

Keywords: instrumentation amplifier, current conveyor, programmable analogue circuit.

1. Introduction

Instrumentation amplifiers (IA) are usually employed as input stages in a variety of applications. Their main purpose is to amplify desired differential signals while simultaneously suppressing the unwanted common mode ones. The application area covers sensor signal amplification, medical instrumentation, data acquisition and many others [1–5]. Most IAs work in the voltage mode (*i.e.* input and output signals are voltage ones) and are built using *operational amplifiers* (OA) and resistor networks [3–5]. New integrated circuit manufacturing technologies enable to use smaller power supply voltages, which resulted in turning to signal processing in the form of current instead of voltage and creation of new active blocks called current conveyors [6–9]. As a result many IAs are built of current conveyors and IAs working in all four possible modes are also in common use [1–2]. In this paper a new concept of *multiple output second order current conveyor* (MOCCII) is presented (Section 2). It uses, as the output stage, a current amplifier reported in [11]. Then MOCCII is used as the main active block of a programmable input mode instrumentation amplifier (Sections 3 and 4). There are numerous IAs with a programmable gain and offset known in the literature [3–5] but there is a lack of a programmable input mode IA. The presented, programmable input mode IA is designed as an integrated circuit block to be used alone or as a sub-block of a microcontroller or FPGA, which can condition analogue signals to be next converted by a system *analogue to digital converter* (ADC).

2. Multiple output current conveyor circuit

Since their introduction [6], current conveyors have been widely used in analogue signal processing applications. To date, many variations of current conveyors have been presented,

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both with positive and negative current gains, their generations being marked from I to III, and also having multiple outputs [7–10]. In this paper, a *multiple output second-generation current conveyor* (MOCCII) is presented and used as an active block of IA. It has inputs Y and X and 3 outputs: Z_P, Z_{M1} and Z_{M2}. Output Z_P is the positive one while Z_{M1} and Z_{M2} are two independent negative outputs. The MOCCII graphical symbol and its terminals' voltages and currents are defined in Fig. 1. A matrix equation describing ideal electrical properties of an MOCCII element is given by:

$$\begin{bmatrix} i_Y \\ v_X \\ i_{ZP} \\ i_{ZM1} \\ i_{ZM2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ i_{ZP} \\ i_{ZM1} \\ i_{ZM2} \end{bmatrix}. \tag{1}$$

From (1) it is apparent that an MOCCII element is equivalent to a second-generation current conveyor (CCII) having 2 negative and 1 positive independent outputs. The main advantage of the below shown structure over the previously presented one [7–9] is simultaneous providing 3 independent outputs, each of them exhibiting similar and good frequency responses. Such properties are usually impossible to obtain using the current mirror cascading technique for generating the negative output.

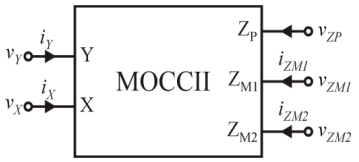

Fig. 1. A graphic symbol of the proposed *multiple output second-generation current conveyor* (MOCCII) block.

2.1. Architecture of MOCCII

The architecture of proposed MOCCII is presented in Fig. 2. It consists of an *operational amplifier* (OA) and – as the output stage – a current amplifier described in [11]. Due to the negative feedback loop in the signal path (which starts at X terminal and then passes through OA and an inverting MN1 device), voltages at Y and X terminals should be of the same value. In a real circuit the equality of voltages at Y and X terminals depends mainly on mismatches of devices in the input stage of OA, and thus this sub-circuit should be designed carefully using relatively large devices and a high overdrive voltage [12]. Simultaneously, any current going via X terminal is the input current flowing to the current amplifier stage, which is marked in Fig. 2 with a dashed line. That is why any current flowing to the X terminal is also amplified and moved to output terminals Z_P, Z_{PM1}, and Z_{M2}. It should be noted that – according to the current amplifier concept in [11] – if all $M_{N1} - M_{N4}$ devices have identical dimensions, then, ideally, neglecting resistances of bias current sources I_{BIAS} and $4I_{BIAS}$, the current gains to output terminals Z_P, Z_{PM1}, and Z_{M2} are equal to –1, 1 and 1, respectively. In a real circuit, which employs cascoded MOS current sources, the absolute values of those current gains are very close but not exactly equal to 1. It is also worth noticing that, according to the circuit in [11], the current gains to all outputs have similar frequency responses.

The output stage of MOCCII works in class A. This implies a constant value of current supply and also limits output current signals to a range of $\pm I_{BIAS}$. The current forced by X terminal is also limited to a range $\pm I_{BIAS}$.

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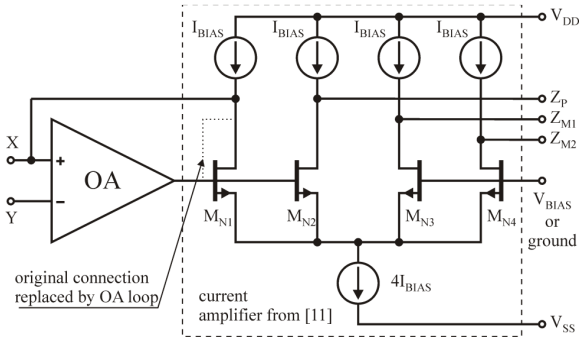

Fig. 2. A general architecture of the multiple output second-generation current conveyor. Instead of a diode connection of the device MN1 (dotted line), an *operational amplifier* (OA) is employed in the negative feedback loop. A dashed line surrounds the employed current amplifier presented in [11].

2.2. Implementation of MOCCII

A design of MOCCII using the architecture from Fig. 2 is presented in Fig. 3. The OA is built using a single pMOS differential pair (devices M_{OA1}–M_{OA2}) with nMOS current mirror as load (devices M_{OA3} – M_{OA4}). A transistor M_{OA5} is the current source for the input differential pair and its dimensions were chosen to obtain a current of approximately 50 μA. Devices M_{N1}–M_{N4} constitute the core of the current amplifier. A bias current source $4I_{BIAS}$ is built with the use of a low voltage cascode current source created by devices M_{NB1}–M_{NB4}. The diode connected devices M_{NB5}, M_{PB11} and M_{PB12} generate a constant voltage feed to the gates of M_{NB1} and M_{NB3}, which is necessary for the proper operation of the low voltage cascode. Similarly, devices M_{PB1}–M_{PB10}, M_{PB13}, M_{NB6} and M_{NB7} create four low voltage cascode current sources I_{BIAS}. The circuit is biased using a constant current of value I_{BIAS} = 250 μA. The obtained value of voltage gain measured from Y to X terminal exceeds 10k V/V, which is sufficiently high to obtain a near unity voltage gain seen from Y to X terminals when the negative feedback loop is closed through connection of X and X_{FB} terminals.

This feedback loop connection is accomplished outside the MOCII circuit in the IA structure using transmission gates. Separation of X and X_{FB} terminals enables to sense a voltage across the resistance R_X, without an extra nonlinear component formed on the transmission gate, which is used as a programmable connection. The C_{COMP} capacitor is necessary to maintain stability of the negative feedback loop.

The MOCCII circuit was designed and simulated in a Cadence Virtuoso IC6.1.5 environment using an AMS 350nm CMOS technology kit. The circuit test setup is presented in Fig. 4. Simulations were carried out with the connection of Y terminal to a voltage signal source, while X and X_{FB} terminals were tied together and connected via a 7kΩ resistor to the signal ground. Output currents were measured at circuit shorts of Z_P, Z_{M1} and Z_{M2} terminals to the signal ground. The simulated results are given in Table 1 and in Fig. 5.

The MOS devices' dimensions given in Fig. 3 are quite high in comparison with the technological minimal ones. The dimensions of transistors were chosen with careful consideration of process mismatches. According to [12] matching of device parameters is reversely proportional to the square root of the device area. In order to obtain an acceptable level of current and voltage offsets as well as acceptable changes of current gain of the conveyor, the design process was started with almost minimal technological dimensions and then the device dimensions were gradually increased until satisfactory parameter values were obtained. If the presented values are not satisfactory in a certain application, a further increase of devices' dimensions can be made, but the square root relationship should be borne in mind,

regarding that better mismatch parameters cost a large circuit area. A big area of devices causes also higher capacitances of devices and – as a result – worse frequency responses are obtained. Especially, increasing a length of MOS transistors implies a significant bandwidth loss of approximately quadratic dependence, so widths of transistors should be expanded firstly and their lengths – only if necessary.

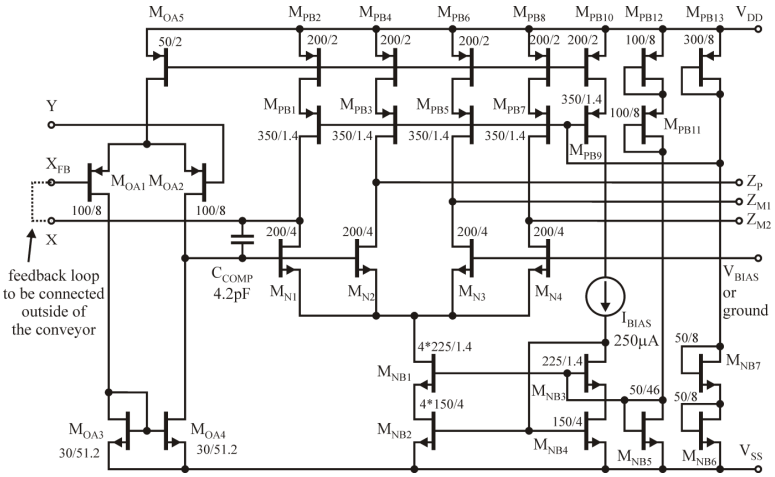

Fig. 3. A detailed scheme of MOCCII designed in AMS 350nm CMOS technology; transistor dimensions are in µm; format is as follows: optional multiplier*width/length.

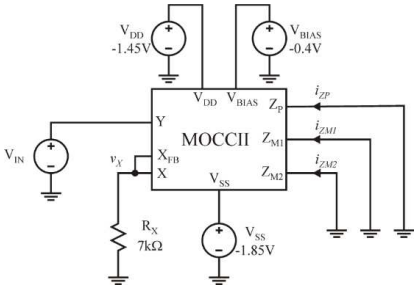

Fig. 4. The testing environment for the amplifier from Fig. 3.

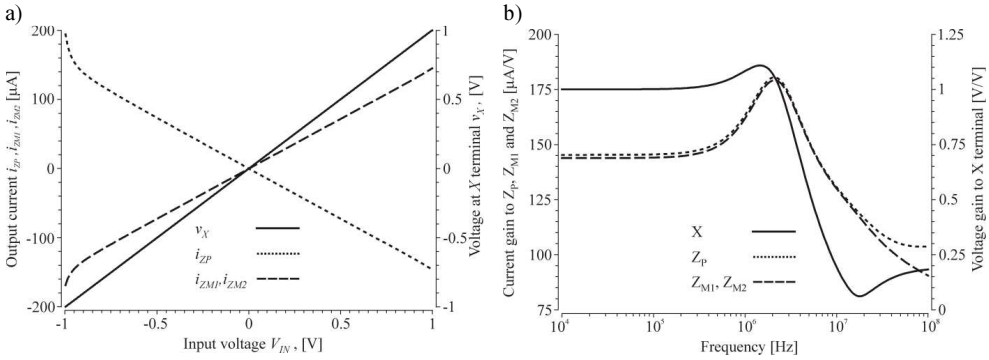

Fig. 5. The simulated characteristics of the MOCCII from Fig. 3 obtained using the testing environment presented in Fig. 4. DC transfer characteristics (a); small signal frequency responses (b).

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Table 1. The simulated parameters of the MOCCII from Fig. 3 obtained with using the testing environment presented in Fig. 4.

Parameter name	Unit	Value
Power supply voltage V_{DD} – V_{SS}	V	3.3
Current consumption	uA	1380
Voltage gain from Y to X	V/V	0.9998
3dB passband of Y to X gain	MHz	3.91
Standard deviation of voltage gain from Y to X, result of 200 runs of MC analysis	μ V/V	45.6
Transconductance from Y to Z_P @ Rx = 7 kΩ	μS	145.5
Frequency of 1deg phase loss at Z_P output	MHz	1.16
Standard deviation of transconductance to Z_P, result of 200 runs of MC analysis	nS	188.7
Transconductance from Y to Z_{M1} and Z_{M1} @ Rx = 7 kΩ	μS	144.1
Frequency of 1deg phase loss at Z_{M1} and Z_{M2} outputs	MHz	1.10
Standard deviation of transconductance to Z_{M1} and Z_{M2}, result of 200 runs of MC analysis	nS	262.5
Resistance of X and X_{FB} terminals tied together for low frequencies	Ω	1.35
Resistance of Z_P terminal for low frequencies	kΩ	371
Resistance of $Z_{M1}$and Z_{M2} terminals for low frequencies	kΩ	722
Equivalent Y input capacitance	fF	790
Equivalent Z_P, Z_{M1} and Z_{M2} capacitance	fF	563
Noise at Z_P output @100 kHz	$pA/\sqrt{Hz}$	10.2
Noise at Z_{PM1} and Z_{PM2} outputs @100 kHz	$pA/\sqrt{Hz}$	16.9
Offset voltage at X terminal for V_Y = 0 V	μV	181.1
Standard deviation of input referred offset voltage, result of 200 runs of MC analysis	μV	583
Offset output current at Z_P for V_Y = 0 V	nA	0.489
Standard deviation of Z_P output current offset, result of 200 runs of MC analysis	nA	1335
Offset output currents at Z_{PM1} and Z_{PM2} for V_Y = 0 V	nA	199.3
Standard deviation of Z_{PM1} and Z_{PM2} outputs current offset, result of 200 runs of MC analysis	nA	2219

3. Instrumentation amplifier design

A circuit diagram of the programmable input mode instrumentation amplifier is presented in Fig. 6. It consists of 2 MOCCII conveyors from Fig. 3 and 16 transmission gates. A schematic of the transmission gate is presented in the right bottom part of Fig. 6. It consists of nMOS and pMOS transistors and an inverter gate. The inverter gate is used only for generating the opposite logic level for the pMOS device. If a supply voltage V_{DD} is applied at the control input EN, then both transistors are working in the ohmic region. The gate is in the closed state and an equivalent resistance occurs between IO_1 and IO_2 terminals with a value of approximately a few hundred ohms . This resistance is slightly nonlinear but due to splitting X and X_{FB} terminals in MOCCII the nonlinearity may be eliminated in the final IA. If EN input is supplied with a V_{SS} voltage, then both MOS devices are cut off and the gate is in the open state. The resistance between IO_1 and IO_2 terminals is very high, theoretically infinitive. The dimensions of transistors in the transmission gate are small in comparison with the MOCCII circuit size and the use of 16 such items does not increase the overall area of IA by much. Feeding the control input of transmission gates with a V_{DD} or V_{SS} voltage constitutes the

final circuit configuration and the resulting mode of work. If the terminal VM is fed with a V_{DD} voltage, then the amplifier works in the input voltage mode. Analogously, if the terminal CM is fed with a V_{DD} voltage, then IA from Fig. 6 works in the input current mode. Equivalent circuit schematics for the voltage and current modes are presented in Fig. 7. The gates being in the open state are omitted, while the gates in the closed state are treated as short circuits with the exception of gates transferring a high current flowing to X terminal of MOCCII, which are represented by a resistance R_G. Both circuits have independent positive and negative current mode outputs OUT_P and OUT_M.

Let the input stage of the MOCCII from Fig. 3 be considered once again, working without connecting together X and X_{FB} terminals. If such a situation occurs, the X terminal may be treated as the output of transconductance amplifier built of a differential pair M_{OA1}, M_{OA2} with a current mirror M_{OA3}, M_{OA4} load and the second stage built of a transistor M_{N1} in the CS configuration, whose transconductance decreases twice due to working in an extended differential pair M_{N1}–M_{N4}. Thus, the approximate, small signal transconductance value in the path from the input differential pair to the current flowing out of X terminal may be expressed as:

$$gm_X = \frac{i_X}{v_Y - v_{XFB}} = -gm_{MOA1}\left(r_{MOA2} \parallel r_{MOA4}\right) \cdot \frac{1}{2} gm_{MN1}, \tag{2}$$

where: i_X is a current flowing out of X terminal; v_Y and v_{XFB} are respective voltages at Y and X_{FB} terminals; gm_{MOA1} is a small signal transconductance of device M_{OA2}; r_{MOA2} and r_{MOA4} are output resistances of devices M_{OA2} and M_{OA4}, respectively; and gm_{MN1} is a small signal transconductance of transistor M_{N1}. The value of (2) is quite high and a simulated value for the circuit in Fig. 3 is equal to 0.738 S. The node $X_{FB,}$ which senses the feedback signal, is placed directly at R_X resistor and thus any resistor R_G representing the transmission gate does not change the transfer characteristic of IA. Please notice that in the above circuit the current flowing out of X terminal flows also out of Z_P and into Z_{M1} and Z_{M2} terminals. Due to this, output currents for the input voltage mode of IA presented in Fig. 7a may be expressed as:

$$i_{OUTP} = -i_{OUTM} = 3\frac{1}{\frac{2}{gm_X} + R_X} V_{IN}\Big|_{R_X >> 2/gm_X} \approx \frac{3}{R_X} V_{IN}, \tag{3}$$

where: R_X is a resistance connected between X_{FB} terminals of MOCCII conveyors and gm_X is a small signal transconductance given by (2).

IA working in the current mode has both Y terminals connected together (to GND_CM node) and MOCCII amplifiers – due to the negative feedback loop – try to maintain the same voltage at X_{FB} terminals. It works like a transconductance amplifier with its input and output tied together. The equivalent input resistance of a single node in respect to GND_CM is thus equal to:

$$\frac{1}{2} R_{IN\_CM} = \frac{1}{gm_X}, \tag{4}$$

and the differential mode resistance is twice as high. The current flowing into X terminal also flows to Z_P and out of Z_{M1} and Z_{M2} terminals, thus output currents may be expressed by:

$$i_{OUTP} = -i_{OUTM} = -2I_{IN}. \tag{5}$$

Please notice that for the current mode only 2 outputs are tied together. Such a connection was chosen to obtain a high CMRR factor. The common mode input currents, due to summation at the outputs, are automatically eliminated only if current gains to Z_P and Z_{M1} are of exactly opposite values.

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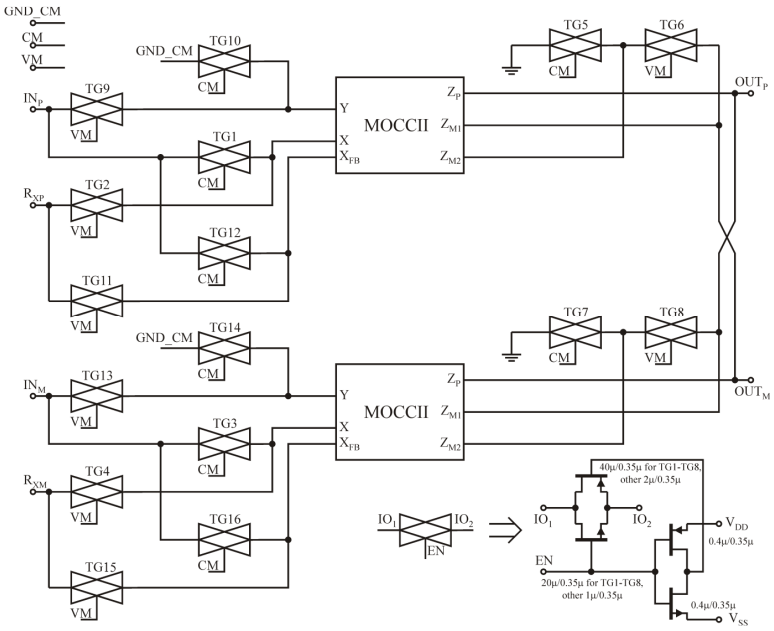

Fig. 6. A programmable input mode instrumentation amplifier using MOCCIIs and transmission gates.

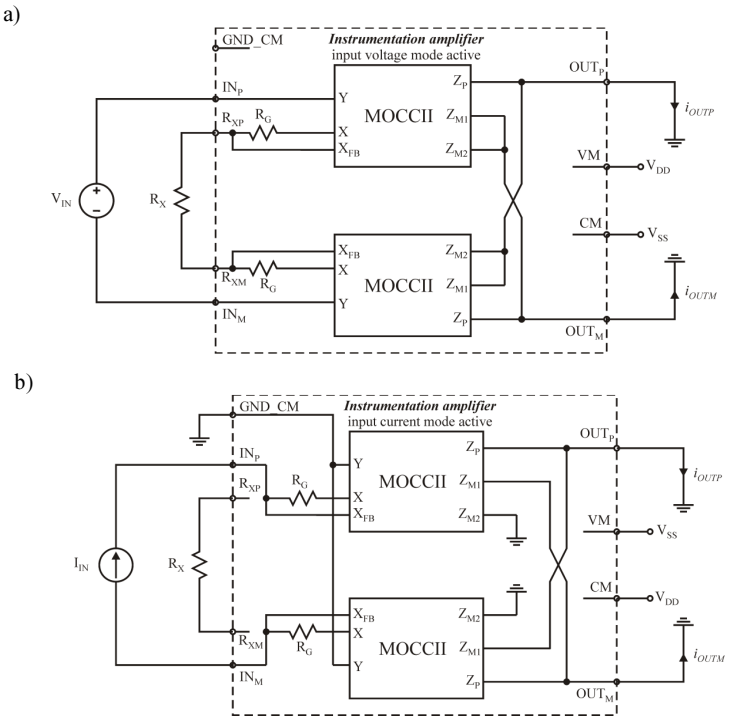

Fig. 7. Equivalent IA schematics in the input voltage (a) and the input current (b) modes together with the desired signal sources and a resistance R_X necessary for proper operation only in the voltage mode. Output currents are measured at shorts to the signal ground. R_G represents resistances of the transmission gate connected to X terminals of MOCCIIs.

4. Simulation results of instrumentation amplifier

The instrumentation amplifier from Fig. 6 working both in the input voltage and current modes has been simulated in detail. Testing environments such as in Fig. 7 with $R_X = 14$ kΩ and additional common mode input sources for simulation of CMRR factor were used. The simulation results are presented in Figs. 8–11 and in Tables 2 and 3. The power consumption is the same for both modes and is presented only in Table 2.

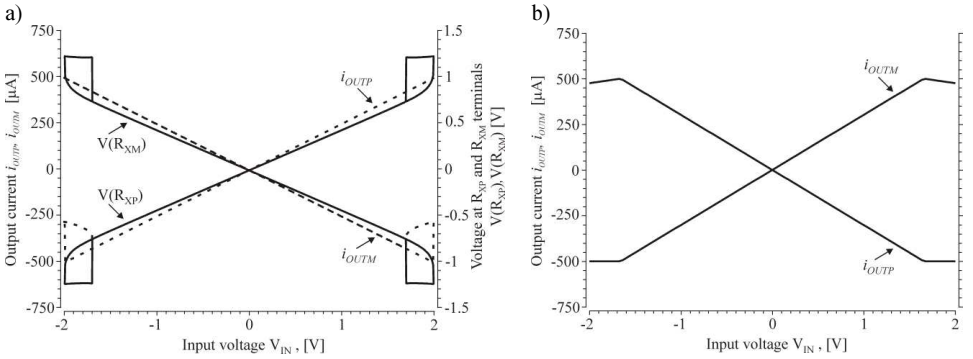

Fig. 8. DC transfer responses of the amplifier from Fig. 6 in (a) the voltage and (b) current modes.

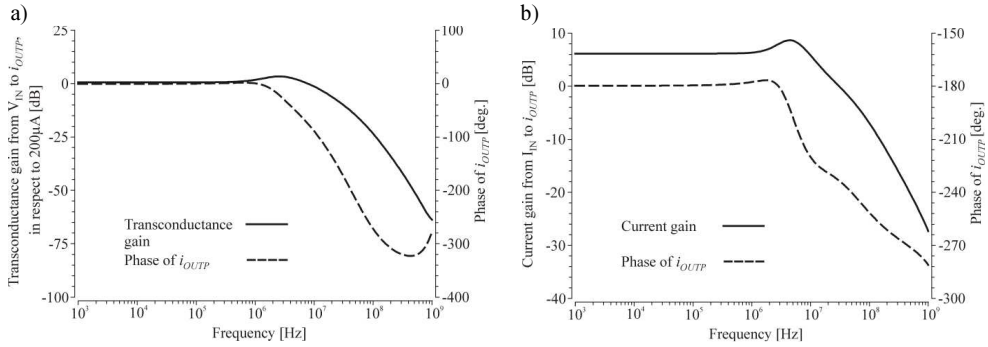

Fig. 9. AC responses of the amplifier from Fig. 6 in (a) the voltage and (b) current modes.

The DC transfer characteristics are presented in Fig. 8. In voltage mode, for the lowest and highest input voltages, a hysteresis is observed. This is caused by a limited operational range of the input MOS pair and to avoid entering this region by the circuit the input level should be limited. It is not observed in the current mode because the reference input GND_CM is connected to the signal ground. The simulated worst-case values of CMRR for 200 runs of MC simulation are equal to 55.3 dB and to 51.4 dB for the voltage and current modes, respectively.

Small signal frequency responses are presented in Fig. 9. Both configurations have a 3 dB frequency located over 11 MHz. Histograms of gains at 100Hz are presented in Fig. 11. Due to relatively large transistors used in MOCCII blocks, standard deviations of gains are small and their values are equal to about 0.13% of the desired gain.

The result of transient analysis for a 10 kHz harmonic signal in the form of THD factor is presented in Tables 2 and 3. Fig. 11 presents the results of transient analysis for a square wave of 100 kHz frequency. There are visible overshoots in the output signal. The current mode IA has a higher passband and higher slope rates at the output signal. A dynamic range defined as a ratio of the RMS value of input signal causing THD = 1% and the input referred integrated

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noise in a 100 Hz –1 MHz passband is equal to 77.3 dB and 85.1 dB for the input voltage and current modes, respectively.

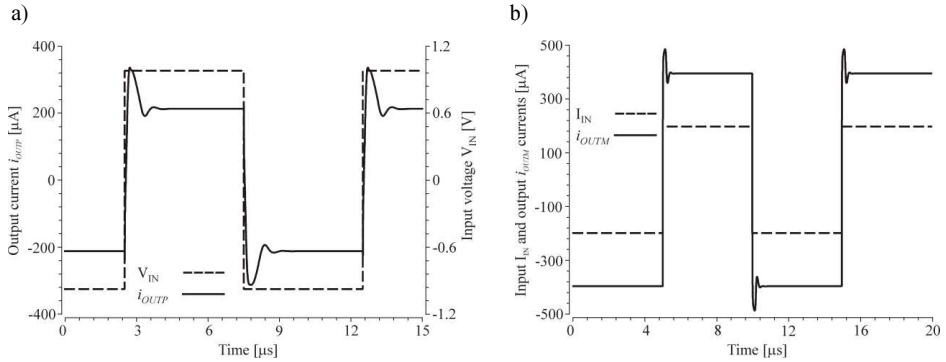

Fig. 10. Transient responses of the amplifier from Fig. 6 in (a) the voltage and (b) current modes. As the input pulse voltage or current sources of 100 kHz frequency were used, respectively.

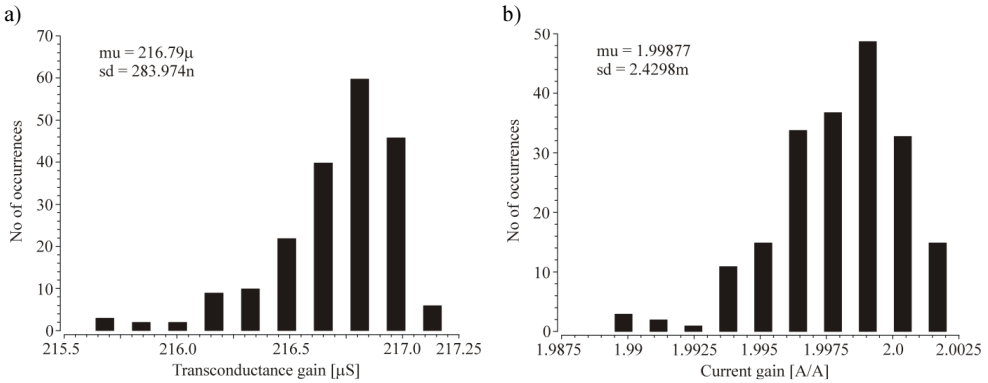

Fig. 11. Histograms of gains for the amplifier from Fig. 6 in (a) the voltage and (b) current modes. The result of 200 MC simulation runs with both mismatch and process changes.

Table 2. The simulated parameters of the instrumentation amplifier from Fig. 6 working in the voltage mode according to Fig. 7a.

Parameter name	Unit	Value
Power supply voltage V_{DD} – V_{SS}	V	3.3
Current consumption	µA	2763
Transconductance gain for Rx = 14 kΩ	µA/V	216.9
Standard deviation of transconductance, result of 200 runs of MC analysis	µA/V	0.284
3dB passband of transconductance gain	MHz	11.95
Output current range	µA	±750
Input referred noise spectral density @100 kHz	$nV/\sqrt{Hz}$	160.3
Input referred integrated noise in bandwidth 100 Hz – 1 MHz	µV	152.3
Amplitude of 10 kHz harmonic signal for output current THD =–40dB	mV	1670
Dynamic range	dB	77.3
Worst case CMRR for 200 MC runs	dB	55.3
Output resistance	kΩ	352.5
Equivalent output capacitance	fF	2005
Differential input capacitance	fF	412.3
Input referred offset voltage	mV	1.82
Standard deviation of input referred offset voltage, result of 200 runs of MC analysis	mV	18.7

Table 3. The simulated parameters of the instrumentation amplifier from Fig. 6 working in the current mode according to Fig. 7b.

Parameter name	Unit	Value
Current gain	A/A	–2
3dB passband of current gain	MHz	16.28
Standard deviation of current gain, result of 200 runs of MC analysis	mA/A	2.43
Input referred noise spectral density @100k Hz	$pA/\sqrt{Hz}$	9.899
Input referred integrated noise in bandwidth 100 Hz – 1M Hz	nA	9.778
Amplitude of 10kHz harmonic signal for output current THD = –40 dB	μA	248
Dynamic range	dB	85.1
Worst case CMRR for 200 MC runs	dB	51.4
Input differential resistance for low frequencies	Ω	2.70
Input referred offset current	nA	98.9
Standard deviation of input referred offset current, result of 200 runs of MC analysis	μA	2.426

5. Conclusion

In this paper a programmable input mode instrumentation amplifier is presented. Such programmability has been not reported in the literature till now, but may be very desirable when a circuit is to be employed in a universal integrated circuit such as an FPGA or a microcontroller. The instrumentation amplifier is built of two multiple output second order current conveyors and 16 transmission gates. The whole circuit has been designed using AMS 350nm CMOS technology in the Cadence Virtuoso environment. The detailed results of simulation of both multiple output current conveyor and instrumentation amplifier are presented. Input mode selection of instrumentation amplifier is performed through appropriate voltage feed to the control nodes. The power supply of the circuit is 3.3 V and it consumes 9.1 mW of power. The IA exhibits a ± 1.68 V linear input range in the voltage mode and ± 250 μA in the current mode. A 3 dB passband of the circuit is located above 11 MHz. The amplifier works in class A, so its current supply is almost constant and does not cause noise disturbing precision analogue circuits working nearby. A dynamic range of the amplifier is equal to 77.3 dB in the input voltage mode and 85.1 dB in the current one. Extensive MC simulations have also been performed. All the results confirm usability of the proposed instrumentation amplifier in real applications in medium precision range applications with the resolution in a range of 10 bits.

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