3D PCB package for GaN inverter leg with low EMC feature

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Keywords

« EMC/EMI », « Gallium Nitride (GaN) », « HEMT », « Wide bandgap devices »

Abstract

This paper presents the adaptation of a 3D integration concept previously used with vertical devices to lateral GaN devices. This 3D integration allows to reduce loop inductance, to ensure more symmetrical design with especially limited Common Mode emission, thanks to a low middle point stray capacitance. This reduction has been achieved by both working on the power layout and including a specific shield between the devices and the heatsink. The performances of this 3D layout have been verified in comparison with a more conventional 2D implementation, using both simulations and measurements.

1. Introduction

During the recent years, an expanse growth of gallium nitride (GaN) transistors manufacturing technology has been observed. These devices start to be commonly used in modern Power Electronics applications. The significant increase of the switching speed associated with these new devices [1] causes several issues such as electromagnetic interference (EMI) non-compliance, voltage overshoot with oscillations, power drive interactions, etc. One of the biggest challenges in implementing these devices is an identification and minimization of the origin of these drawbacks. This paper first briefly reminds the main design rules associated with the layout dedicated to high speed switching (section 2). Then, the advantages of a 3D integration solution previously used with vertical devices are presented, and the necessary adaptations for being used with lateral GaN devices introduced in section 3.
A specific attention is paid to the shielding of the leg middle point with respect to ground: both power layout and heatsink contribute to this stray capacitance is addressed. Finally, in section 4 the performances of the proposed 3D layout, in comparison with a more conventional 2D implementation are evaluated.

2. Layout impact on EMC of power converters with GaN devices

The transitions of currents and voltages during switching operations in phase-leg configuration (further considered as a commutation cell) are well-known sources of electromagnetic disturbances.

Those transients together with existence of capacitive and inductive stray elements generate high frequency currents which are usually separated into differential (DM) and common mode (CM). Fig.1 illustrates the equivalent circuit of a switching cell, including the most impacting stray elements originating the main EMC issues. The inductive nature of the electrical link between the decoupling capacitor and the switching devices is taken into account by the internal stray inductance of the capacitor (ESL - Equivalent Series Inductance), Ls+ and Ls- as well as the two Lc, which are also the parts of the gate circuits. These latter are also accounted using Lg.
The capacitive behavior of the layout is modeled using C+ and C-, between DC bus and ground, and also Cout which represents the stray behavior between the output of the converter and the ground. In addition, other stray capacitances Ciso are important to model the propagation path of Common Mode current through the driver's power supplies. Finally, the stray capacitances of components are also part of the model, since they can generate oscillations with other stray elements of the layout.
The following subsections the impact of all these stray elements on the EMC behavior of the switching cell is detailed.

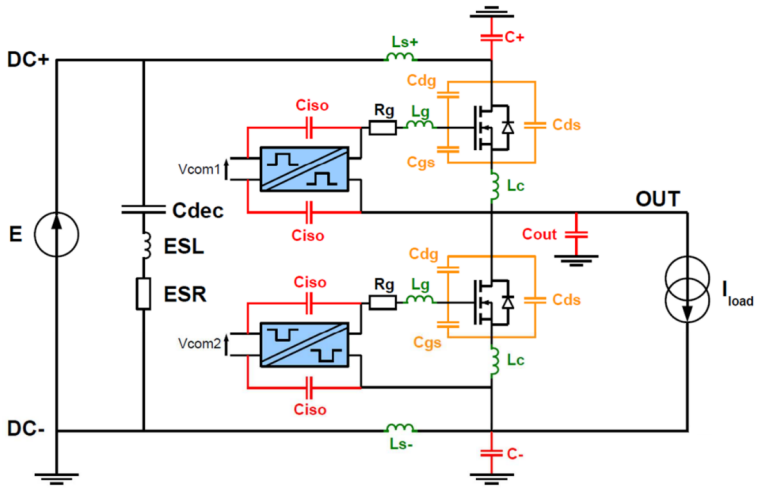

Fig. 1: Electrical scheme of commutation cell with parasitic elements [2]

2.1. Voltage overshoot and ringing

The most visible effect of high-speed switching operation is the voltage overshoot across transistors at turn off. The overshoot is caused by an induced voltage drop across an inductance $L_{switching}$ of the commutation loop ($L_{switching}$ being the sum of inductances: Ls+, Ls-, 2*Lc and ESL according to Fig. 1 [2] also with mutual inductances between them). The high value of di/dt together with $L_{switching}$ can generate overshoot exceeding the voltage rating of the device which may cause its damage. To achieve a very high current commutation speed, the stray inductance of the switching loop has to meet nano – or even subnanohenry range.
Another effect related to the stray inductance $L_{switching}$ are voltage oscillations at transistor turn off. Those oscillations are related to $L_{switching}$ and parasitic output capacitance of a device (Coss). The oscillations cause additional losses and add peaks on a spectrum in the high frequency range. Moreover, the ringing phenomena may change switching conditions for the next commutation if the oscillations are not properly damped. The damping factor describing this process can be calculated by using Eq. 1. According to this equation, the reduction of the stray inductance $L_{switching}$ leads to a significant increase of damping factor [3].

$$\zeta = \frac{R}{2} \cdot \sqrt{\frac{Coss}{L_{switching}}} \quad (1)$$

2.2. Common mode capacitances

The capacitive behavior of the switching cell including the stray capacitances to the ground is shown in Fig. 1. The most impacting capacitance is Cout, since it is submitted to a high dV/dt during transients and generates high CM current. Besides, gate driver insulation and supply stray capacitance Ciso creates an additional path for CM noise. This is not addressed in this paper, but previous work as [4] did focus on this specific aspect.

Moreover, two stray capacitances (C+ and C-) are connected from stable potentials DC+ and DC- to the ground, creating an additional path for CM current and can provide recycling of the current inside switching cell. They should thus be as large as possible. However, C+ and C- should be designed carefully to keep the symmetry. Otherwise high frequency currents flowing in DC bus induce voltage variation, that can create additional common mode current [2].
In summary, the most important design effort is to reduce the capacitance Cout and maintain the symmetry (equal values) of capacitance C+ and C-, which have to be increased to help in recycling CM current.

2.3. Decoupling capacitors and symmetry of DC+ and DC- layout

One of the key aspects for reaching low stray inductance in a power loop is using decoupling capacitors. Their role is to create a low impedance path for high frequency currents circulating in a switching cell. Decoupling capacitors are suppressing high frequency AC signals or voltage spikes at the input of the switching cell and ensure a stable DC voltage at the transistor transients. The selection of decoupling capacitors should be done carefully to ensure a correct value of the capacitance and low ESL for high damping and filtering high frequency transient currents [5].
Moreover, connections of decoupling capacitors and GaN devices (from both sides DC+ and DC-) should be kept symmetrical (the same value of L+ and L- stray inductances). Non-symmetrical design can cause a generation of differential mode current from switching cell to converter's supply and additionally with a lack of symmetry C+, C- capacitances may cause coupling between differential and common mode [6].

2.4. Power and gate circuits coupling

There are two types of coupling between power and gate circuit: inductive and capacitive. Both of them can interact and negatively influence GaN switching performance causing a false turning on or off, or slowing down commutations. The inductive coupling is represented with the common source inductance Lc. A high current variation in a power loop generates the disturbances on the gate circuit and negatively affects the commutation process increasing the switching losses. Thus, above mentioned couplings between power and gate circuits must be minimized, e.g. by designing a Kelvin Source Connection [7]. The inductive coupling also exists due to the mutual inductance between the power and gate part. It should be minimized by designing a small gate loop surface and geometrical separation of power and gate loops. The inductance Lc accounts for both effects, as explained in [8]
The capacitive coupling is created through the "Miller capacitance" (Cgd). The voltage variations dVds/dt cause the flow of parasitic current through Cgs and the whole gate circuit which can lead to false turn-on if the inducted voltage drop on the gate impedance is above the threshold value of GaN device [9]. A negative voltage for turning off can significantly improve gate immunity on the Miller effect. However, it can also increase the global losses in case of using large dead times. Therefore, to avoid this disturbance, the gate circuit must be designed with a low value of a stray inductance Lg+Lc.

3. 3D layout for GaN transistors

According to the role of each stray elements underlined in the previous section, designing a power and gate circuit layout suited for high speed devices should meet following requirements:

- Minimizing stray inductances, thanks to reduced loop area
- Reducing mutual inductances between power and gate circuits, using e.g. perpendicular planes
- Reducing Cout and increasing C+ & C-, keeping a perfect symmetry of C+, C-, Ls+, Ls- to avoid mode conversion.

Nowadays, all commercial GaN transistors are produced with a lateral (horizontal) arrangement and adapted for planar modules. This approach corresponds to the classical way of designing power converters, which can be called "2D", where all power components are placed on the one side of PCB for one side cooling system. Using all degrees of freedom in the layout design, this planar design approach prevents to reach previously mentioned guidelines. Furthermore, reaching small loop inductance is easier with vertical implementation, especially for high voltage: the sub-nanohenry performance reached by [10] in a 2D implementation was achieved for a 40V application, using ultra small package.

In this section, we will therefore present how to adapt a promising 3D power layout concept – PCoC: Power Chip on Chip - to lateral GaN devices. At first, the main features of the PCoC concept will be reminded. This implementation will then be adapted to GaN lateral devices. Shielding the middle point of the switching cell is one key feature of the 3D layout, therefore a dedicated section will focus of this aspect.

3.1. Power Chip-on-Chip concept

The solution of "3D" power loop structure (Power Chip-on-Chip, PCoC) can be proposed (Fig. 2) to reduce $L_{switching}$ and decrease EMI generation by keeping symmetrical design and placing components one below the other. This idea has been developed originally for vertical semiconductor devices (Silicon and Silicon Carbide) [11] [2]. The main idea of this concept is an integration of the power devices inside a bus-bar structure. Two distribution planes are placed on the top and bottom of the system, creating large areas of copper connected to the stable potentials DC+ and DC-. These wide conductive sections ensure an extremely small inductance between power ports and switching cell. The decoupling capacitors might be placed vertically between DC+ and DC- very close to the power transistors' pads. In this manner the power loop area is reduced and the stray inductance $L_{switching}$ is reduced to the minimum (Fig. 2). Bus bar idea offers the parasitic couplings minimization and symmetrical arrangement of the copper tracks which affects on EMI reduction.
The other main advantage of the PCoC concept is that the 3D arrangement allows obtaining the middle point of the dies (load connection) surrounded by the DC+ and DC- potentials. Therefore, the DC bus acts as a shield with respect to ground, thus reducing the value of Cout to almost zero, maximizing C+ and C-, and keeping symmetry of all stray elements of the DC bus.

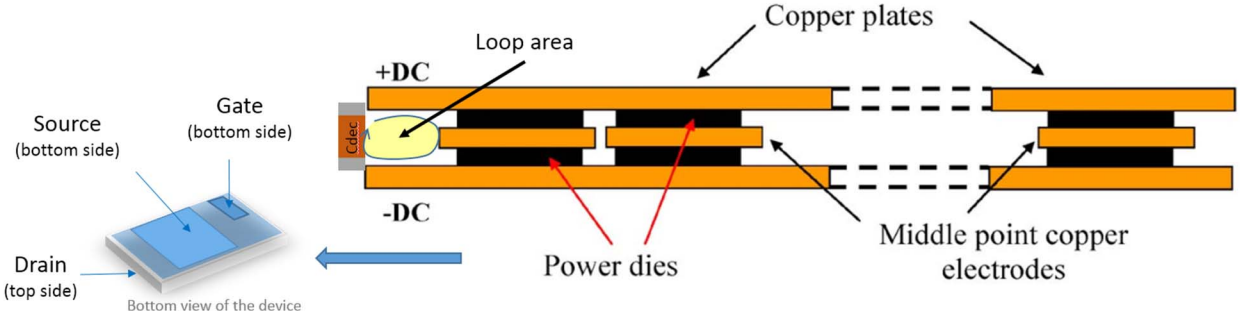

Fig. 2: PCoC concept basis [11] using vertical devices

However, the lateral arrangement of the GaN devices does not allow the simple stacking of the devices to build a switching leg, since all connections are on the same side, the other side being only a thermal pad. Therefore, the concept has to be modified.

3.2. Proposed 3D PCoC design for lateral GaN devices

The proposed conception utilizes only PCB to arrange all connections and provides a high level of integration between discrete components and PCB copper layers (planes/polygons) and tracks. The basic idea from [12] is shown in Fig.3. In this paper, the proposed design focuses on simplicity of manufacturing and assembling the boards. Thus, the multilayer PCB with the minimum number of layers which gives satisfying results (4 layers) was used to implement the PCoC structure.

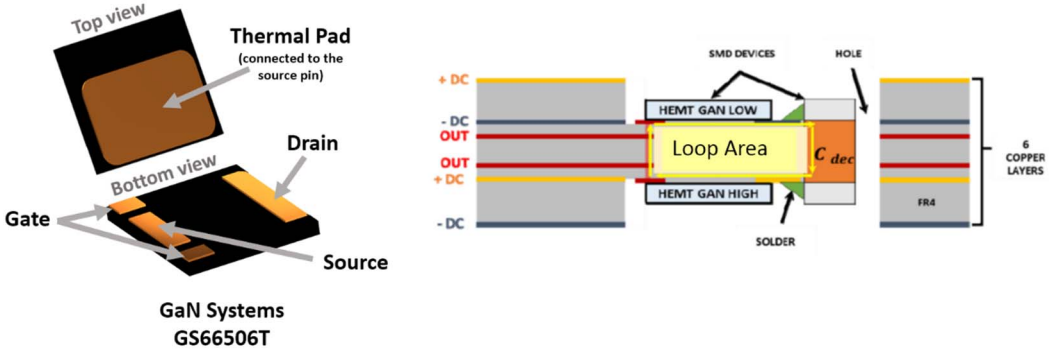

Fig. 3: PCoC concept of [12], which will be used with lateral devices from GaN Systems [13]

In this PCoC concept the thermal path has to be separated from electrical connections since the PCB used for this purpose cannot evacuate easily generated heat. Therefore, external heatsinks are used on both sides of the switching cell as displayed in the Fig. 4. Using other technology as Insulated Metal Substrate (IMS) instead of PCB would allow conducting the heat flux using the same side of the chip, but this is usually only a single layer substrate disabling all necessary connections e.g. for gate circuits. Therefore, we found some specific packages allowing the different use of each sides: one for electrical connection and one thermal pad for the heatsink [13].

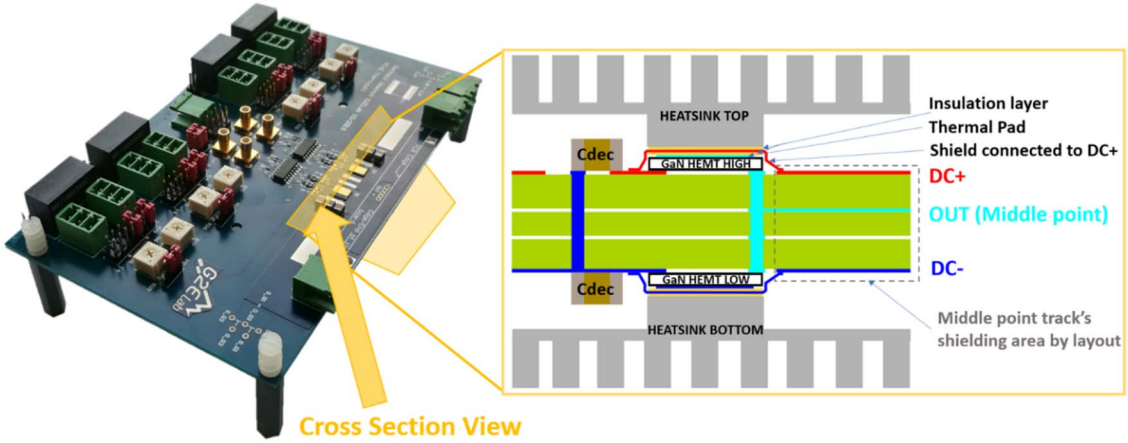

Fig. 4: Prototype of converter with the ‘‘3D’’ PCoC layout and cross view of arranged cooling system

The GaN Systems GS66506T transistors [13] with 650V blocking capability and a continuous drain current 22.5A and top cooling thermal pad are used. Moreover, the decoupling capacitors placement differ from the Fig. 3. They are placed horizontally (on the both sides of PCB) and connected to the bus-bars directly and by dedicated vias. Twelve 100nF 630V SMD capacitors (KEMET C1210C104KBR) in case 1210 were used to decouple two phase-legs of converter (6 capacitors per phase-leg). Those capacitors, together with two EPCOS CeraLink capacitors 500nF 700V, are creating a DC-Link with 2.2µF capacity. All of those components are placed symmetrically on the both sides of PCB.

The exploded 3D view of the power layout is shown in Fig. 5. The GaN switches are marked by arrows, indicating the placement one below the other corresponding to the PCoC idea. The transistors are connected directly to the DC+ and DC- bus bars and the common point (middle point of phase-leg) is created by the vias connection. The converter’s phase-leg middle point track is arranged on the inner layer of the PCB, therefore being in the middle of the DC bus, as in the PCoC basic concept. The decoupling capacitors are placed as close as possible to the switches on each side of the PCB (6 capacitors for each phase-leg – 3 on the top and 3 on the bottom). The switching loop is illustrated in Fig. 5: The loop area is as small as possible, since it is contained inside the PCB thickness. In order to reduce more the switching loop, the PCB with a reduced thickness can be considered. Embedded dies technology is another option that could permit also to place GaN components closer one to the other. Regarding gate drive layout design, short connections and perpendicular plane with power layout have been chosen to meet the design criteria of section 2.4.

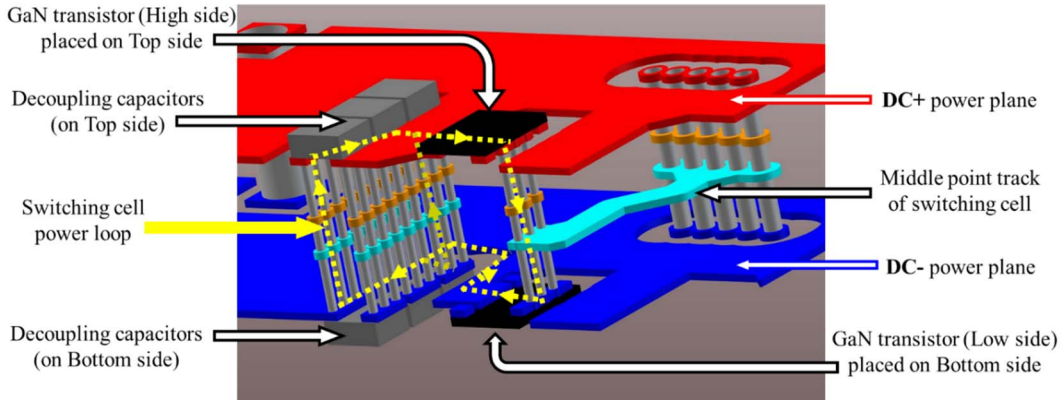

Fig. 5: Exploded 3D view of proposed PCoC layout (thickness of the board in scale 10:1)

3.3. Shielding

Beside symmetry and small switching loop area, the superior advantage of the PCoC concept is the shielding of the middle point of the leg, connected to the output filter of the converter. As displayed in Fig. 5, this middle point is located in the inner layer of the converter, as in the original concept of Fig. 2. Therefore, shielding reduces Cout (middle point to ground capacitance) to almost zero, since it is embedded inside the DC bus. However, there is another stray capacitance to the ground, which is brought by the GaN die itself: the thermal pad of the GaN devices used in our application is actually connected to the source. Therefore, the Top Switch of the inverter leg will also contribute to the Cout value described in Fig. 1, what illustrates the electrical representation in Fig. 6, where Cout has two contributions: Cout_Layout and Cout_Heatsink.
It is worth noting that even without the direct connection of the thermal pad to the source, as in the used dies, a quite large stray capacitance between those potentials would also exist and the issue would remain. In the current situation using package [13], Cout_Heatsink can be roughly evaluated through a parallel plate capacitor formula. The thermal pad area is 5.1*3.1mm² and the thickness of the insulator between die and heatsink is approximatively 100µm. Permittivity is considered equal to unity in this first approximation. Therefore, Cout_Heatsink is roughly 1.5pF.

Reducing this value without degrading the thermal path is not possible. Therefore, it has been decided to insert a conductive layer between the die and the heatsink, insulated from both thermal path and heatsink, and to connect this layer to the DC+ potential. This results in capturing all Common Mode currents generated through this stray capacitance and recycle it internally inside the converter through a stable potential. The principle is illustrated in Fig. 7. It has been supposed that the thermal path is constant, therefore the insulation layers are only 50µm, resulting in twice the initial capacitance.

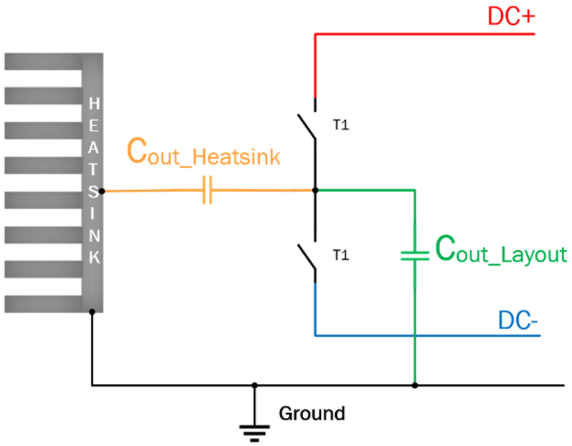

Fig. 6: Different contributions to Cout (middle point to ground stray capacitance): power layout and Top Switch

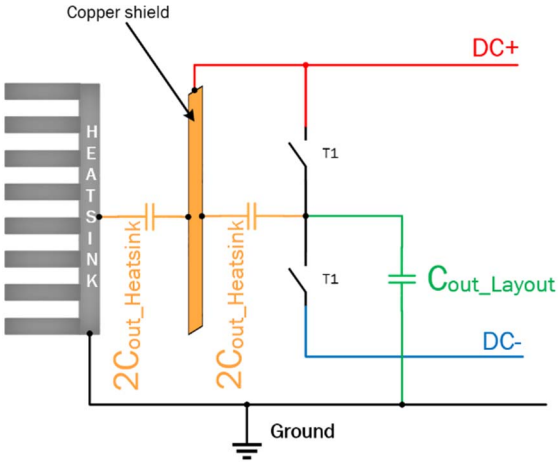

Fig. 7: Removing the impact of Cout_Heatsink using a shielding layer connected to the DC plus potential

To validate the principle of this shielding approach a simple circuit simulation has been carried out, without the effect of the power layout (Cout_Layout). A simple switching cell has been connected to a LISN (Line Impedance Stabilization Network) in order to obtain the Common Mode current. Fig. 8 shows the comparison in the initial case where the conducting layer is not connected (thus Cout_Heatsink = 1.5pF) with the case where it is connected to the DC+ potential. The decrease of CM current on the whole frequency range is impressive, between 20 and 50dBs.

To verify this result, an experimental validation has also been carried out with the converter built according to the geometry of Fig. 4. To focus on the heatsink shielding only and masking all other stray imperfection an emulation of the phenomena with high values of lumped capacitors (2.2nF) has been used (Fig. 9 right). Again, the CM reduction is huge when the shield is connected to DC+ potential, as displayed in Fig. 9 left. Some resonance around 20MHz results from the effect of the stray inductance of the lumped capacitors.

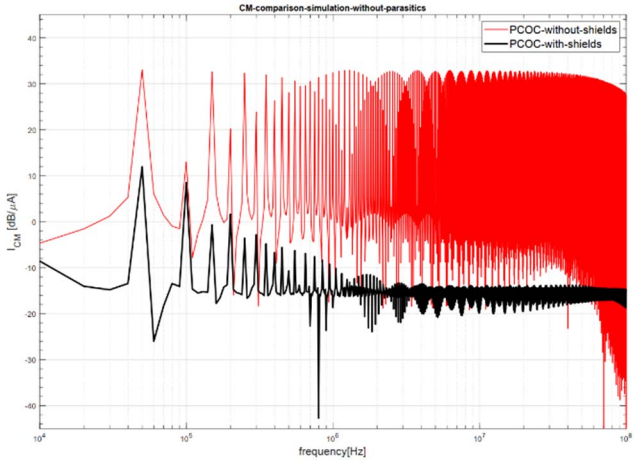

Fig. 8: Effect of heatsink shield connection to the DC+ on CM current– No other stray elements

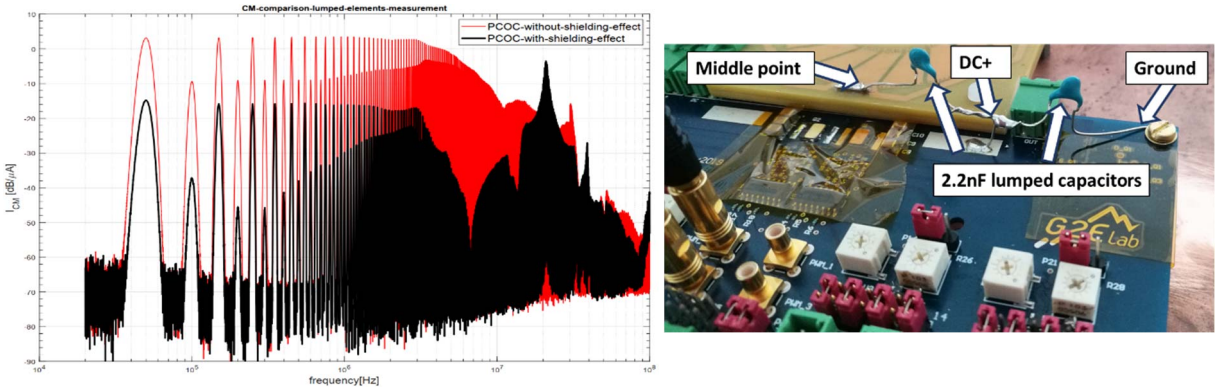

Fig. 9: Emulation of heatsink shield effect with high values lumped capacitors to avoid the impact of other stray elements

Finally, a full electrical model of the 3D power layout has been obtained using Ansys Q3D Extractor [14]. This model of the power layout has been completed with the stray capacitance of the Top switch device to the heatsink, according to Fig.7. In order to compare two extreme cases, two different power layouts have been modeled: one with the middle track embedded in the busbar, as in Fig. 5, and the shield of the heatsink connected to the DC+ potential (best case) and the other one without the heatsink shield and with a power layout of the DC bus not shielding the middle track (worst case). The comparison between these two extreme cases shows the large impact of the contributions of both Cout_Heatsink and Cout_Layout. The reduction of only 10dBs with both shielding effects will be discussed in section 4: it is due to a non-perfect overlap between DC bus and middle point track, which results in a non-zero value for Cout_Layout.

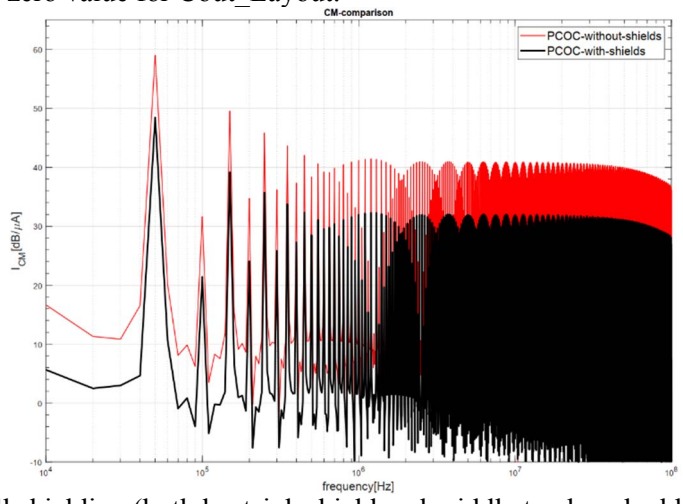

Fig. 10: Effect of a full shielding (both heatsink shield and middle track embedded in the DC bus) in comparison with no shield (no heatsink shield and middle track outside the DC bus) on CM

4. Performance evaluation of PCoC-GaN Layout

With the proposed adaptation and efforts put on the heatsink shielding, the PCoC-GaN can be realized and tested. To assess the EMC performances of the switching leg, two different versions have been built: one 3D corresponding to Fig. 5 and another one using a more conventional 2D layout illustrated in Fig. 11. Both PCBs look quite similar as shown by Fig. 12, except that in the 2D version all 6 decoupling capacitors and 2 power devices are on the same side. Both prototypes include two switching legs in order to realize two inverters in future tests.

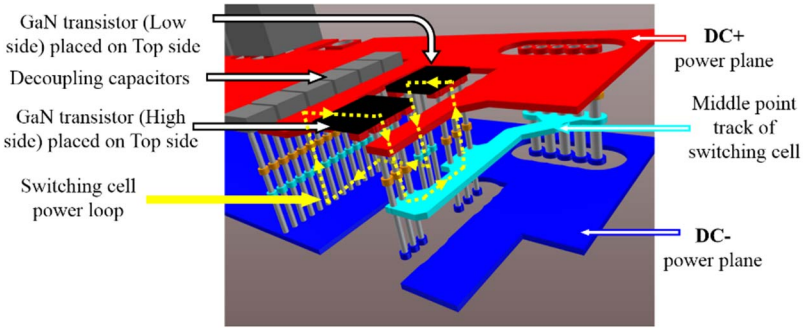

Fig. 11: Exploded 3D view of a conventional 2D layout (thickness of the board in scale 10:1)

Fig. 12: 2 prototypes realized: one PCoC-GaN and one 2D realization

The first test was to measure the performances in terms of voltage overshoot. Using the simulations from Q3D the stray inductance of the 2D and 3D layouts has been compared. They have been computed at 100MHz, which is approximatively the equivalent frequency of the transitions measured in the actual converters (Fig. 13). Results are given in Table 1. The voltage overshoot of the 2D layout is actually larger than the 3D layout, what confirms the stray inductance evaluation with simulation.

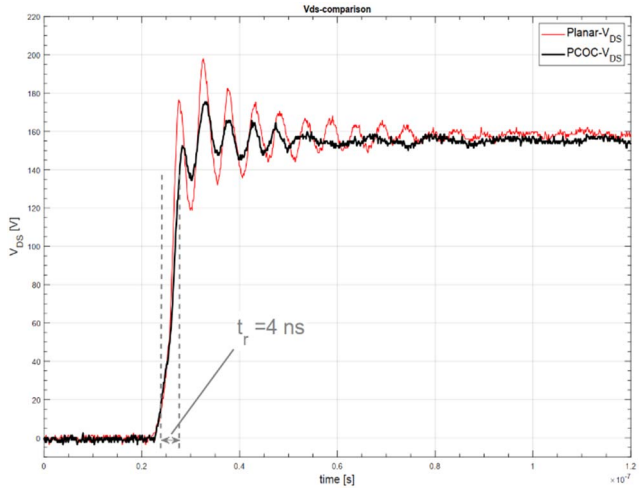

Table I: Stray inductance of the switching cell. Comparison between 2D and 3D layouts at 100MHz.

Layout	2D	3D
Stray inductance @100MHz	7.0nH	5.2nH

Fig. 13: Voltage overshoot comparison between 2D layout and 3D Layout

The second important feature of the switching cell to be verified is obviously the EMC performances. A first simulation based on the Q3D models of the two layouts (including the shielding of heatsink for both layouts, since phenomena are similar in the 2D layout) allows comparing both switching cells in terms of CM generation (Fig. 14). The emission is about 6dBs lower for the PCoC-GaN.

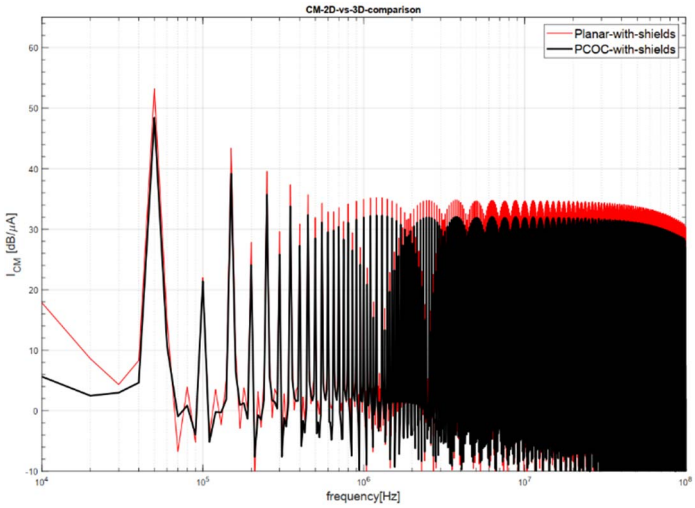

Fig. 14: Comparison in terms of CM current between 2D and 3D layouts based on simulations

After investigation, it appears that this difference can be attributed to a better shielding of the middle track in the 3D case, in comparison with the 2D layout (Fig. 15), due to the higher number of devices on the same level in the 2D layout, which occupies a larger area.

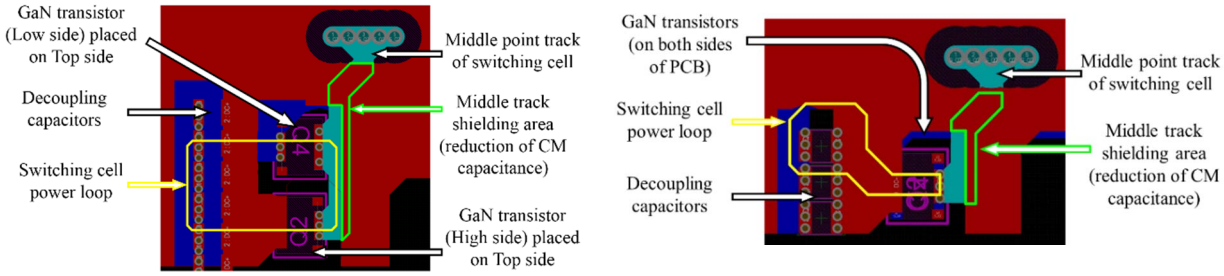

Fig. 15: Middle track embedded in the DC bus: comparison between 2D (left) and 3D (right) layouts. The 3D layout is better shielded (higher surface of middle track embedded in the DC bus). Note also the illustration of switching loop area.

Finally, the comparison of EMI in terms of DM current has also been checked (Fig. 16) and is a bit better for the PCoC-GaN. This can be due to the more symmetrical design even if further investigations have to be carried out regarding this matter.

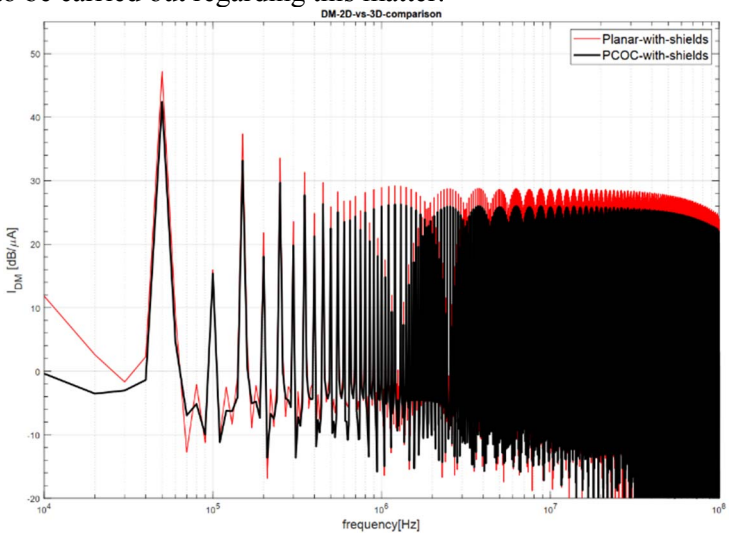

Fig. 16: Comparison in terms of DM current between 2D and 3D layouts based on simulations.

Unfortunately, the two prototypes failed during EMC measurements carried out in a hurry due to reduced amount of time available in the Lab before finalizing the paper (only one half day per week allowed during COVID time for this research action in the EMC Lab). Therefore, no experimental results are available to confirm the simulations.

Conclusion

With dramatically increasing switching speeds of wide bandgap devices, the careful design of power layout becomes a key step to build a converter operating properly. Reduced voltage overshoot and low EMI generation require fulfilling design rules as sub-nanohenry switching cell inductance, symmetrical design of the DC bus in terms of both stray inductance and capacitance, and reduced capacitance of the middle point of the leg with respect to the ground. To achieve these goals a 3D layout (Power Chip on Chip) concept previously introduced has been adapted to GaN devices, which are lateral and not vertical as SiC or Si dies. Multilayer PCB with the minimum number of layers (4 layers) was used to implement the PCoC structure with minimum cost.
A specific attention has been paid to the shielding of the middle track by embedding it inside the DC bus. Another key point has been identified regarding the Common Mode generation: the thermal pad of the GaN devices used is electrically connected to the source, thus increasing the middle point capacitance through the stray capacitance of the top switch with the heatsink. A specific shielding solution has been proposed and validated with both simulations and measurements in a specific test case. Both 3D and conventional 2D power layouts need this solution to reduce CM current generation. Finally, the 3D power layout exhibits lower loop inductance than the conventional 2D layout, thus lower voltage overshoot. Unfortunately, only power waveform has been recorded, since the two prototypes failed during EMC tests. However superior performances of the 3D layout are expected when looking at simulation results.

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