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A Direct Modulation for Matrix Converters based on the One–cycle Atomic operation developed in Verilog HDL

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***Abstract*—This paper presents a fast direct Pulse Width Modulation (PWM) algorithm for the Conventional Matrix Converters (CMC) developed in Verilog Hardware Description Language (HDL). All PWM duty cycle calculations are performed in one cycle by an atomic operation designed as a digital module using an FPGA basic blocks. The algorithm can be extended to any number of output phase. The improved version of the discontinuous Direct Analytic Voltage PWM (DAV–PWM) method is proposed, in which the use of trigonometry, angles and program loops has been eliminated. The proposed DAV–PWM is equivalent to the Space Vector Modulation (SVM), it can be applied during input asymmetry and also allows for the control of the displacement input angle. The proposal has been verified using the circuit simulation in PSIM, digital structure modelling in ModelSim, and finally through an experiment.**

***Index Terms*—matrix converters, AC/AC converters, pulse width modulation, fpga device.**

NOMENCLATURE

T	Transposition of the matrix.
$\mathbf{v}_\mathrm{i}$	Measured input voltages $[v_{\mathrm{i}1}, v_{\mathrm{i}2}, v_{\mathrm{i}3}]^T$.
$\mathbf{v}_\mathrm{o}$	Averaged output voltages $[v_{\mathrm{o}1}, v_{\mathrm{o}2}, v_{\mathrm{o}3}]^T$.
$\mathbf{i}_\mathrm{i}$	Averaged input currents $[i_{\mathrm{i}1}, i_{\mathrm{i}2}, i_{\mathrm{i}3}]^T$.
$\mathbf{i}_\mathrm{o}$	Measured output currents $[i_{\mathrm{o}1}, i_{\mathrm{o}2}, i_{\mathrm{o}3}]^T$.
$\mathbf{D}$	PWM duty cycle matrix with size 3×3.
x	Real signal component.
y	Imaginary signal component.
$\mathbf{v}_\mathrm{ix}$	Matrix of $\mathbf{v}_\mathrm{i}$ in–phase components.
$\mathbf{v}_\mathrm{iy}$	Matrix of $\mathbf{v}_\mathrm{i}$ quadrature components.
$\mathbf{v}_\mathrm{ox}$	Real parts of reference voltages $[v_{\mathrm{o}1\mathrm{x}}, v_{\mathrm{o}2\mathrm{x}}, v_{\mathrm{o}3\mathrm{x}}]^T$.
$\mathbf{v}_\mathrm{oy}$	Imag. parts of reference voltages $[v_{\mathrm{o}1\mathrm{y}}, v_{\mathrm{o}2\mathrm{y}}, v_{\mathrm{o}3\mathrm{y}}]^T$.
ϕ_i	Input displacement angle.
$s_\mathrm{i}, s_\mathrm{o}$	Input, output voltage sectors.
ω_i	$= 2\pi f_\mathrm{i}$, where f_i is the input frequency.
ω_o	$= 2\pi f_\mathrm{o}$, where f_o is the output frequency.
q	$= V_\mathrm{o}/V_\mathrm{i}$, Voltage transfer ratio.
q_max	$= \sqrt{3}/2$, Maximum value of q.
T_PWM	Modulation period.
f_s	$= 1/T_\mathrm{PWM}$ sampling frequency.

I. INTRODUCTION

THE CMC, shown in Fig. 1, contains semiconductor switches arranged into a matrix configuration divided into three cells $\{h_{11}, h_{21}, h_{31}\}$, $\{h_{12}, h_{22}, h_{32}\}$, and $\{h_{13}, h_{23}, h_{33}\}$. Comparing to AC/DC/AC back–to–back converters with large capacitors in DC–link, the CMC allows for direct AC–AC conversion using the small input filter, which is an advantage of these solutions [1]–[3]. The general motor drive application scheme with the matrix converter is illustrated in Fig. 1. Such a topology permits for regenerative power from the electrical motor M with negligible input grid current harmonic content. An important feature of the CMC control is the possibility to adjust the input displacement angle to zero [4]–[6]. The single switch h can be built from two transistors with two diodes or two RB–IGBT devices [1], [7].

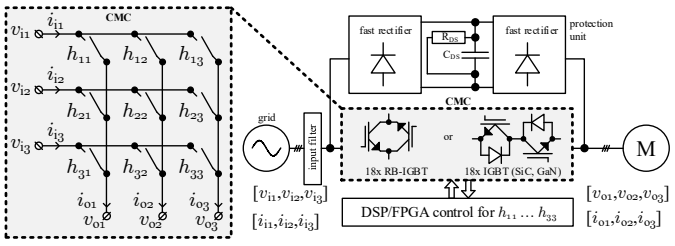


Fig. 1. Classic Matrix Converter and its typical application scheme.

The single CMC's cell is properly controlled to prevent line–to–line short circuits and to maintain a continuous waveform of the load current. Due to the safe commutation process requirement, the dead–time mechanism should be applied during the generation of switches control signals. The overvoltage upon the switch, caused by an interruption of the inductive current, has to be absorbed by a clamp circuit [8], [9]. The reduction of the scale of both the input filters, and the clamp circuit, can be reached by applying faster semiconductors with a high operations frequency, thus a panel size of the CMC can be significantly reduced [10]. Attempts to integrate this panel with the electric motor have already taken place [11]. Gallium Nitride (GaN) and Silicon Carbide (SiC) semiconductors offer fundamental advantages over silicon solutions [12]–[15]. The switch's operation frequency can be very high compared to the silicon counterparts, which makes these devices great for high–frequency application, which also includes high–speed drives in compressors or high–speed generators in gas turbines [16]–[18]. Such applications require complex calculations within a short period of time.

TABLE I
THE SUMMARY OF THE CONDUCTED RESEARCH PATH.

formal analysis	Conducted using Matlab R2020a software, containing symbolic variables, matrix operations and graphical visualization of the vectors arrangement.	
	ANSI C	Verilog HDL
code developing	The algorithm code written in ANSI C/C++ was developed in Visual Studio 2019 as a function of the user DLL block for power electronic circuit modelling software – PSIM 11.	Equivalently, the same functionality has been developed using Verilog HDL language using ModelSim - Intel Fpga Starter Edition 10.5b.
simulation and validation	Simulation has been performed using the complete electrical scheme of CMC and RL load using PSIM11 software. The control board was emulated using the DLL user block.	For early validation of the Verilog HDL synthesizability, the Quartus 18.1 has been used with SignalTap Logic Analyzer with conjunction with DE10–Lite evaluation board.
experiment	A 5kW CMC with control board based on multicore ADSP–SC589 DSP from Analog Devices and MAX10 Intel FPGA device. The bidirectional power switch was built using two SiC transistors C3M0075120D.	

The paper presents an approach to computations performed in FPGA in one step, during one–cycle, without trigonometry and angles. Thus, the execution time of the PWM duty cycles calculation is atomic and limited only by the critical timing constraints of the FPGA device. The development of a digital structure that performs such an algorithm, in one clock cycle, requires the use of an appropriate modulation method that uses only simple arithmetic operations supported by the Verilog HDL. Moreover, the proposed solution should allow to obtain the maximum voltage transfer ratio and to adjust the angle at the input of the system, which is a characteristic feature of the PWM modulation for CMC [1].

PWM modulation strategies for CMC have been widely reported in literature, as the direct control by Venturini approach [3], [19], [20], scalar control realized according to Roy method [21], and the Space Vector Modulation (SVM) [1], [22]. Other control methods, like hysteresis and Direct Torque Control (DTC), are interesting alternatives [23], [24]. However, the torque ripple in the low–speed region or switching frequency variations according to the change of the motor speed are drawbacks of these approaches. The mentioned methods are not suitable for developing the simplest solution, which should be built from basic digital elements like multiplexes, adders and multipliers. A simplified carrier–based modulator based on the concept of a virtual matrix converter was presented in [25]. The proposed algorithm allows for obtaining the same instantaneous matrix states as the SVM method with a smaller number of calculations. Although the solution represents a more synthetic and systematic approach, this original approach has a major disadvantage. An input displacement angle is permanently equal to zero and cannot be adjusted.

The concept of simplifying and generalizing the PWM modulation algorithm is also presented in publications [26], [27]. As with the previous method, the proposal makes it possible to calculate PWM duty cycles without trigonometry with minimal computational effort. Moreover, the proposed computation scheme allows for the application of various methods of power factor control. Among the described modulation methods, the authors indicated that the Direct Analytic Voltage Pulse Width Modulation (DAV–PWM) is optimal because it allows reaching the maximum voltage transfer ratio equal to 0.866 with the same switch states collection as the SVM modulation. This algorithm has been developed as a sequential code, which contains a program loop for preselection input voltage vectors. Such a program loop has to be eliminated within the atomic and concurrent implementation based on an FPGA device. The paper mainly addresses this issue and proposes certain improvements, which are clarified in section II. The theoretical basis of an improved DAV–PWM modulation algorithm, ready for the HDL conversion, has been presented in the next section. Power electronics simulation, modelling based on the Hardware Description Language (HDL), and Hardware–In–the–Loop (HIL) verification have been presented in section IV. The conducted research path is summarized in Table I. Experimental results are presented in section V. The Verilog HDL code of the improved DAV–PWM algorithm is available as an appendix after the conclusion section.

II. PROPOSAL FOR CHANGES IN THE DAV-PWM

The use of an FPGA chip offers new possibilities to design the computation structure with a short execution time, provided that these algorithms do not use advanced mathematical functions, such as trigonometric functions, and not contain the program loops. Therefore, the computation scheme of the DAV–PWM modulation should be optimised. The most important modifications of the DAV–PWM algorithm are explained in the following section.

• ***The quadrature component generation of an input voltage***

Each input voltage with the pulsation ω_{i} can be expressed as a rotating vector as shown in Fig. 3. For pure sinusoidal input voltages with an amplitude V the $imaginary$ coordinates are just quadrature components. Thus, the analytic signals corresponding to input voltages can be expressed as follows

$$\mathbf{v_i} = V \begin{bmatrix} \cos(\omega_{\mathrm{i}} t) & \sin(\omega_{\mathrm{i}} t) \\ \cos(\omega_{\mathrm{i}} t - 2\pi/3) & \sin(\omega_{\mathrm{i}} t - 2\pi/3) \\ \cos(\omega_{\mathrm{i}} t + 2\pi/3) & \sin(\omega_{\mathrm{i}} t + 2\pi/3) \end{bmatrix} \quad (1)$$

If the input voltages are not perfectly sinusoidal, all coordinates should be determined using Hilbert filter or FFT/DFT based operation [28]–[30], which cannot be easily implemented in FPGA without using an advanced Intellectual Property Core. However, calculations using Clarke's triple transforms, although simple, in the case of asymmetry cause a distortion of the input current [26]. In practice, error signals in the form of DC offsets, glitches, and momentary voltage sags may occur in measurements. Therefore, coordinates can be computed by Double Second Order Generalized Integrator with loop feedback extension functioning as Orthogonal Signal Generator (DSOGI–OSG), shown in Fig. 2, which in the OSG part prevents unexpected resonance and variables overflow [31]–[33]. If processed signal frequency does not have an exact value, another extension of SOGI structure, called the Frequency Locked Loop FLL, may be applied [34]–[36].

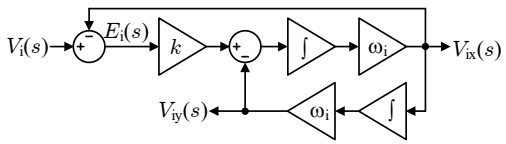


Fig. 2. DSOGI–OSG structure in continuous time–domain.

• ***A simpler approach to the input displacement angle regulation***

According to the concept proposed in papers [26] and [27], an input angle displacement regulation is realised by tilting the trajectory Γ by the desired displacement angle, exactly equal to $\phi_{\rm i}$, as is illustrated in Fig. 3. The modification of the Γ trajectory results in decreasing the voltage transfer ratio q. Thus, reference output voltages can be represented by the following formula

$$\mathbf{v_o} = q \cdot \cos(\phi_{\rm i}) \left[\begin{array}{c} \cos(\omega_{\rm o}) + v_{\rm cm} \\ \cos(\omega_{\rm o} - 2\pi/3) + v_{\rm cm} \\ \cos(\omega_{\rm o} + 2\pi/3) + v_{\rm cm} \end{array} \right] \left[\begin{array}{ccc} 1 & \tan(\phi_{\rm i}) \end{array} \right] \tag{2}$$

where the common–mode signal $v_{\rm cm}$ is expressed as follows

$$\begin{array}{l} v_{\rm cm} = -0.5(\max_{\rm o} + \min_{\rm o}) \\ \max_{\rm o} = \mathrm{MAX}\{\cos(\omega_{\rm o}), \cos(\omega_{\rm o} - 2\pi/3), \cos(\omega_{\rm o} + 2\pi/3)\} \\ \min_{\rm o} = \mathrm{MIN}\{\cos(\omega_{\rm o}), \cos(\omega_{\rm o} - 2\pi/3), \cos(\omega_{\rm o} + 2\pi/3)\}. \end{array} \tag{3}$$

To achieve the maximum voltage transfer ratio, the trajectory Γ should to be shifted to the nearest vertex of the triangle $\Delta_{[1,2,3]}$. According to the origin DAV–PWM algorithm, coordinates of the shift vector are designated by the program loop routine, in which the algorithm selects the best candidate among the input voltage vectors set [26]. This solution can also be improved to meet the optimization requirements. The Gamma Γ modification in equation (2) can be replaced by a formula containing a rotation matrix. Thus, the relation between input and output voltages in CMC may be written in a following general form

$$\mathbf{v_o} \cdot \mathbf{R} = \mathbf{D} \cdot \mathbf{v_i} \tag{4}$$

where

$$\mathbf{R} = \left[\begin{array}{cc} \cos(\phi_{\rm i}) & -\sin(\phi_{\rm i}) \\ \sin(\phi_{\rm i}) & \cos(\phi_{\rm i}) \end{array} \right] \tag{5}$$

and $\mathbf{D}$ is a square matrix that contains all PWM duty cycles

$$\mathbf{D} = \left[\begin{array}{ccc} d_{11} & d_{12} & d_{13} \\ d_{21} & d_{22} & d_{23} \\ d_{31} & d_{32} & d_{33} \end{array} \right] \tag{6}$$

for switches h_{11} – h_{33}. Taking into account the properties of the $\mathbf{R}$ matrix, equation (4) can be finally rewritten as

$$\mathbf{v_o} = \mathbf{D} \cdot (\mathbf{v_i} \cdot \mathbf{R}^{-1}) = \mathbf{D} \cdot \mathbf{v_{iR}} \tag{7}$$

Now, the desired angle of displacement $\phi_{\rm i}$ can be achieved by angular displacement of the input vector collection (1). This result has a significant impact on the optimization

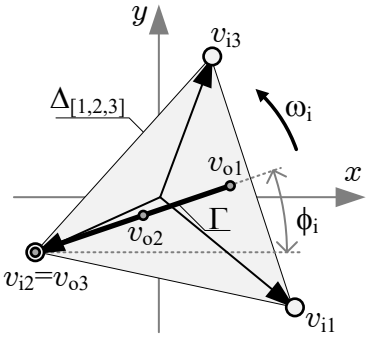


Fig. 3. Regulation of an input power factor in CMC by tilting the trajectory Γ.

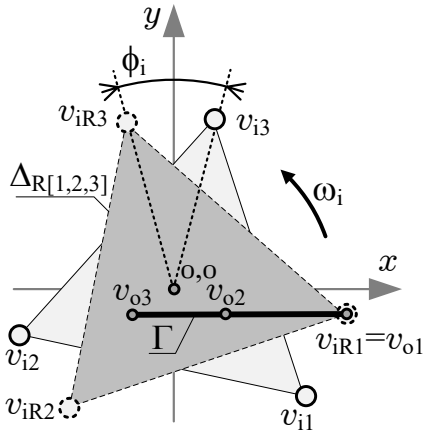


Fig. 4. A new synthesis field $\Delta_{\rm R[1,2,3]}$ after rotation of the original input vectors.

of the origin DAV–PWM algorithm because all calculations can be performed for reference voltage, which always has a zero imaginary component. Hence, the selection of the shift coordinates is simplified and free from an undesired program loop. Reference to the new synthesis field $\Delta_{\rm R[1,2,3]}$ shown in Fig. 4, the shift vector always correspondes to an intermediate vertex between the top and the bottom vertex, which can be immediately selected in a much simpler way using comparators instead of the program loop.

• ***Simplification of the reference output voltage generation***

The trajectory shift operation eliminates the common voltage from equation (2). Therefore, this component can be deleted in the proposed version of the DAV-PWM algorithm. In consequence, only the sinusoidal voltage references can be applied in the algorithm.

III. An improved DAV–PWM modulation algorithm

A schematic diagram of the improved DAV–PWM modulation algorithm is presented in Fig. 5. The input voltage $\{v_{\rm i1}, v_{\rm i2}, v_{\rm i3}\}$ from measurements is converted into analytic signal pairs using DSOGI–OSG or DSOGI–FLL structure. Next, all input vectors are multiplied by the rotation matrix $\mathbf{R}$ (5), which takes arguments – $\cos\phi_{\rm i}$ and $\sin\phi_{\rm i}$ – from the input power factor control routine. Three coordinates pairs for

TABLE II
DEPENDENCE OF THE SHIFT VECTOR COORDINATES v_s, $\max_o$, AND $\min_o$ ON INPUT AND OUTPUT SECTOR NUMBER.

s_{iR} or s_o	v_{sx}	v_{sy}	$\max_o$	$\min_o$
1	$v_{iR2x} - \min_o$	v_{iR2y}	v_{o3x}	v_{o1x}
2	$v_{iR1x} - \min_o$	v_{iR1y}	v_{o2x}	v_{o3x}
3	$v_{iR3x} - \max_o$	v_{iR3y}	v_{o2x}	v_{o1x}
4	$v_{iR3x} - \min_o$	v_{iR3y}	v_{o1x}	v_{o2x}
5	$v_{iR1x} - \max_o$	v_{iR1y}	v_{o3x}	v_{o2x}
6	$v_{iR2x} - \max_o$	v_{iR2y}	v_{o1x}	v_{o3x}

modulating signals

$$\mathbf{v_o} = \begin{bmatrix} v_{o1x} + v_{sx} & v_{sy} \\ v_{o2x} + v_{sx} & v_{sy} \\ v_{o3x} + v_{sx} & v_{sy} \end{bmatrix} \tag{8}$$

are selected according to the input sector s_{iR} and the output sector s_o. Both sectors are directly identified using comparators as shown in Fig. 6 and Fig. 7.

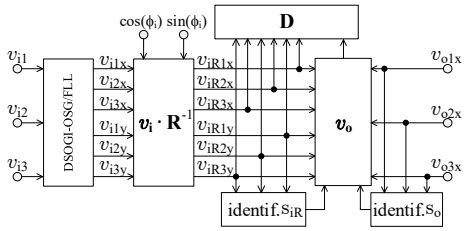


Fig. 5. Schematic diagram of the improved DAV–PWM modulation algorithm.

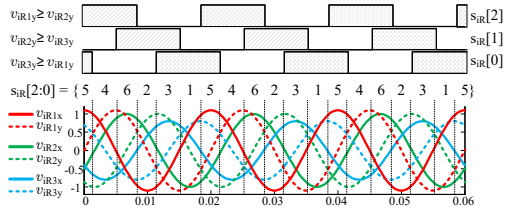


Fig. 6. Identifying the sector of the rotated input vectors using three comparators during an amplitudes asymmetry.

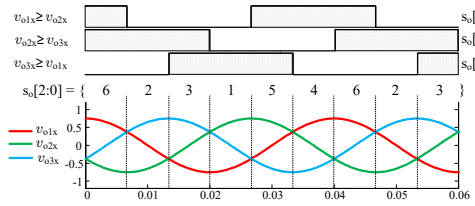


Fig. 7. Identifying the output voltage sector using three comparators.

Dependencies of the shift vector coordinates on the input and output sectors are referred to in Table II. The collection of PWM duty cycles for switches h_{11}, h_{21}, and h_{31} can be calculated without trigonometry and angles using the following formulas

$$d_{11} = \xi \cdot \left| \det \begin{bmatrix} v_{iR2x} - \mathbf{v_o}(1,1) & v_{iR2y} - \mathbf{v_o}(1,2) \\ v_{iR3x} - \mathbf{v_o}(1,1) & v_{iR3y} - \mathbf{v_o}(1,2) \end{bmatrix} \right| \tag{9}$$

TABLE III
THE PWM DUTY CYCLE MATRICES $\mathbf{D}$ WITHIN AN INPUT AND OUTPUT VOLTAGE SECTORS IN DAV–PWM MODULATION.

s_{iR} \ s_o	4,6 (1,3)	2,3 (4,5)	1,5 (2,6)
2(5)	$\begin{bmatrix} 1 & d_{12} & d_{13} \\ 0 & d_{22} & d_{23} \\ 0 & d_{32} & d_{33} \end{bmatrix}$	$\begin{bmatrix} d_{11} & 1 & d_{13} \\ d_{12} & 0 & d_{23} \\ d_{13} & 0 & d_{33} \end{bmatrix}$	$\begin{bmatrix} d_{11} & d_{12} & 1 \\ d_{12} & d_{22} & 0 \\ d_{13} & d_{32} & 0 \end{bmatrix}$
1(6)	$\begin{bmatrix} 0 & d_{12} & d_{13} \\ 1 & d_{22} & d_{23} \\ 0 & d_{32} & d_{33} \end{bmatrix}$	$\begin{bmatrix} d_{11} & 0 & d_{13} \\ d_{21} & 1 & d_{23} \\ d_{31} & 0 & d_{33} \end{bmatrix}$	$\begin{bmatrix} d_{11} & d_{12} & 0 \\ d_{21} & d_{22} & 1 \\ d_{31} & d_{32} & 0 \end{bmatrix}$
3(4)	$\begin{bmatrix} 0 & d_{12} & d_{13} \\ 0 & d_{22} & d_{23} \\ 1 & d_{32} & d_{33} \end{bmatrix}$	$\begin{bmatrix} d_{11} & 0 & d_{13} \\ d_{21} & 0 & d_{23} \\ d_{31} & 1 & d_{33} \end{bmatrix}$	$\begin{bmatrix} d_{11} & d_{12} & 0 \\ d_{21} & d_{22} & 0 \\ d_{31} & d_{32} & 1 \end{bmatrix}$

$$d_{21} = \xi \cdot \left| \det \begin{bmatrix} v_{iR1x} - \mathbf{v_o}(1,1) & v_{iR1y} - \mathbf{v_o}(1,2) \\ v_{iR3x} - \mathbf{v_o}(1,1) & v_{iR3y} - \mathbf{v_o}(1,2) \end{bmatrix} \right| \tag{10}$$

$$d_{31} = 1 - d_{11} - d_{21} \tag{11}$$

where $\det$ means the determinant of the matrix 2×2, and

$$\xi = \left| \det \begin{bmatrix} v_{iR2x} - v_{iR1x} & v_{iR2y} - v_{iR1y} \\ v_{iR3x} - v_{iR1x} & v_{iR3y} - v_{iR1y} \end{bmatrix} \right|^{-1} \tag{12}$$

Others PWM duty cycles, in the second and third row of (8), can be computed analogously. The PWM duty cycle matrices $\mathbf{D}$ within an input s_{iR} and output s_o voltage sectors in DAV–PWM modulation are summarized in Table III. The $\mathbf{D}$ matrix consists of nine duty cycles $d_{11} - d_{33}$, which are transformed into the sequence of logical signals for switches state control. These sequences are usually generated by the specialized digital structure based on counters and comparators according to the selected commutation strategy in CMC [37]–[41]. The Cyclic Venturini approach and the 4–step commutation strategy have been chosen [5].

IV. POWER ELECTRONICS SIMULATION, HDL MODELLING, HIL VERIFICATION.

This section presents results obtained during the functional simulation in PSIM11 software, behavioural modelling of the Hardware Description Language (HDL) using ModelSim Intel FPGA environment, and the Hardware–In–the–Loop (HIL) verification using Quartus Intel FPGA software with Signal Tap Logic Analyzer (STLA) tool.

• ***Simulation and switch state sequences comparison for DAV–PWM and SVM***

The PSIM environment was used to simulate CMC control and verify the algorithm compiled as the user DLL block, which is written in C–language. The proposed improved algorithm maintains the important properties of DAV–PWM modulation proposed in [26]. The obtained sequences of switch states, including the waveforms of line–to–line voltages, remain unchanged. An input voltage amplitude asymmetry or phase angle disturbance change the shape and area of the synthesis field limiting the value of the voltage transfer ratio q. However, during operation with a unity power factor, currents on both sides of the converter are sinusoidal, as can be seen in Fig. 8 where three selected input conditions for RL load type are presented. The article proposes a direct modulation algorithm, in which the switch states are not explicitly declared as in the conventional SVM modulation method. Table IV presents

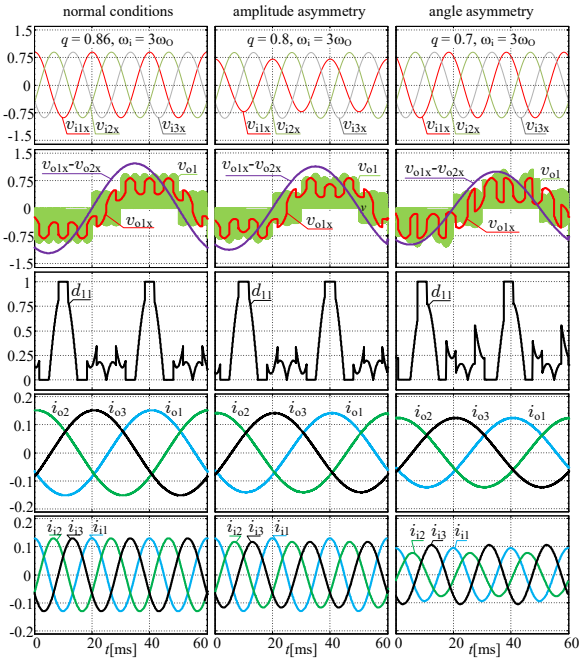


Fig. 8. Three selected source voltage conditions during operation with a unity power factor at the input – simulation using PSIM11 software.

TABLE IV
THE SWITCH STATES COLLECTION FOR SVM METHOD.

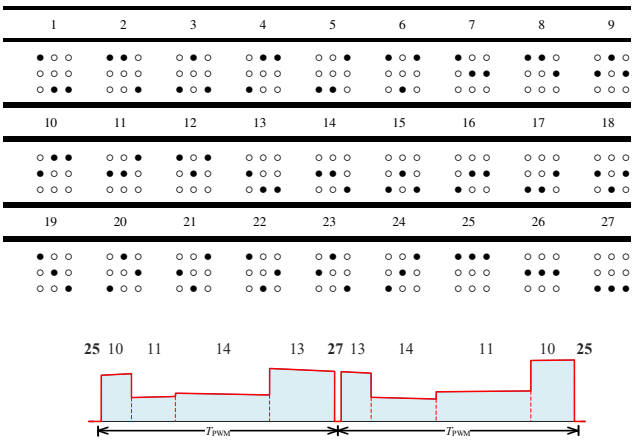


Fig. 9. Two periods of the load voltage for the 10–switch–double–sided modulator for conventional SVM method.

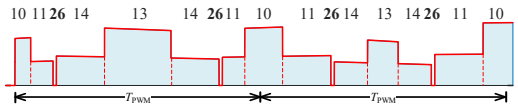


Fig. 10. Two periods of the load voltage for 8–switch–double–sided switch states sequence for SVM and DAV–PWM modulations.

all switch states of CMC. Black dots represent the active switches in the matrix panel. Several modulation techniques are compared in paper [42] and analyzed in [43]. Among the described switch state sequences two of them can be distinguished: 10–switch double–sided shown in Fig. 9, and low–distortion 8–switch sequence illustrated in Fig. 10. The

TABLE V
DECODED SVM SWITCHING SEQUENCES FOR DAV–PWM MODULATION WITH CYCLIC VENTURINI SCHEME.

	s_o		
s_{iR}	6(1)	2(5)	3(4)
5(2)	25,02,01,02,25,08,07,08,25	25,02,03,02,25,08,09,08,25	25,10,09,10,25,04,03,04,25
4(3)	27,01,02,01,27,13,14,13,27	27,03,02,03,27,15,14,15,27	27,03,04,03,27,15,16,15,27
6(1)	26,11,10,11,26,14,13,14,26	26,11,12,11,26,14,15,14,26	26,07,12,07,26,16,15,16,26
2(5)	25,04,05,04,25,10,11,10,25	25,12,11,12,25,06,05,06,25	25,06,01,06,25,12,07,12,25
3(4)	27,05,04,05,27,17,16,17,27	27,05,06,05,27,17,18,17,27	27,01,06,01,27,13,18,13,27
1(6)	26,07,08,07,26,16,17,16,26	26,18,17,18,26,09,08,09,26	26,18,13,18,26,09,10,09,26

switch states for DAV–PWM modulation can be derived using the switch state parser connected with all 9 control signals $h_{11} - h_{33}$. The state parser is a Matlab script, which operates on the PSIM data saved in CSV file format. Decoded SVM switching sequences for DAV–PWM modulation with Cyclic Venturini scheme are collected in Table V. The following major conclusions can be formulated based on the switch state sequences comparison:

- both, the SVM method and DAV–PWM use the same active vectors in their input and output voltage sectors,
- the construction of the switch state sequences in the DAV–PWM method is identical to the sequence for SVM shown in Fig. 10,
- the proposed DAV–PWM allows for reducing the harmonic distortion by having two zero vectors per period as reported in [42], but only the approach illustrated in Fig. 9 permits for reduction of switch operation frequency,
- tabularizing the switch state sequences is not necessary for a carrier–based modulation such as DAV–PWM.

• ***HDL compilation***

The ModelSim software was applied for modelling the digital module of the PWM duty cycle computation, in which the behavioural equivalent of the C–language developed DAV–PWM modulation had been coded using the Verilog HDL. The ModelSim simplified simulation diagram is shown in Fig. 11. This software is usually dedicated for digital core or module simulation but here that software has been used for developing the matrix converter control module. The fixed–point Q15 format arithmetic, in comparison with the single–precision format, often permits for developing very fast algorithms without pipelines and recursive operations. Continuous signals, such as input voltages, can be represented by the large tables of 16–bit values. The discreet sampling time was generated by the counter with auto–reload. An input displacement angle has been expressed as a sin–cos pair expressed by constant Q15 values. For simulation purpose only, the Cyclic–Venturini switching strategy was developed in Verilog HDL using non–synthesizable modelling based on the signal delay command. This Verilog HDL piece of code is intentionally depicted in the drawing. Selected electrical waveforms, sectors, and PWM duty cycles in the analogue form, modelled using ModelSim simulation environment, are shown in Fig. 12. The load current was modelled using the first–order Infinite Impulse Response filter (IIR). All line–to–line load voltages were generated using the signal switching approach controlled by the input sector number.

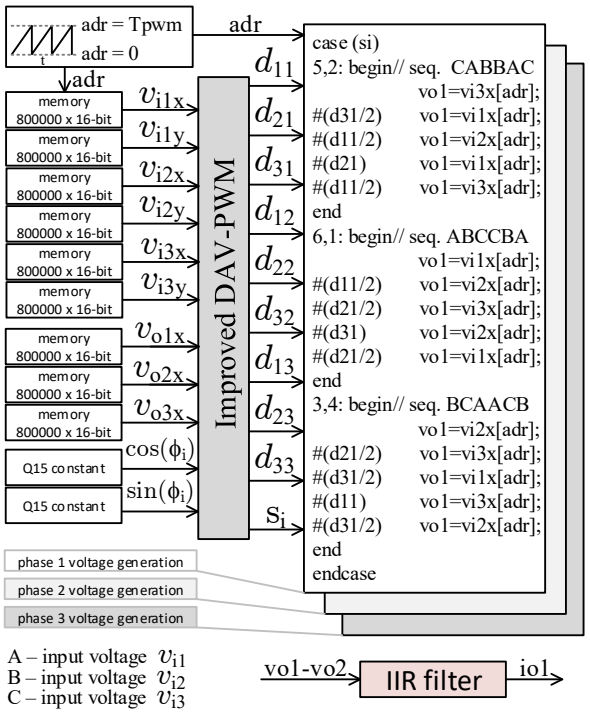
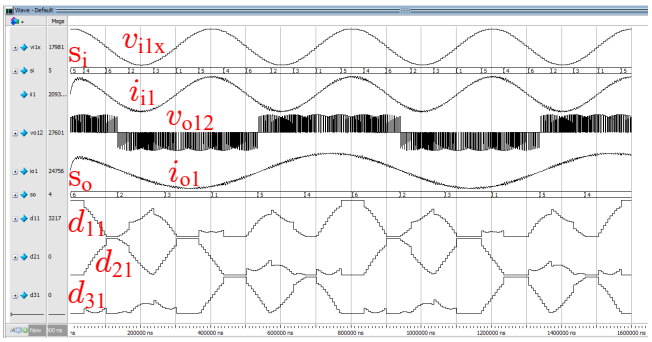
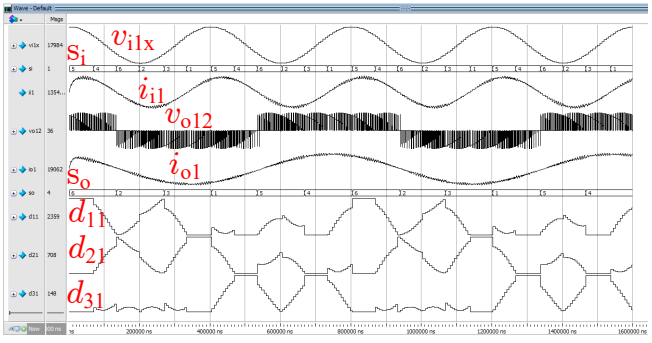


Fig. 11. ModelSim simplified simulation diagram.



(a)



(b)

Fig. 12. Waveforms in the analogue form obtained by modelling of DAV–PWM algorithm written in Verilog HDL using ModelSim environment: (a) $q = 0.86$, $\phi_i = 0$, $\omega_i = 2\omega_o$, (b) $q = 0.75$, $\phi_i = -\pi/6$, $\omega_i = 2\omega_o$.

- ***HIL verification***

For early validation of the Verilog HDL project file synthesizability, the Quartus 18.1 with Signal Tap Logic Analyzer was used. An evaluation board DE10–Lite was used during the HIL test. Two debugging tools were used during the validation stage. As shown in Fig. 13, the In–System Sources and Probes tool was used to give phase and frequency of signals generated by CORDIC Numerically Controlled Oscillators (NCO), while the Signal Tap Analyzer tool allowed to visualize and record of the selected signals in real–time. Fig. 14 shows an improved DAV–PWM algorithm signals during the debug session using the Signal Tap Logic Analyzer for $\omega_i/\omega_o = 2.67$, $f_s = 1$ MHz, and $q = 0.8$. The proposed PWM duty cycle computation module resource utilization is presented in Table VI.

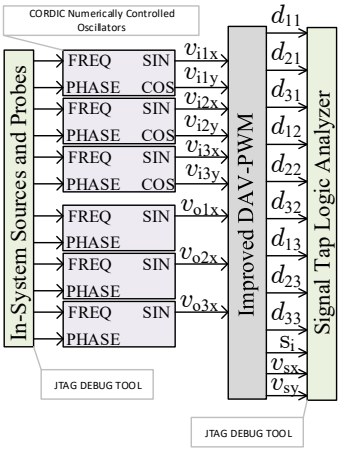


Fig. 13. Early validation scheme of the improved DAV–PWM algorithm developed in Verilog HDL.

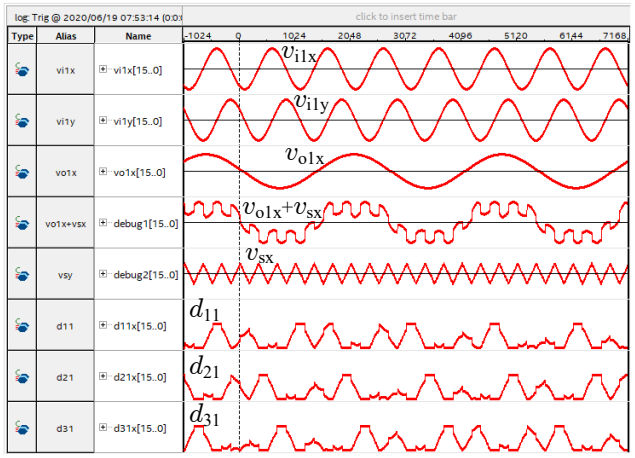


Fig. 14. Improved DAV–PWM algorithm signals during the debug session using the Signal Tap Logic Analyzer.

TABLE VI
AN IMPROVED DAV–PWM DUTY CYCLE COMPUTATION MODULE RESOURCE UTILIZATION.

resource name	utilization
Logic Cells	1454
Dedicated Logic Register	211
DSP Elements	40
DSP 18x18 multipliers	20

V. Experimental results

A 5kW CMC with the control board, shown in Fig. 15, based on multicore ADSP–SC589 DSP from Analog Devices and MAX10 Intel FPGA device were used during experiment stage. The bidirectional power switch was build using two SiC transistors C3M0075120D. The schematic diagram of the experiment configuration is shown in Fig. 16. The block diagram of performed computation by FPGA device during an experiment is presented in Fig. 17. Q15 symbol indicates digital structures based on fixed–point arithmetic, while SP means the floating–point IP core used for time cycles scaling. This element is needed to preserve constant modulation frequency. The modulation period was $100\mu s$, while algorithm computation in Q15 blocks was accomplished through $100ns$ positive clock pulse.

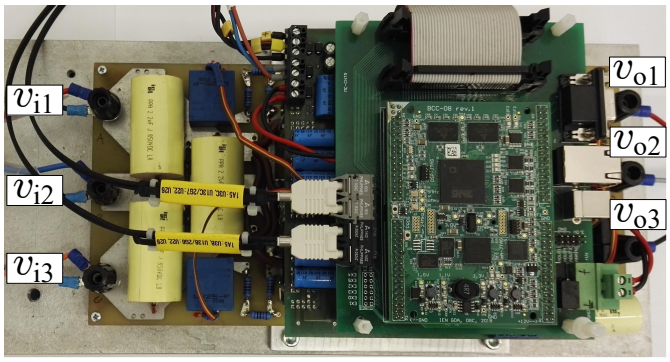


Fig. 15. A 5kW matrix converter with the DSP–FPGA control board.

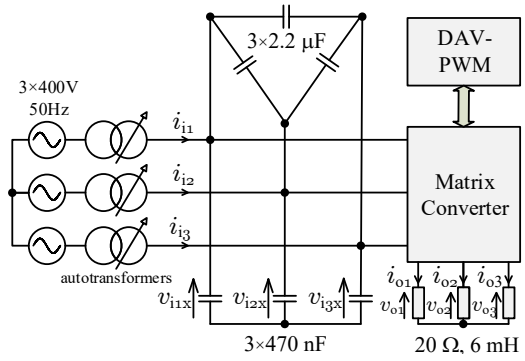


Fig. 16. The schematic diagram of the experiment configuration.

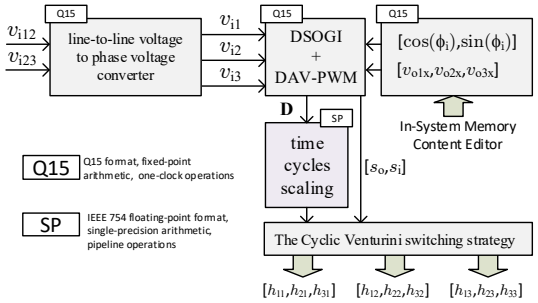
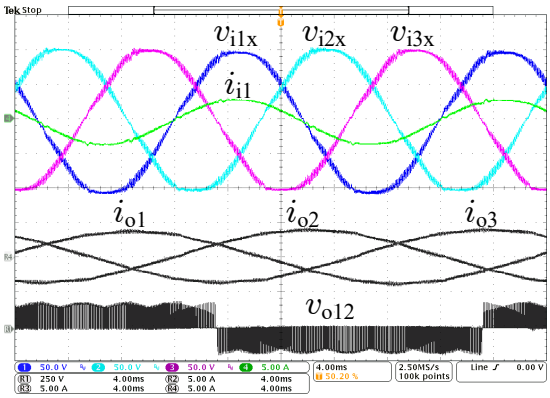
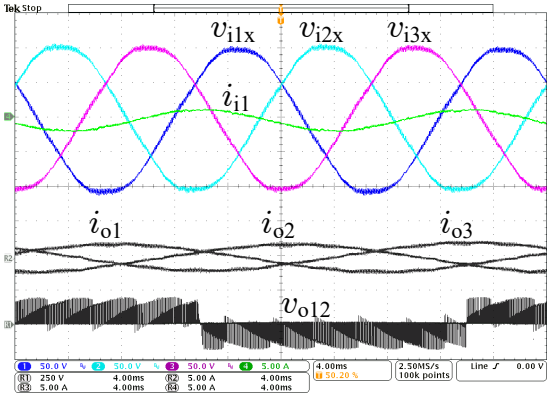


Fig. 17. The block diagram of performed computation by FPGA device during an experiment.

The waveforms for the normal operation with a zero displacement angle value ϕ_i and modulation with $\phi_i = -\pi/4$ are shown in Fig. 18. The proposed modulation method can be used in the case of supply voltage asymmetry. Despite such conditions, the input currents in each phase are sinusoidal. Experimental results for a significant asymmetry of input voltages $\{V_{i1} = 75V,\ V_{i2} = 100V,$ and $V_{i3} = 125V\}$, are shown in Fig. 19.



(a) $q = 0.86$, $\phi_i = 0$



(b) $q = 0.6$, $\phi_i = -\pi/4$

Fig. 18. Experimental results for $\omega_o/\omega_i = 0.5$ and symmetric input amplitudes for: (a) unity power factor, (b) reactive power generation.

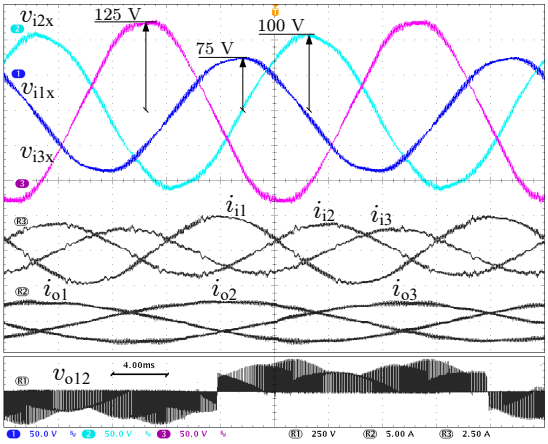


Fig. 19. An output and input currents for asymmetrical input voltage source for DAV–PWM modulation: $q = 0.55$, $\omega_o/\omega_i = 0.5$.

VI. Conclusion

The proposed computation scheme of PWM duty cycles does not require trigonometry operation and angles resulting in simplistic matrix converter control algorithm. All calculation is based on basic arithmetic operations that can be easily implemented in the FPGA within one clock tact. The proposed general direct modulation is an SVM equivalent when the low–distortion 8–switch double–sided modulator is applied. However, compared with SVM, the proposed DAV–PWM algorithm is much simpler. The comparision of the SVM and the improved DAV–PWM is presented in Table VII. With regard to the solution presented in [26], the following benefits were obtained, as presented in Table VIII.

TABLE VII
THE COMPARISION OF THE SVM AND THE IMPROVED DAV–PWM.

	SVM	DAV–PWM
maximum voltage transfer ratio q if $\cos(\phi_i) = 1$	0.866	0.866
an input angle control	yes	yes
the q dependency from the input angle ϕ_i	$q = 0.866 \cdot \cos(\phi_i)$	$q = 0.866 \cdot \cos(\phi_i)$
trigonometric functions in the formulas for the PWM duty cycles	yes	no
implementation in FPGA using HDL	difficult	simple
execution time of the PWM duty cycle	several hundred clock cycles	one clock
switch states table	switch state sequences are pre–selected and placed in the look–up table	tabularizing of the switch state sequences is not needed
ready for hybrid modulation	no – this algorithm is hermetic and the modulation can not be modified in the fly during the device is running	yes – it is enough to modify the reference voltage waveform
ready for multiphase output (5 or more terminals)	no – both, the optimal switch state sequences and the PWM duty cycles formulas must be elaborated again	yes – a new output phase is represented by the same commutation cell, an only new double multiplier block is required for the PWM duty cycles computing
PLL requirements	yes – for the indication of the output voltage sectors and also the input current sectors	no – there is no PLL needed

The discussed approach is suitable and more robust for FPGA implementation than a conventional approach such as SVM. For a better understanding of the solution developing process, the paper also briefly describes the HDL project compilation stage and HIL verification. Moreover, an early functional simulation of the CMC control can be performed using the ModelSim software. Finally, the solution can be represented only by one Verilog HDL file, thus an export to another FPGA vendor platform is not complicated and is not necessary to explicitly predefined the semiconductor switch states as in the SVM methods. Each converter cell is controlled independently in a direct way. This is especially convenient when the number of outputs is greater than the standard three. Simulation files are provided in the IEEE DataPort portal to increase understanding of the paper. The first file is a script for the Matlab environment, which is a presentation of the proposed modulation. The second file contains the testbench of the proposed Verilog HDL modulator [44].

TABLE VIII
THE COMPARISION OF THE PREVIOUS [26] AND THE IMPROVED DAV–PWM ALGORITHMS.

	previous	present
maximum voltage transfer ratio q if $\cos(\phi_i) = 1$	0.866	0.866
an input angle control method	the reference voltages' trajectory Γ slope	based on the input voltage rotation matrix $\mathbf{R}$
the extraction method of the quadrature components of the input voltages	the Clarke transformation on each natural axis a–b–c	using the DSOGI–OSG structure
the occurrence of program loops in the algorithm	yes – for selection of the best reference voltage trajectory position inside the synthesis field	no program loop
ready to use in	DSP and processors only using the C-code	C-code and HDL-code allow the use in both, DSP and FGPA based application
shortening the calculation time	—	$\approx 30\%$ in DSP, one–cycle operation in the FPGA device

Appendix

The Verilog HDL code of the improved DAV–PWM algorithm.

```
//module definition
module ImprovedDAVPWM #(parameter MSB=33,LSB=18)
(
 input iCLK,
 input signed [15:0] vi1x,vi2x,vi3x,vi1y,vi2y,vi3y,
 input signed [15:0] vo1x,vo2x,vo3x,R_cos,R_sin,
 output reg[15:0] d11,d21,d31,d12,d22,d32,d13,d23,d33,sum,
 output reg [2:0] si,so
);
//x-coordinate difference
reg signed [16:0] vi1x_vo1x,vi2x_vo1x,vi3x_vo1x;
reg signed [16:0] vi1x_vo2x,vi2x_vo2x,vi3x_vo2x;
reg signed [16:0] vi1x_vo3x,vi2x_vo3x,vi3x_vo3x;
//y-coordinate difference
reg signed [16:0] vi1y_py,vi2y_py,vi3y_py;
//the real line-to-line voltage
reg signed [16:0] vi1x_vi2x,vi2x_vi3x,vi3x_vi1x;
//the imaginary line-to-line voltage
reg signed [16:0] vi1y_vi2y,vi2y_vi3y,vi3y_vi1y;
//minimum and maximum output voltage
reg signed [15:0] min_vox,max_vox;
//shift vector coordinates
reg signed [15:0] vsx,vsy;
//input vector coordinates after rotation
reg signed [31:0] viR1xx,viR2xx,viR3xx,viR1yy,viR2yy,viR3yy;
//rescaled input vector coordinates
reg signed [15:0] viR1x,viR2x,viR3x,viR1y,viR2y,viR3y;
//shifted real coordinates of output voltages
reg signed [15:0] vo1xx,vo2xx,vo3xx;
//rational functions for matrix D calc.
reg signed [33:0] d11w,d21w,d31w,d12w,d22w,d32w,d13w,d23w,d33w,d00w;
//absolute rational functions for matrix D calc.
reg signed [33:0] d11ww,d21ww,d31ww,d12ww,d22ww,d32ww,d13ww,d23ww,d33ww,d00ww;

//behavioural description
always @(posedge iCLK)
begin
//output voltage sector calculation
so[2]=(vo1x >= vo2x)? 1:0; so[1]=(vo2x >= vo3x)? 1:0; so[0]=(vo3x >= vo1x)? 1:0;
//maximum output voltage
case(so)
1: max_vox = vo3x;2: max_vox = vo2x;3: max_vox = vo2x;
4: max_vox = vo1x;5: max_vox = vo3x;6: max_vox = vo1x;
endcase
//minimum output voltage
case(so)
1: min_vox = vo1x;2: min_vox = vo3x;3: min_vox = vo1x;
4: min_vox = vo2x;5: min_vox = vo2x;6: min_vox = vo3x;
endcase
//rotation of the input vectors
viR1xx = vi1x * R_cos - vi1y * R_sin; viR1yy = vi1x * R_sin + vi1y * R_cos;
viR2xx = vi2x * R_cos - vi2y * R_sin; viR2yy = vi2x * R_sin + vi2y * R_cos;
viR3xx = vi3x * R_cos - vi3y * R_sin; viR3yy = vi3x * R_sin + vi3y * R_cos;
//scaling of the rotated input vectors
viR1x=viR1xx[30:15]; viR1y=viR1yy[30:15]; viR2x=viR2xx[30:15];
viR2y=viR2yy[30:15]; viR3x=viR3xx[30:15]; viR3y=viR3yy[30:15];
//input voltage sector calculation
si[2]=(viR1y>=viR2y)? 1:0; si[1]=(viR2y>=viR3y)? 1:0; si[0]=(viR3y>=viR1y)? 1:0;
//y-coordinate of shift vector
case(si)
5,2: vsy=viR1y; 4,3: vsy=viR3y; 6,1: vsy=viR2y;
endcase
//x-coordinate of shift vector
case(si)
6: vsx=viR2x-max_vox; 1: vsx=viR2x-min_vox; 3: vsx=viR3x-max_vox;
4: vsx=viR3x-min_vox; 5: vsx=viR1x-max_vox; 2: vsx=viR1x-min_vox;
endcase
//the real line-to-line input voltage
vi1x_vi2x=viR1x - viR2x; vi2x_vi3x=viR2x - viR3x; vi3x_vi1x=viR3x - viR1x;
//the imaginary real line-to-line input voltage
vi1y_vi2y=viR1y - viR2y; vi2y_vi3y=viR2y - viR3y; vi3y_vi1y=viR3y - viR1y;
```

```
//shifted the real coordinates of output voltages
vo1xx=vo1x+vsx; vo2xx=vo2x+vsx; vo3xx=vo3x+vsx;
//x-coordinate difference
vi1x_vo1x=viR1x - vo1xx; vi2x_vo1x=viR2x - vo1xx; vi3x_vo1x=viR3x - vo1xx;
vi1x_vo2x=viR1x - vo2xx; vi2x_vo2x=viR2x - vo2xx; vi3x_vo2x=viR3x - vo2xx;
vi1x_vo3x=viR1x - vo3xx; vi2x_vo3x=viR2x - vo3xx; vi3x_vo3x=viR3x - vo3xx;
//y-coordinate difference
vi1y_py=viR1y - vsy; vi2y_py=viR2y - vsy; vi3y_py=viR3y - vsy;
//rational functions
d11w=(vi2x_vo1x*vi3y_py)-(vi3x_vo1x*vi2y_py);
d21w=(vi3x_vo1x*vi1y_py)-(vi1x_vo1x*vi3y_py);
d31w=(vi1x_vo1x*vi2y_py)-(vi2x_vo1x*vi1y_py);
d12w=(vi2x_vo2x*vi3y_py)-(vi3x_vo2x*vi2y_py);
d22w=(vi3x_vo2x*vi1y_py)-(vi1x_vo2x*vi3y_py);
d32w=(vi1x_vo2x*vi2y_py)-(vi2x_vo2x*vi1y_py);
d13w=(vi2x_vo3x*vi3y_py)-(vi3x_vo3x*vi2y_py);
d23w=(vi3x_vo3x*vi1y_py)-(vi1x_vo3x*vi3y_py);
d33w=(vi1x_vo3x*vi2y_py)-(vi2x_vo3x*vi1y_py);
d00w=(vi1x_vi2x*vi3y_vi1y)-(vi1y_vi2y*vi3x_vi1x);
//their absolute value
d00ww = (d00w<0) ? -d00w : d00w; d11ww = (d11w<0) ? -d11w : d11w;
d21ww = (d21w<0) ? -d21w : d21w; d31ww = (d31w<0) ? -d31w : d31w;
d12ww = (d12w<0) ? -d12w : d12w; d22ww = (d22w<0) ? -d22w : d22w;
d32ww = (d32w<0) ? -d32w : d32w; d13ww = (d13w<0) ? -d13w : d13w;
d23ww = (d23w<0) ? -d23w : d23w; d33ww = (d33w<0) ? -d33w : d33w;
//PWM duty cycles update
sum = d00ww[MSB:LSB];
d11 = d11ww[MSB:LSB]; d21 = d21ww[MSB:LSB]; d31 = d31ww[MSB:LSB];
d12 = d12ww[MSB:LSB]; d22 = d22ww[MSB:LSB]; d32 = d32ww[MSB:LSB];
d13 = d13ww[MSB:LSB]; d23 = d23ww[MSB:LSB]; d33 = d33ww[MSB:LSB];
end
endmodule
```

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