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Ladder-Based Synthesis and Design of Low-Frequency Buffer-Based CMOS Filters

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Abstract: Buffer-based CMOS filters are maximally simplified circuits containing as few transistors as possible. Their applications, among others, include nano to micro watt biomedical sensors that process physiological signals of frequencies from 0.01 Hz to about 3 kHz. The order of a buffer-based filter is not greater than two. Hence, to obtain higher-order filters, a cascade of second-order filters is constructed. In this paper, a more general method for buffer-based filter synthesis is developed and presented. The method uses RLC ladder prototypes to obtain filters of arbitrary orders. In addition, a set of novel circuit solutions with ultra-low voltage and power are proposed. The introduced circuits were synthesized and simulated using 180-nm CMOS technology of X-FAB. One of the designed circuits is a fourth-order, low-pass filter that features: 100-Hz passband, 0.4-V supply voltage, power consumption of less than 5 nW, and dynamic range above 60 dB. Moreover, the total capacitance of the proposed filter (31 pF) is 25% lower compared to the structure synthesized using a conventional cascade method (40 pF).

Keywords: buffer-based filters; low-frequency filters; biomedical filters; analogue filters; CMOS filters; low-power analogue circuits; analogue circuits

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1. Introduction

Buffer-based analogue filters are in fact unity-gain amplifiers (i.e., buffers, followers) characterized by a bandwidth that is limited to the required frequency. For example, a simple two-stage Miller operational amplifier can be converted to a filter when it is configured as a unity-gain amplifier by closing a negative feedback loop. In this case, the limited bandwidth is due to Miller compensation, which results in a low-pass transmittance with one dominant pole, i.e., a first-order low-pass filter. Synthesis of a second-order response is also possible, however, only for certain classes of buffers—for instance a few variants of source followers including undamped [1,2], super [3], flipped [4–6], and ones that belong to other classes [7–10]. The advantage of the buffer-based filter realizations is a substantially lower number of transistors compared to traditional Operational Transconductance Amplifier Capacitor (OTA-C) structures [11–14] since a single transistor or a differential pair replaces the entire OTA. Consequently, the buffer-based filters are referred to as "transistorized" filters [6,15]. The reduced number of transistors decreases power and noise, whereas a simplified circuitry allows for an operation with supply voltage being as low as 0.3 V [9]. The buffer-based, transistorized filters are used for low power and low voltage applications in high frequency range [2–5,15], as well as for low-frequency, ultra-low power bioelectrical sensors [1,6–10].

Realizations of buffer-based filters reported in the literature tend to be "individual" and down-to-top, as they start from a transistor-level circuit and end at Laplace transmittance. A typical design of a biquadratic structure is as follows. First, a potential candidate (i.e., a buffer) for filter realization is selected. Next, two capacitors are connected to internal nodes of a buffer's transistor-level circuit. Then, an equivalent OTA-C (Gm-C) schematic is extracted, and the Laplace transmittance is derived. Finally, if the transmittance is found to

be desirable, the buffer circuit parameters (transistor transconductances, node capacitances, etc.) are selected to meet the required filter parameters. Assuming higher-order filter is needed, it is constructed as a cascade of biquadratic cells.

In this paper, a systematic approach to the synthesis of buffer-based filters is proposed. It originates from the traditional and well-developed top-to-down method that exploits RLC ladder to prototype an OTA-C (G_m-C) filter structure [11,16]. In the final stage of the synthesis, the G_m-C schematic is converted onto the transistor-level circuit, which permits synthesis of "transistorized" filters of any order. In addition to the proposed synthesis method, new transistor-level designs of low-frequency filters operating at 0.4 V supply voltage are also introduced. Two examples of fourth-order, low-pass, 100-Hz filters based on using both the conventional cascade method and the proposed ladder-based approach are presented. The introduced design framework reduces the total filter capacitance, which is an important advantage when integrating low-frequency filters on a chip.

2. Synthesis Method

The foundation of the proposed synthesis of buffer-based filters is based on a certain analogy between a unity-gain buffer and an OTA-C filter obtained from a single-resistance terminated ladder prototype. The details are provided below.

2.1. The Analogy

Figure 1a shows a second-order, low-pass ladder filter terminated by a single resistor. At low frequencies, in the ladder passband, the inductor L_{2P} and the capacitor C_{1P} represent a short and an open circuit, respectively. Consequently, the output voltage V_{out} is equal to the input V_{in}, and the passband voltage gain is 1 V/V.

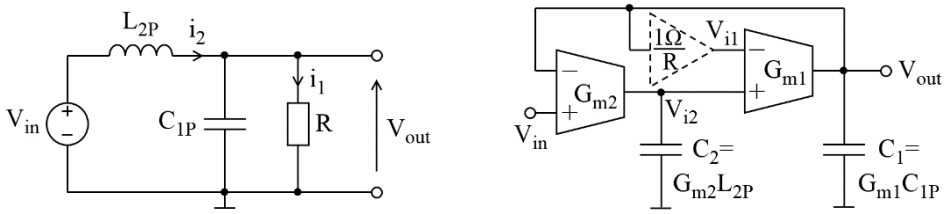

Figure 1. Second-order low-pass filter: (**a**) single-resistance terminated ladder prototype; (**b**) OTA- C (Gm-C) realization.

Figure 1b presents the OTA-C filter obtained from the ladder of Figure 1a using the conventional state variable method (inductor currents and capacitor voltages are expressed by the corresponding nodal voltages in the OTA-C filter [16]). At low frequencies, the capacitors C_1 and C_2 can be treated as open circuits. OTAs are characterized by a high open-loop voltage gain (due to $G_m >> G_o$, G_o is the output conductance), thus the use of negative feedback loops results in virtual short circuits between positive (+) and negative (−) inputs of OTAs. Consequently, at low frequencies, the output voltage of the OTA-C filters is equal to the input voltage ($V_{out} = V_{in}$) resulting in a passband gain of 1 V/V. The input resistance of the structure of Figure 1b increases to infinity and the output resistance decreases to zero at low frequencies. Therefore, the considered structure is in fact a unity-gain amplifier/buffer with bandwidth limited by the capacitances C_1 and C_2. The Laplace transfer function of the filters depicted in Figure 1a,b is

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\omega_0^2}{s^2 + s\omega_0/Q + \omega_0^2} = \frac{1}{s^2 L_{2P}C_{1P} + sL_{1P}/R + 1} = \frac{G_{m1}G_{m2}/(C_1C_2)}{s^2 + sG_{m1}/(C_1R) + G_{m1}G_{m2}/(C_1C_2)} \quad (1)$$

where $\omega_0 = 2\pi f_0$ is so-called a natural frequency, and Q denotes a quality factor.

Note that the voltage amplifier characterized by the gain of 1 Ω/R (V/V) is usually not shown in schematic diagrams because R is typically 1 Ω. However, here this amplifier is used for analyses derived in subsequent sections of this work.

OTA-C filters of higher orders also feature the analogy to unity-gain buffers when synthesized from RLC ladders terminated by single resistance. An example fourth-order filter is considered in Section 5.

2.2. Lossless and Lossy Integrator Circuits

Based on the example circuit of Figure 1b it can be observed that the OTA-C filter requires both lossless and lossy integrators. In general, a second-order filter requires at least one set of such components. In the filter of Figure 1b, the lossless circuit is represented using an open-loop OTA of G_{m2}, whereas the lossy circuit with the closed-loop OTA of G_{m1}. As mentioned earlier, a unity-gain buffer made of the Miller amplifier (Figure 2a, [17]) cannot be used for synthesis of a biquadratic filter, because its OTA-C equivalent schematic does not contain a lossy integrator. In fact, the circuit in Figure 2a features the second-order characteristic (1), but with Q increasing to infinity.

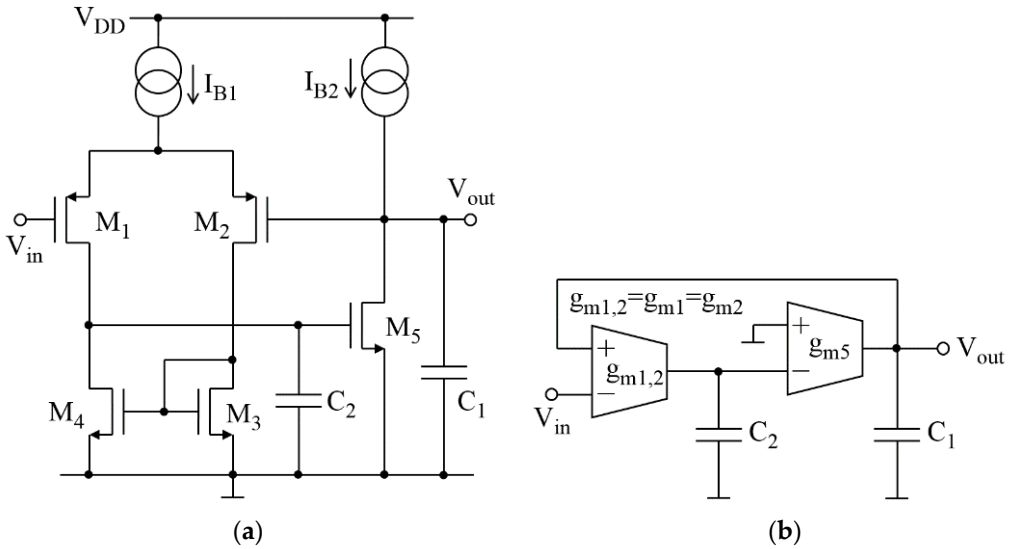

Figure 2. Example of a unity-gain buffer which cannot realize a second-order filter: (**a**) transistor-level circuit; (**b**) OTA-C (Gm-C) equivalent circuit.

The buffer-based biquad realizations reported in the literature contain lossless and lossy integrators. One should emphasize that the equivalent OTA-C schematics of these biquads may differ from the circuit in Figure 1b. For example, a closed-loop OTA (i.e., a lossy circuit) can be placed at the filter input [6,8,9]. Such reverse OTA-C topologies can also be obtained from ladders with single-resistance termination. The first method exploits the bilateral nature of ladders, i.e., the ladder of Figure 1a can be driven in a current mode from its output (V_{out}) side leading to the reciprocal OTA-C structures [18]. Alternatively, a different type of single-resistance terminated ladder that has a resistor on its input can be used [19]. To make the work concise, the synthesis examples are limited to conventional ladder configurations that are terminated with an output resistor, as shown in Figure 1a.

The transistorized solutions for lossless and lossy integrators are presented in the next section.

3. Implementation of Integrator Circuits

3.1. Proposed Lossless Integrator

The proposed lossless integrator is depicted in Figure 3a. It comprises a standard differential amplifier (transistors M_1–M_4), and a floating integrating capacitor (C). C_{par1} and C_{par2} are the main parasitic capacitances.

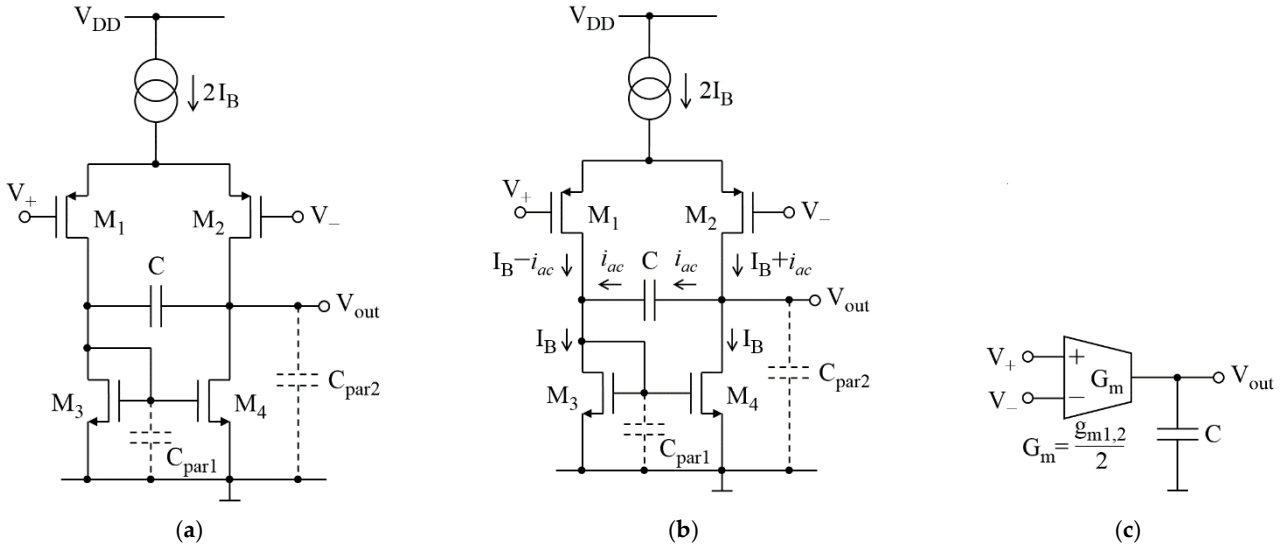

Figure 3. Proposed lossless integrator: (**a**) transistor-level circuit; (**b**) the flow of currents under conditions C_{par1} << C, C_{par2} << C, and $C_{par1} \geq C_{par2}$; (**c**) equivalent OTA-C (Gm-C) diagram. The transconductance $g_{m1,2}$ means $g_{m1,2} = g_{m1} = g_{m2}$.

The transfer function of the integrator in Figure 3a is given as

$$\frac{V_{out}(s)}{(V_+ - V_-)(s)} = \frac{g_{m1,2}}{2} \cdot \frac{1}{sC + sC_{par2} \cdot \frac{s(C+C_{par1})+g_{m3}}{sC_{par1}+g_{m3}+g_{m4}}} \tag{2}$$

where $g_{m1,2} = 2g_{m1}g_{m2}/(g_{m1} + g_{m2})$. If g_{m1} is equal to g_{m2} then $g_{m1,2} = g_{m1} = g_{m2}$.

It can be shown that under proper conditions C_{par1} does not significantly affect the AC response of the integrator. For example, if C_{par1} is large (C_{par1} >> C) then the drain of M_1 is "strongly" shorted to GND and, as a consequence, C is connected in parallel to C_{par2}. The transmittance (2) reduces to the simple form $0.5g_{m1,2}/(s(C + C_{par2}))$ which represents a close-to-ideal integrator. Nevertheless, for low-frequency filters C is tens of pF, thus applying C_{par1} >> C is impractical. Note that C_{par1}, as well as C_{par2} result from parasitic capacitances of transistors, and they are tens to hundreds of fF. Therefore, in a practical low-frequency circuit, the inequalities C_{par1} << C and C_{par2} << C are fulfilled resulting in reduction of the integrator transmittance (2) to the form

$$\frac{V_{out}(s)}{(V_+ - V_-)(s)} \cong \frac{g_{m1,2}}{2} \cdot \frac{1}{sC} \cdot \frac{sC_{par1} + g_{m3} + g_{m4}}{s(C_{par1} + C_{par2}) + g_{m3} + g_{m4}} \tag{3}$$

The last fractional term in (3) represents a transmittance of an allpass filter. Thus, to improve the integrator response (3) one can slightly increase C_{par1}. Even small C_{par1} comparable to C_{par2} provides acceptable results. Figure 3b presents the flow of currents assuming $C_{par1} \geq C_{par2}$, C_{par1} << C, and C_{par2} << C. Under these conditions the integrating capacitor C intercepts most of the AC current (i_{ac}) and the transistors M_3 and M_4 conduct only DC currents of I_B (the current mirrors M_3-M_4 operate rather like an auto bias circuit). In consequence, the proposed integrator configuration with a floating capacitor has three major advantages over the conventional grounded-capacitor configuration. First, the parasitic capacitance C_{par1} helps to stabilize the currents in M_3 and M_4. Second, the mismatch between g_{m3} and g_{m4} does not affect AC response of the integrator. Third, due to $i_{ac} = 0.5 \cdot g_{m1,2} \cdot (V_+ - V_-)$, an integration time constant is doubled, that is advantageous for low-frequency filter realizations. In a filter synthesis process, the floating-capacitor integrator of Figure 3a can be represented by the Gm-C integrator composed of a grounded capacitor of C and a transconductor of $G_m = 0.5g_{m1,2}$, as shown in Figure 3c.

In the analysis presented here, the output conductances (g_{ds}) of the transistors are neglected because otherwise the integrator transfer function becomes too complicated to

interpret. The body effect in the differential pair M_1-M_2 is also neglected in the analysis because it does not affect the transfer function (2).

3.2. Lossy Integrator

A lossy integrator can be implemented using the proposed differential integrator in Figure 3a through introduction of a feedback loop that connects the output V_{out} to the inverting input V_{-}. However, one can derive a much simpler implementation using a conventional MOS source follower shown in Figure 4a. Its transmittance is as follows

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{g_m + sC_{gs}}{g_m + g_{mb} + s(C + C_{gs})} \cong \frac{g_m}{g_m + g_{mb} + sC} \tag{4}$$

where g_{mb} denotes the bulk (body) transconductance of the MOS transistor, and C_{gs} is its gate-source capacitance.

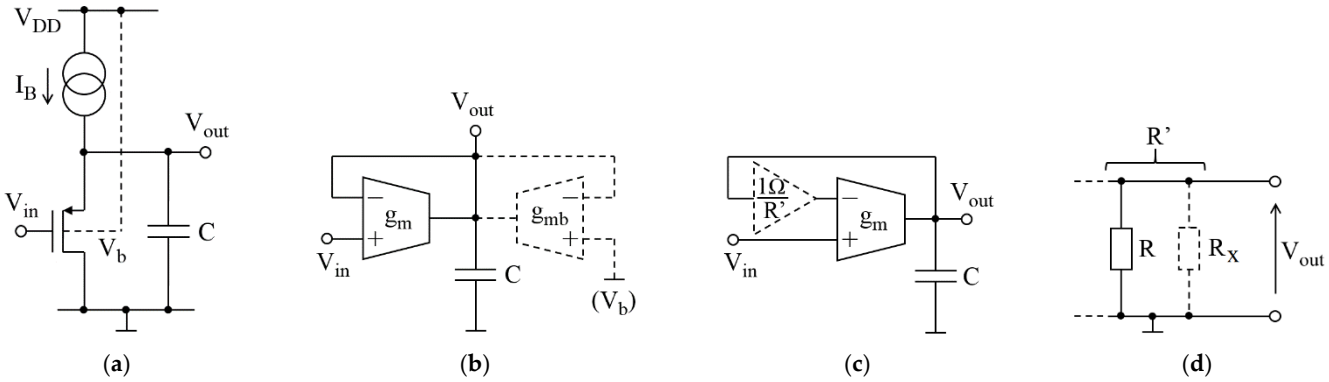

Figure 4. Lossy integrator based on MOS source follower: (**a**) transistor-level circuit; (**b**,**c**) equivalent OTA-C diagrams; (**d**) modified ladder tail due to the body effect in MOS transistor. $R' = g_m/(g_m + g_{mb})$ (Ω), $R_X = g_m \cdot R/(R \cdot g_m + R \cdot g_{mb} - 1\Omega \cdot g_m)$ (Ω).

The integrator transmittance (4) has a pole associated with $C + C_{gs}$ and a parasitic zero associated with C_{gs}. However, this zero is located 2 to 3 decades away from the pole because in low-frequency realizations the integrating capacitance C is of the order of pF and is much higher than the parasitic C_{gs} (fF). Thereby, C_{gs} can be neglected in (4). On the other hand, the parasitic body transconductance g_{mb} cannot be neglected in (4) because it is comparable to the main integrating transconductance g_m ($g_{mb} \approx 0.2\, g_m$). Therefore, when the transistor body terminal V_b is not connected to V_{out} (see Figure 4a), the body effect results in an additional OTA of g_{mb}, as shown in Figure 4b, or in an additional voltage amplifier of gain of $1\ \Omega/R' = 1 + g_{mb}/g_m$ (V/V), as depicted in Figure 4c. Fortunately, these extra amplifiers do not need to be implemented because the body effect can be accounted for in the course of filter synthesis by pre-modifying the component values in a ladder prototype. The body effect alters the termination resistor value to R', as explained in Figure 4d. The new value of R' involves updating the rest of the ladder components resulting from denormalization of impedance. For example, the component values in the ladder of Figure 1a, pre-modified due to the body effect, would be: $R' = 1\ \Omega/(1 + g_{mb}/g_m)$, $C_{1P}' = C_{1P} \cdot R/R'$, and $L_{2P}' = L_{2P} \cdot R'/R$.

4. Proposed Biquadratic Filter

Using the integrators of Figures 3a and 4a, the biquadratic filter can be synthesized according to the schematic of Figure 1b. Assuming no-body-effect in the integrator of Figure 4a (V_b connected with V_{out}), the transistor-level realization of the filter can be represented as the transistor-level circuit shown in Figure 5. Note that the synthesis has resulted in the filter based on the unity-gain buffer of ref. [20], but in opposite-transistor-type configuration.

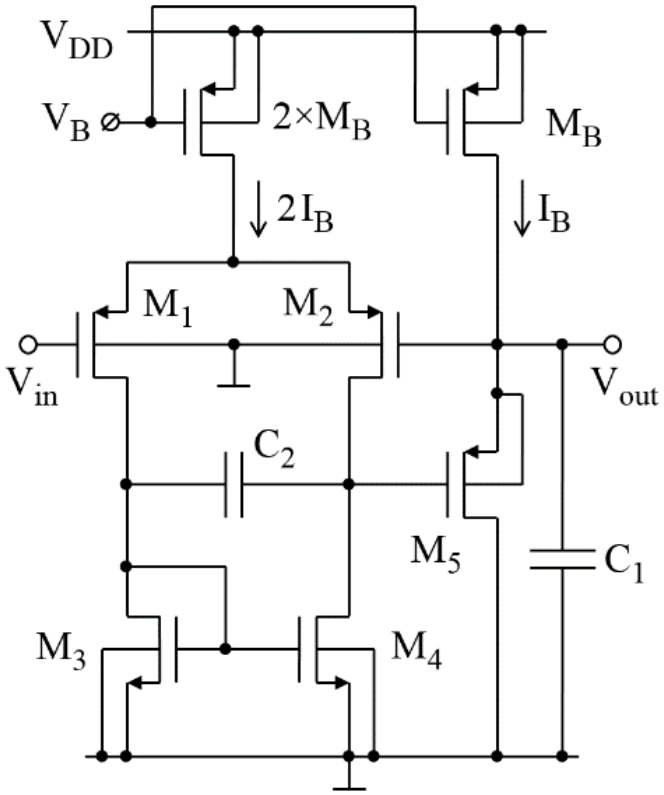

Figure 5. The 0.4-V biquadratic filter obtained on the basis of the ladder prototype in Figure 1a. C_1, C_2 and I_B are 9.2 pF, 8.7 pF, and 250 pA, respectively, assuming Butterworth approximation and f_{-3dB} of 100 Hz.

The example 100-Hz filter has been designed for biomedical applications with a supply voltage of 0.4 V and power consumption in the range of 1 nW. To address the requirement for such a low supply voltage, the X-FAB transistors with low threshold voltages (nominal $V_{THP} = -0.35$ V, $V_{THN} = 0.4$ V) are selected. Furthermore, bulks of the M_1 and M_2 transistors are connected to GND to reduce their threshold voltage to about −0.25 V. The bulk and source of M5 are connected in order to reduce the threshold voltage, as well as to avoid a correction of filter parameters due to the body effect (as described in Section 3.2). The bias current I_B is set to 250 pA in order to limit the transistors' transconductance to the level of a few nS and allow use of filter capacitors with practical values no greater than a few tens of pF. The detailed parameters of the transistors are given in Table 1.

Table 1. Simulated OP parameters of transistors (I_B = 250 pA, V_{DD} = 0.4 V, T = 27 °C).

Transistor	W/L [µm/µm]	g_m [nS]	g_{ds} [pS]	V_{TH} [V]	V_{GS} [V]	V_{DS} [V]
M_B	10/6	8.18	40	−0.334	−0.112	−0.141
$2 \times M_B$	$2 \times 10/6$	16.24	150	−0.334	−0.112	−0.112
M_1	5/3	7.84	31.4	−0.251	−0.028	−0.170
M_2	5/3	7.95	88.4	−0.251	−0.028	−0.107
M_3	10/10	7.69	62.2	0.387	0.117	0.117
M_4	10/10	7.77	20.5	0.387	0.117	0.180
M_5	$3 \times 5/3$	8.3	18	−0.337	−0.080	−0.259
M_{SH}	$3 \times 5/3$	8.3	18	−0.337	−0.080	−0.259

Note that the dimensions of the "mirroring" transistors, M_3 and M_4, are large to increase their parasitic capacitances (C_{par1} in Figure 3a) and improve an integrator response, as explained earlier in Section 3.1. The "integrating" transistors, M_1, M_2, and M_5, have transconductances of $g_{m1} \cong g_{m2} = g_{m1,2} = 7.9$ ns and $g_{m5} = 8.3$ nS. Thus, the transconductances of the equivalent OTAs in Figure 1b are: $G_{m1} = g_{m5} = 8.3$ nS, $G_{m2} = g_{m1,2}/2 = 7.9/2$ nS.

Assuming the Butterworth filter approximation (that means $Q = 0.707$ which implies that $\omega_0 = \omega_{-3dB}$), the components in the ladder prototype of Figure 1a have the following values normalized for ω_0 of 1 rad/s: $R = 1\ \Omega$, $L_{1P} = 1.414$ H, and $C_{1P} = 0.707$ F [21]. Thus, for $f_{-3dB} = f_0 = 100$ Hz (i.e., $\omega_0 = 2\pi \cdot 100$ rad/s), the capacitances in the biquad of Figure 5 are: $C_1 = 0.707 \cdot g_{m5}/(200\pi) = 9.34$ pF, $C_2 = 1.414 \cdot g_{m1,2}/2/(200\pi) = 8.89$ pF.

With the supply voltage V_{DD} of 0.4 V the drain-source voltage (V_{DS}) of the transistors approaches the triode region limit i.e., 100–200 mV (see Table 1). Under these conditions, the transistors' output conductances (g_{ds}) increase, which affects f_0 and Q. However, the deviation in the filter characteristics, caused by the increased g_{ds}, is relatively small and can therefore be compensated by a small (up to a few percent) adjustment of the filter capacitances [19]. The corrected values of the capacitances in the biquad of Figure 5 are $C_1 = 9.2$ pF and $C_2 = 8.7$ pF.

The simulated amplitude characteristic of the proposed biquad follows the ideal (RLC prototype) response down to −80 dB, as shown in Figure 6a. The detailed values of passband gain and −3-dB frequency are 0.99 V/V and 100 Hz.

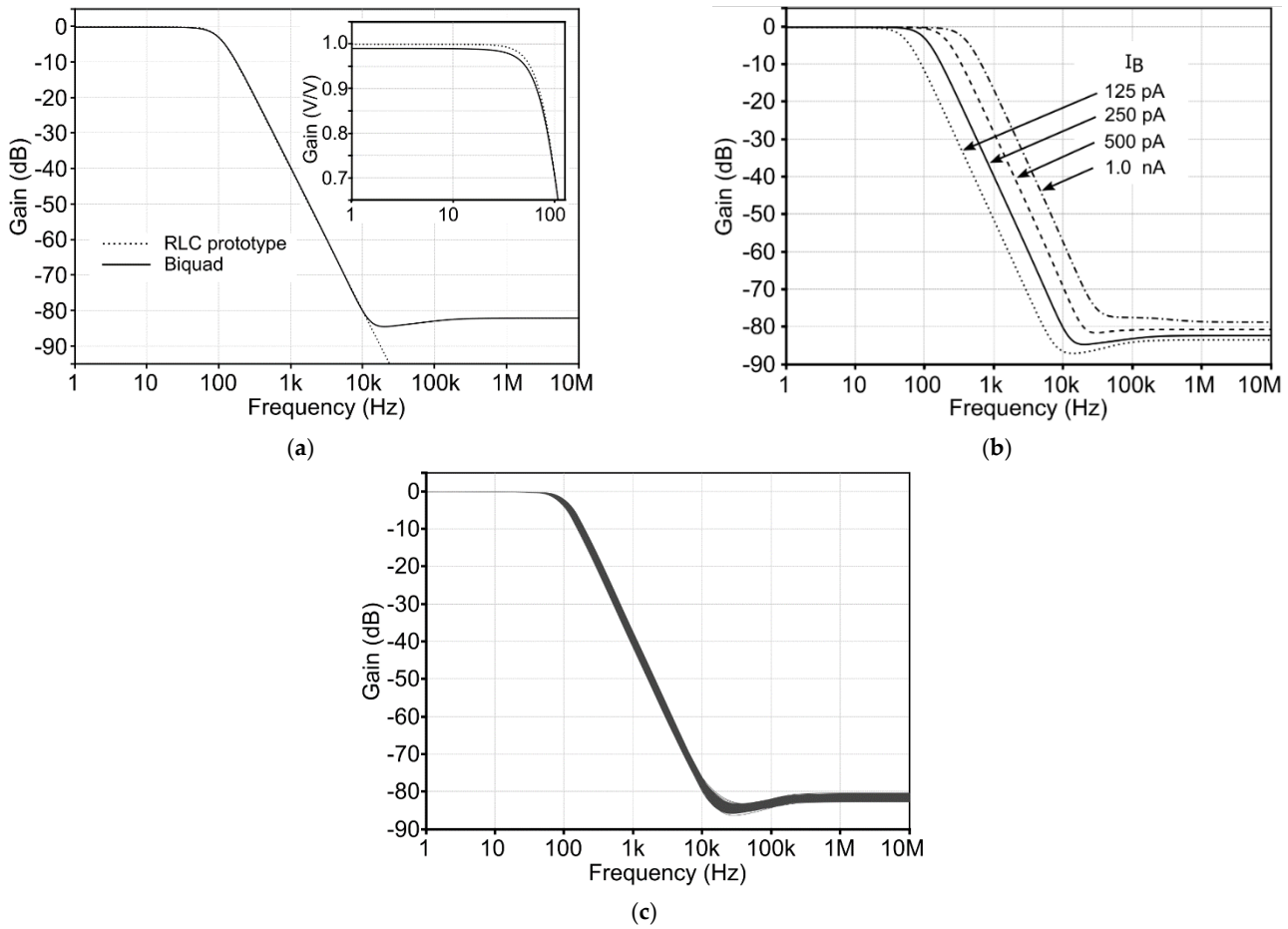

Figure 6. Simulation results of the biquad in Figure 5: (**a**) amplitude characteristic at the nominal bias I_B of 250 pA; (**b**) bandwidth tuning; (**c**) amplitude characteristic under the process spread and transistors-&-capacitors mismatch (500 Monte Carlo runs).

The −3-dB frequency can be tuned from 50 Hz to 377 Hz by means of changing the bias current I_B from 125 pA to 1 nA (Figure 6b). In the presence of the process deviation as well as transistor and capacitor mismatch (Figure 6c), the biquad keeps its passband gain of near 0.98–0.99 V/V and stopband attenuation of over 80 dB, whereas spread in the −3- dB frequency is only 4.5 Hz (1 sigma). The filter features a maximum input sine amplitude of 103.4 mV_{peak} (conditions: output THD = 1%, fundamental frequency = 20 Hz,

optimal DC input level = 260 mV). The input-referred noise integrated from 1 Hz to 100 Hz is 29 μV_{RMS}, which results in a biquad dynamic range of 68 dB.

5. Fourth Order Filters

In this section, two designs of fourth-order low-pass filters are presented and compared. One design is obtained using a ladder-based synthesis. Another one is generated by cascading the two biquads of Figure 5. The parameters of the obtained filters have been compared with each other and with the reference ladder prototype.

5.1. Proposed Ladder-Based Filter

Figure 7a,b shows, respectively, the 4th-order ladder prototype with single-resistance termination and the corresponding OTA-C schematic obtained by the state variable method. Assuming the ideal OTAs (i.e., $G_m >> G_o$), the filter in Figure 7b behaves as a unity-gain buffer because its input resistance is infinity, output resistance decreases to zero, and its gain is 1 V/V in the passband—regardless of the capacitance and the OTA transconductance values.

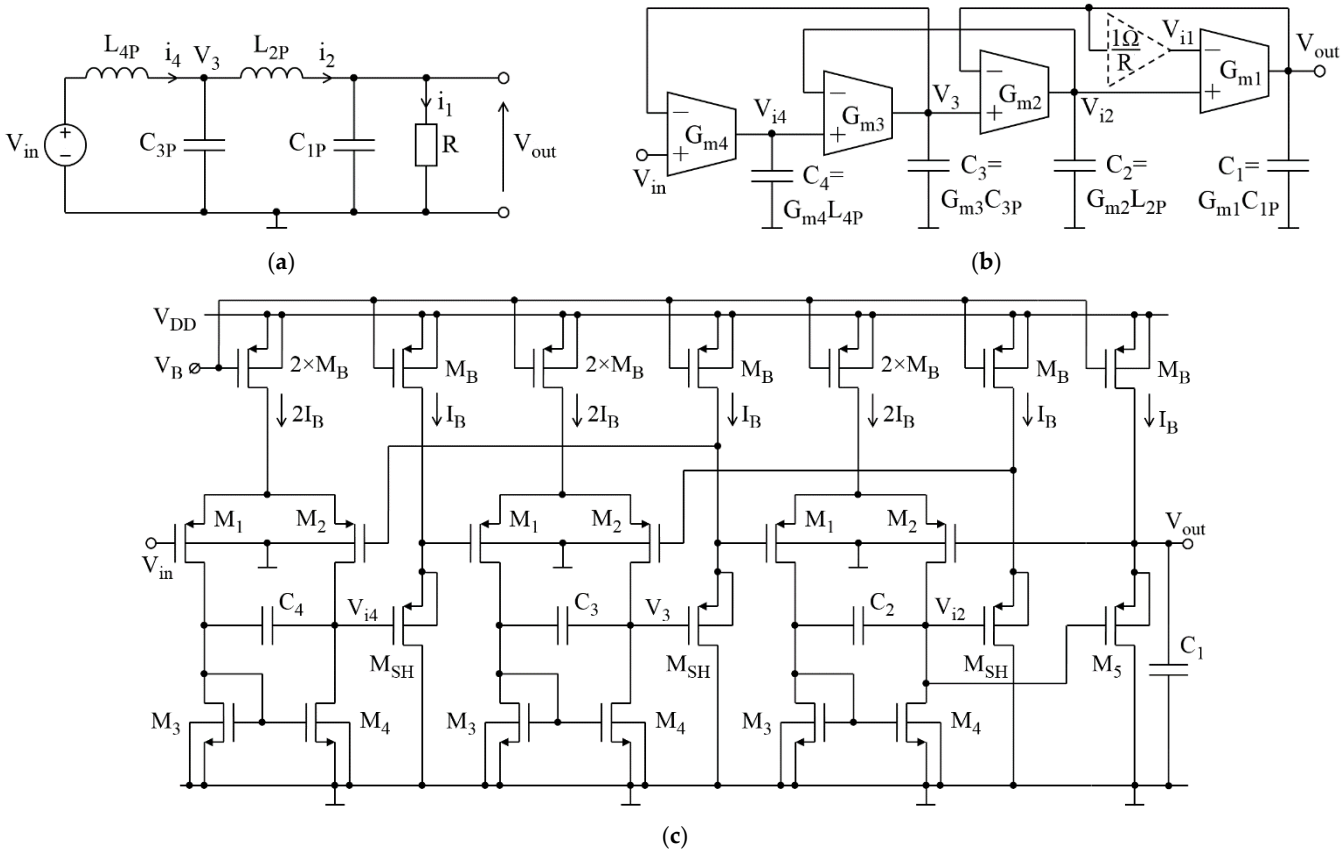

Figure 7. The 0.4-V, 100-Hz, fourth-order filter: (**a**) single-resistance terminated ladder prototype; (**b**) OTA-C (Gm-C) schematic; (**c**) transistor-level circuit. C_1 = 4.98 pF, C_2 = 6.73 pF, C_3 = 9.80 pF, C_4 = 9.50 pF, and I_B = 250 pA assuming Butterworth approximation and f_{-3dB} of 100 Hz.

Using the integrators shown in Figures 3a and 4a and following the schematic in Figure 7b (for R = 1) the transistorized filter shown in Figure 7c is obtained. The transistor parameters are the same as in the biquad of Figure 5 (see Table 1). Notice that three additional voltage shifters (M_{SH}) are used in the circuit. They increase the source-drain voltages of the M_2 transistors to 100–120 mV, allowing them to operate in the saturation region. Without the shifters, the M_2 source-drain voltages would be around 30 mV, that is below the triode region boundary.

Transconductances of OTAs in Figure 7b correspond to transconductances of transistors in Figure 7c as follows: $G_{m1} = g_{m5}$, $G_{m2} = G_{m3} = G_{m4} = g_{m1,2}/2$. The components in the normalized Butterworth ladder of Figure 6a are as follows: R = 1 Ω, C_{1P} = 0.3827 F, C_{3P} = 1.5772 F, L_{2P} = 1.0824 H, and L_{4P} = 1.5307 H [21]. Therefore, assuming $f_{-3dB} = f_0$ = 100 Hz, the capacitances calculated for the filter in Figure 7c are as follows: $C_1 = g_{m5} \cdot C_{1P}/(2\pi f_0)$ = 5.05 pF, $C_2 = g_{m1,2} \cdot L_{2P}/(2\pi f_0)$ = 6.80 pF, $C_3 = g_{m1,2} \cdot C_{3P}/(2\pi f_0)$ = 9.91 pF, and $C_4 = g_{m1,2} \cdot L_{4P}/(2\pi f_0)$ = 9.62 pF. After applying correction to these capacitances due to low V_{DD} and increased g_{ds} (as mentioned earlier in Section 4 [19]), their final values are as follows: C_1 = 4.98 pF, C_2 = 6.73 pF, C_3 = 9.80 pF, and C_4 = 9.50 pF.

5.2. Cascade Filter

Cascading the two biquads from Figure 5 results in the fourth-order filter shown in Figure 8. To obtain the Butterworth approximation and 100-Hz bandwidth, the natural frequencies and quality factors of the consecutive biquads should be: $\omega_{0A} = 2\pi \cdot 100$ rad/s, Q_A = 0.541, $\omega_{0B} = 2\pi \cdot 100$ rad/s, and Q_B = 1.307. Assuming the transistor transconductances given in Table 1 and using Equation (1), the calculated filter capacitances in Figure 8 are: C_{1A} = 7.146 pF, C_{2A} = 11.252 pF, C_{1B} = 17.265 pF, and C_{2B} = 4.657 pF. The final post-corrected values are: C_{1A} = 7.10 pF, C_{2A} = 11.14 pF, C_{1B} = 17.10 pF, and C_{2B} = 4.60 pF.

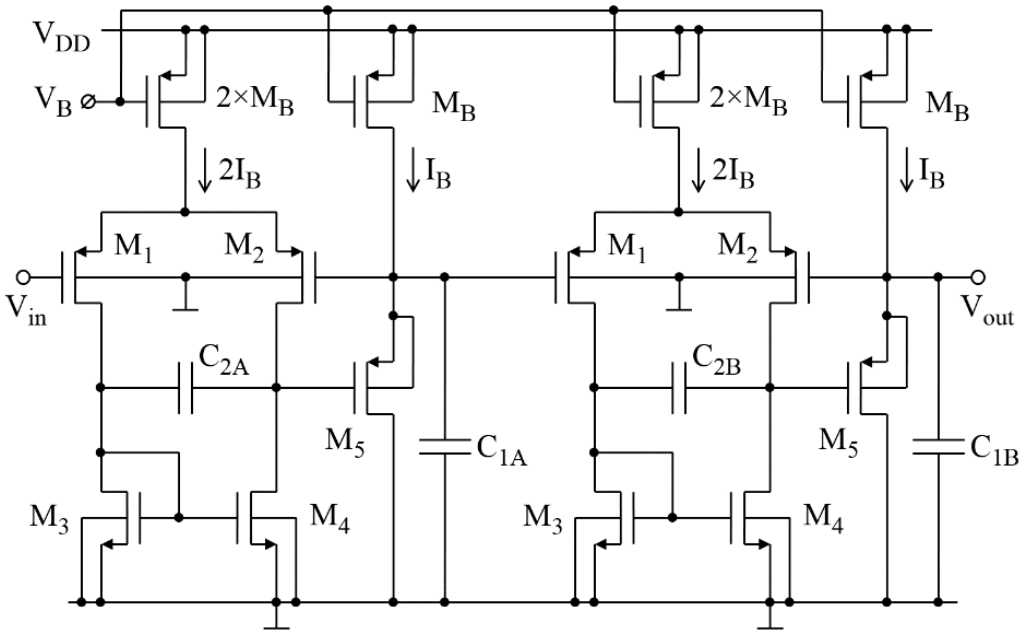

Figure 8. The 0.4-V, 100-Hz, fourth-order filter—the cascade of two biquads of Figure 5. C_{1A} = 7.10 pF, C_{2A} = 11.14 pF, C_{1B} = 17.10 pF, C_{2B} = 4.60 pF, and I_B = 250 pA assuming Butterworth approximation and f_{-3dB} of 100 Hz.

5.3. Simulations and Comparison

The nominal amplitude responses (for I_B = 250 pA) of the designed fourth-order structures are shown in Figure 9a. In the passband, the circuits have the same gain of 0.97–0.98 V/V (−264 mdB to −175 mdB). In the stopband, the gain of the ladder-based filter decreases to −120 dB, which is a worse result compared to the cascade filter (−160 dB). The −3-dB frequency in both realizations is the same (100.1 Hz) and can be tuned from 51 Hz to 377 Hz (Figure 9b).

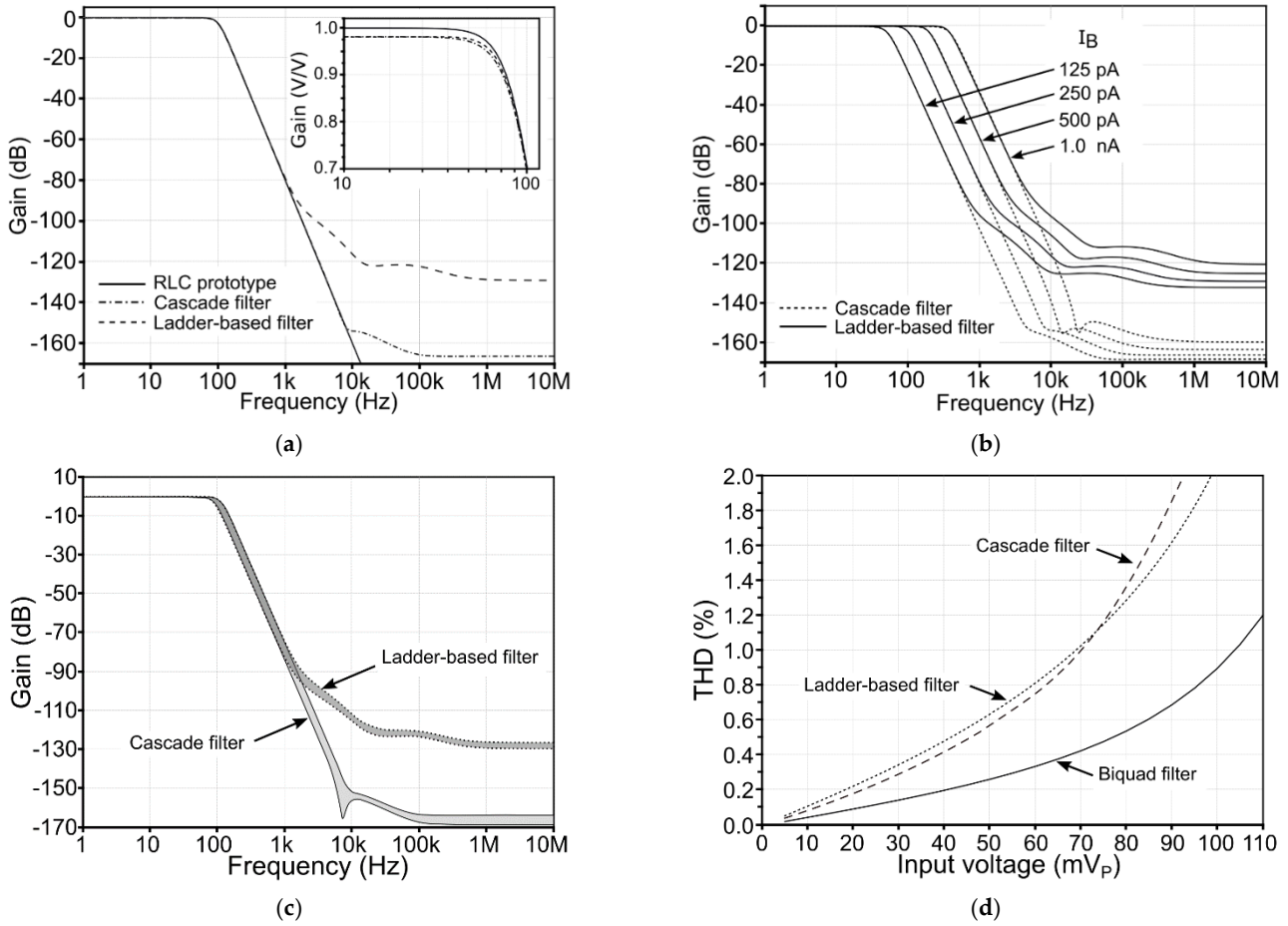

Figure 9. Simulation results of the fourth-order filters: (**a**) amplitude characteristic at the nominal bias I_B = 250 pA; (**b**) bandwidth tuning; (**c**) amplitude characteristic under the process spread and transistors-&-capacitors mismatch (500 Monte Carlo runs); (**d**) output THD at the input frequency of 20 Hz and optimal input DC level of 260 mV.

The influence of fabrication process spread and the mismatch of the filter components is illustrated in Figure 9c. As can be seen both filters behave similarly. The changes in the passband gain are insignificant, whereas a 1-sigma deviation in −3-dB frequency is only 4.5 Hz. Details of the filter performance under process-voltage-temperature (PVT) variations are provided in Appendix A.

In conclusion, both the ladder-based and cascade filters feature a similar maximum input sine amplitude of about 70 mV_{peak} (Figure 9d) and a noise of about 50 μV_{RMS}. As a result, a similar dynamic range of about 60 dB is obtained for both circuits. The ladder-based realization provides 8.9 pF smaller total capacitance, that translates to a reduction of 4050 μm^2 on a chip assuming the use of typical MIM capacitors of 2.2 $fF/\mu m^2$. Since the area of the capacitors determines the total area of the filters, the latter parameter is easily scalable and predictable. In addition, the total current consumption can be easy predicted because it results simply from the total number of the bias sources I_B, as given in Table 2.

Table 2. Scalable properties of the developed 0.4-V, 100-Hz filters.

Filter	Current Consumption	Total Capacitance	Layout Area
Biquad of Figure 5	$3 \cdot I_B$	C_T = 18.07 pF	A = 8214 μm^2
Ladder-based 4th-order filter of Figure 7	$10 \cdot I_B$	$\cong$1.66 C_T	$\cong$1.66 A
Cascade 4th-order filter of Figure 8	$6 \cdot I_B$	$\cong$2.2 C_T	$\cong$2.2 A

6. Summary of Low-Frequency Filter Performance

The parameters of the proposed and other state-of-the-art transistorized filters are collated in Table 3. The filters from [6–10] are selected due to their reported low supply voltages. The examples of OTA-C realizations, [11,12,14] are also included in the comparison. These OTA-C filters feature much smaller total capacitance (6–9 pF) compared to the transistorized solutions (25–80 pF). This results from the fact that a linear OTA has smaller transconductance (compared to a transistor) because linearization techniques are involved in its reduction. Thus, OTAs in refs. [11,12,14] have been linearized by a source degeneration reducing the transconductance to the range of single nano siemens. However, linearization techniques also increase the complexity and noise of the circuit [13,21]. In consequence, the OTA-C filters [11,12,14] are characterized by a high noise of over 190 μV_{RMS}. Note that OTA-C filters from refs. [11,12] feature a passband gain that is much lower than 1 V/V (−10.5 and −6 dB respectively), implying an increase of the input referred noise (IRN). However, one should emphasize that the low gain of these structures results from a synthesis based on double-resistance terminated ladders being characterized by 0.5-V/V gain. Thus, the noise performance of OTA-C filters [11,12] could be improved if ladders with single-resistance termination and gain of 1-V/V were used.

The transistorized solutions gathered in Table 3 provide only a slightly better dynamic range compared to OTA-C realizations. However, the power consumption of the transistorized filters (6–15 nW) is one to two orders lower compared to OTA-C filters (350–450 nW). In terms of power consumption, the proposed filters achieve best results of 0.6–1 nW (predicted by simulations). In addition, in terms of total capacitance and supply voltage, the proposed solutions outperform all other filters except the one from ref. [9].

Table 3. Low-frequency filter performance review.

	Transistorized								OTA-C		
	This Work			[6]	[7]	[8]	[9]	[10]	[11]	[12]	[14]
	Figure 5	Figure 7c	Figure 8								
Results	Sim.	Sim.	Sim.	Meas.	Meas.	Meas.	Sim.	Meas.	Meas.	Meas.	Meas.
Process [µm]	0.18	0.18	0.18	0.35	0.18	0.35	0.18	0.35	0.18	0.18	0.18
Supply [V]	0.4	0.4	0.4	0.6	1	0.9	0.3	1.5	1	1	1.8
Order, N	2	4	4	4	4	4	4	4	5	5	9
Cut. freq. fc [Hz]	100	100	100	101	732 [2]	100	100	100	240	50	5.4k [3]
Power, P [nW]	0.3	1	0.6	0.9	14.4	4.26	0.676	5.25	453	350	360
DR [dB]	68	59.6	60.6	47	55	48.2	58.1	56.9	50	49.9	34
IRN [μV_{RMS}]	29	51	46	46.27	50	80.5	87	39.38	340	194	560 (−62dB)
DC gain [dB]	−0.024	−0.191	−0.165	−2.77	−6	−0.05	0.144	−0.09	−10.5	−6	0
Tot. Cap. [pF]	18.07	31.03	39.94	60.56	80	38.5	25.2	47.14	6.76	6.8	9
Area [mm^2]	0.0082 [1]	0.014 [1]	0.018 [1]	0.168	0.13	0.11	0.0115 [1]	0.1	0.13	0.12	0.03
FOM [4]	2.20×10^{-14}	4.19×10^{-14}	2.47×10^{-14}	4.74×10^{-14}	8.94×10^{-14}	2.21×10^{-13}	2.91×10^{-14}	2.31×10^{-13}	7.55×10^{-12}	2.8×10^{-11}	2.18×10^{-13}

[1] Predicted assuming the use of MIM capacitors of 2.2 fF/μm^2. [2] Center frequency of a bandpass filter. [3] Constant delay bandwidth of an allpass filter. [4] FOM = P/(N·fc·DR).

7. Conclusions

Buffer-based "transistorized" filters are a promising alternative to OTA-C-based structures. The synthesis methodology of buffer-based filters, using the analogy to RLC ladder filters with single-resistance termination, was presented. Innovative transistor-level solutions operating at supply voltages of only 0.4 V were also proposed.

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Appendix A

This appendix provides in Tables A1 and A2 simulations results of −3-dB frequency and DC gain (passband gain) of the proposed fourth-order filters under PVT variation.

Table A1. Process (CMOS 180 nm X-FAB) corner simulation results for the ladder-based filter in Figure 7c.

	T = 0 °C					T = 27 °C					T = 60 °C				
V_{DD}	TM	WP	WS	WO	WZ	TM	WP	WS	WO	WZ	TM	WP	WS	WO	WZ
							−3-dB frequency [Hz]								
0.42	109.5	111.5	106.9	108.1	110.5	100.9	100.9	99.5	100.5	100.2	90.8	77.47	92.5	93.1	80.0
0.40	107.9	110.4	104.6	106.1	109.3	100.1	100.3	98.5	99.6	99.5	90.3	77.15	91.9	92.6	79.6
0.38	104.6	108.3	98.5	101.2	106.8	98.8	99.3	96.5	97.9	98.4	89.5	76.7	90.8	91.6	78.9
							DC gain [V/V]								
0.42	0.9747	0.9813	0.9569	0.9717	0.9724	0.9783	0.9718	0.9735	0.9802	0.9703	0.9466	0.9783	0.9721	0.9703	0.8779
0.40	0.9747	0.9812	0.9569	0.9717	0.9724	0.9783	0.9716	0.9735	0.9801	0.9702	0.9463	0.9780	0.9720	0.9701	0.8771
0.38	0.9746	0.9811	0.9569	0.9715	0.9723	0.9781	0.9713	0.9734	0.9800	0.9700	0.9457	0.9778	0.9718	0.9696	0.8759

Table A2. Process (CMOS 180 nm X-FAB) corner simulation results for the cascade filter in Figure 8.

	T = 0 °C					T = 27 °C					T = 60 °C				
V_{DD}	TM	WP	WS	WO	WZ	TM	WP	WS	WO	WZ	TM	WP	WS	WO	WZ
							−3-dB frequency [Hz]								
0.42	108.4	110.5	105.7	107.0	109.4	100.4	101.4	98.7	99.6	100.5	92.0	81.5	92.4	93.2	86.4
0.40	107.7	110.0	104.8	106.3	108.9	100.0	101.1	98.2	99.2	100.2	91.7	81.2	92.1	92.9	86.1
0.38	106.6	109.1	103.1	104.8	108.0	99.4	100.6	97.4	98.5	99.7	91.3	80.8	91.6	92.4	85.7
							DC gain [V/V]								
0.42	0.9834	0.9857	0.9782	0.9829	0.9817	0.9814	0.9674	0.9816	0.9842	0.9728	0.9296	0.7751	0.9739	0.9662	0.8351
0.40	0.9833	0.9855	0.9772	0.9827	0.9816	0.9812	0.9670	0.9814	0.9839	0.9726	0.9287	0.7734	0.9737	0.9656	0.8337
0.38	0.9830	0.9852	0.9768	0.9822	0.9814	0.9808	0.9667	0.9811	0.9834	0.9722	0.9271	0.7707	0.9733	0.9645	0.8312

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