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Hybridized Space-vector Pulse Width Modulation for Multiphase Two-level Voltage Source Inverter

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***Abstract*- In space vector pulse width modulation (SVPWM) algorithms for multiphase two-level voltage source inverters (VSI), the components of active vectors in all orthogonal spaces have to be calculated within the processor and stored in its memory. These necessitate intensive computational efforts of the processor and large memory space. This paper presents a hybridized SVPWM for multiphase two-level VSI. In this algorithm, elements of the vector coefficient inverse matrix are calculated once outside the inverter processor and treated as constant values; this reduces the computational efforts of the processor and memory space. This scheme reverses the computational steps used in classical SVPWM. Arbitrarily pre-selected active vectors (for any position and amplitude of the reference vectors) with durations determined using classical SVPWM concept are utilized. The durations of switching vectors are analyzed and the switching sequences in individual inverter phases are optimized to reduce the number of commutations. This approach demonstrates that resignation from classical analytical method in multiphase two-level VSI enables the creation of simplified modulation algorithm. This modulation strategy enables an independent generation of multiple output voltage vectors with independent rotating speed, lengths and positions. Experimental validation of the algorithm was carried out on two-level five-phase VSI with RL load.**

I. Introduction

A single multiphase voltage source inverter (VSI) can be used to independently control several multiphase motors with sinusoidal rotor field distribution and phase transposition. It can also supply a single multiphase motor with quasi-rectangular rotor field distribution; where the electromagnetic torque can be enhanced by utilizing higher current harmonics [1]–[2]. In such applications, it is necessary to ensure the possibility of generating several output voltage vectors with independent rotating frequencies, positions and lengths.

The classical approaches to the Space Vector Pulse Width Modulation (SVPWM) algorithms, usually used in three-phase inverters, require determining the polygon sector where the reference voltage vector is located. The vector durations are calculated for the active vectors surrounding this sector, [3]. The dc-link voltage can be optimally utilized if the vectors are well chosen (if they surround the sector). The duration of the active and zero voltage vectors are used to calculate the on-times of the switches in each of the inverter phases. The determined on/off-times are sent to the processor timers to generate the gate signals for inverter power switches.

The aforementioned described approach does not work well in multiphase inverters, where it is necessary to generate independently multiple output voltage vectors. Calculation of the durations for the active vector nearest to the reference voltage vectors can generate values greater than the switching period or even negative. This is because in a multiphase VSI, all the active vectors in all the orthogonal spaces depend on each other. The works presented in the literature are dedicated to solving this occurrence. When the calculated durations are negative, the next set of active vectors is selected and all the calculations are repeated, [4]. While this approach makes it possible to find the optimal set of active vectors, it is time-consuming. The computational efforts can be reduced if off-line prepared lookup tables are used, where the active vectors are specified for any position of reference voltage vectors, [5]. However, this method requires an enormous amount of processor memory. In some SVPWM strategies, the optimal set of active vectors is selected based on the analyses of the variables that are dependent on the reference vectors. For a five-phase system, the appropriate active vectors can be determined based on the analysis of ten variables which depend on the components of two reference vectors in orthogonal planes, [6]. However, for the case of inverters with more phases, the complexity of the algorithm will increase following this basic concept: the number of switching vectors for two-level converters is equal to 2^n, where n is the number of phases. While a five-phase VSI can produce 32 switching vectors determined in two orthogonal planes, a nine-phase VSI can produce 512 interdependent vectors in four orthogonal spaces, [7].

In SVPWM-controlled multiphase inverter, it is possible to use two adjacent large active vectors (nearest two vectors, NTV, SVPWM) to synthesize a single reference voltage vector; however, the algorithm for this approach cannot control the higher harmonics in additional subspaces. The problem of generating voltages in multiphase VSIs is significantly simplified if only a single voltage vector has to be generated [8]. In this case, the active vector sets with the appropriate duration ratio have to be used, [9]-[14]. The appropriate proportion of vector durations of such sets allows obtaining a non-zero output voltage vector in only one of the orthogonal systems. By changing the ratio of these vector durations, it is also possible to obtain an output voltage with injected higher harmonics, [15], but the positions of all the obtained output voltage vectors are mutually dependent. The method shown in [16] bases on the virtual active vector**.** This vector is constructed using 3 large active vectors (for a 5-phase system) to eliminate the voltage components in harmonic subspaces. The presented switching patterns are optimized; they contain 6 active vectors. Only one inverter

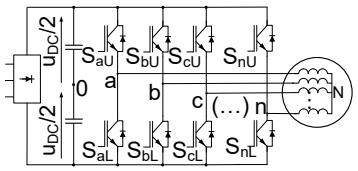

Fig. 1. The *n*-phase Voltage Source Inverter

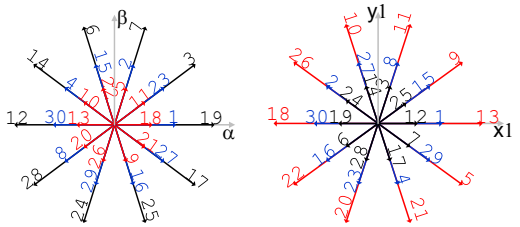

Fig. 2. Active vectors of a five-phase VSI in αβ space and x1y1 auxiliary subspace

phase-leg changes switching state in every switching action; this will not generate CMV spikes during the dead-time. The algorithm proposed in [17] is based on NTV-SVPWM method and allows the control of third harmonic component in a five-phase system. In [18], the analysis of multiphase SVPWM method based of multiple orthogonal spaces was presented. This method allows the generation of first and third output voltage harmonics; wherein the positions of both generated output voltage vectors are mutually dependent. The SVPWM proposed in [19] is dedicated to the generation of the fundamental voltage harmonic in multiphase Cascade H-Bridge inverter. Generating only one voltage vector in multiphase inverter allows the control of only one motor.

If the additional voltage vectors are simultaneously generated with a position dependent on the position of the basic voltage vector, it is possible to increase the value of the motor torque. It is not possible to independently control many motors supplied from the same inverter if all reference voltage vectors are not generated independently. This problem is the subject of researches presented in many publications, [6], [18] ,[20]. The modulation method for a five-phase inverter, presented in [21], requires the use of two such sets of active vectors. Each set is used to generate a non-zero output voltage in only one orthogonal frame; and is providing zero voltage in the other. Because of the larger number of vectors activated in subsequent sets (2 sequences with 4 vectors; that is 8 active vectors), the commutation number is increased. The commutation number can be reduced using the method proposed in [22]. This method relies on the sets of active vectors defined in orthogonal planes as proposed in [21], and the switching pattern is optimized by summation of durations of all planes on a per-leg basis.

From the foregoing, the works presented in the literature reveal that the predominant problem in SVPWM algorithms for multiphase inverters is finding the optimal set of active vectors that will allow independent generation of multiple output voltage vectors. This problem is analyzed in most of SVPWM modulation algorithms proposed for multi-phase systems. It turns out that the extension of SVPWM from 3-phase to multiphase system involves rigorous and complex computational algorithms. This is mainly due to the need to identify the optimal sequence of switching vector before determining their durations.

This paper proposes a simple SVPWM algorithm for multiphase voltage source inverters. The proposed solution reverses the procedure used in classical SVPWM solutions. In the classical solutions, it is necessary to select optimally the active vectors for which the durations will be determined. The on-times for the inverter active switches are calculated based on these durations. In the proposed solution, the optimal sequence of active vectors can be determined at the end of the algorithm, based on the previously calculated on-times; the SVPWM algorithm is based on the sequence of arbitrary pre-selected active vectors. Obtaining the optimal sequence of result vectors requires optimization procedures; the main goal of which is to fit the sequence of active and zero vectors to the switching period and to reduce the number of transistor commutations. This task is performed by grouping the gate signals in individual inverter phases and by adjusting the duration of the zero vectors. This optimization is necessary because the algorithm uses any active vectors that are not correlated with the positions and lengths of the reference vectors. In results, the proposed method simplifies the major problem of SVPWM algorithms for multiphase VSIs; which is the need for the specification of the relevant active vectors.
Since the algorithm uses dependencies dedicated to SVPWM algorithms, and the optimization is carried out in individual phases of the inverter (which is a feature of SPWM algorithms), the solution has been called the hybridized SVPWM algorithm. This control approach demonstrates that resignation from classical analytical method in multiphase two-level VSI enables the creation of relatively simple modulation algorithm.

This modulation approach provides a generalization of the SVPWM strategy for five-phase VSI with third harmonic injection, as proposed in [23]. The proposed algorithm can be formulated for two-level VSIs with any number of phases and enables the simultaneous generation of independent output voltage vectors with various lengths (voltages) and positions (frequencies). In the odd phase system, the vectors are defined in *(n-1)/2* orthogonal spaces. In the case of even phase system, it is possible to define the vectors in *(n-2)/2* orthogonal spaces, [1].

The proposed SVPWM algorithm was deployed in a five-phase (*(n-1)/2* orthogonal spaces) two-level VSI supplying a star connected RL loads. Comparatively, the SPWM algorithm with min-max function injection was deployed in the control of the same VSI that supplies the same loads. The SPWM with common-mode voltage injection is commonly considered a replacement for the SVPWM methods, especially in multiphase inverters**,** [24].

The detailed step-by-step calculations of the proposed SVPWM algorithm are provided in the following sections of this paper. All theoretical analyses are verified with experimental results.

II. Space Vector Pulse Width Modulation

The output voltages of an *n*-phase VSI shown in Fig. 1 can be described as:

$$u_{xN} = \frac{u_{DC}}{2}\left(T_{xU} - T_{xL} - \frac{1}{n}\sum_{x=a}^{n}\left(S_{xU} - S_{xL}\right)\right), x = a...n \quad (1)$$

where u_{xN} is the voltage between the *x*-phase and motor star point (*N*), u_{DC} is the dc-link voltage, S_{xU}, S_{xL} are the gate signals for the *x*-phase upper ($_U$) and lower ($_L$) switches with the values: 1 – the switch is turned on, and 0 – the switch is turned off.

The phase voltages corresponding to active and zero voltage vectors can be determined by inserting appropriate states of the gate signals in (1). All the output voltages, assigned to active and zero vectors, can be transformed by applying the decoupled (Clarke's) transformation matrix, which replaces the original sets of *n* variables with new sets in orthogonal space $\alpha\beta$ and subspaces *xy*:

$$\begin{bmatrix} u_\alpha & u_\beta & u_{x1} & u_{y1} & \dots & u_{x(n-3)/2} & u_{y(n-3)/2} & u_o \end{bmatrix}^T = \boldsymbol{X}\cdot\begin{bmatrix} u_{aN} & u_{bN} & u_{cN} & \dots & u_{nN} \end{bmatrix}^T, \quad (2)$$

where u_o is the zero-sequence component, and the transformation matrix $\boldsymbol{X}$ for an arbitrary number of phases '*n*' in power invariant form is given in [1].

Note that the last two rows of the matrix X in [1] define the two zero-sequence components of even-phase systems and the last row of the transformation matrix is omitted for all odd phase systems (only a single zero-sequence component is utilized). The first two rows define the variables that will lead to fundamental flux and torque production in a multiphase motor, the next rows define *(n-4)/2* (for *n*=even) or *(n-3)/2* for *n*=odd pairs of x-y components, wherein the pairs of x-y components are completely decoupled from all other components.

The obtained active and zero voltage vectors can be redefined using normalized coefficients $\boldsymbol{V}$:

$$\begin{bmatrix} u_\alpha & u_\beta & u_{x1} & u_{y1} & \dots & u_{x(n-3)/2} & u_{y(n-3)/2} & u_o \end{bmatrix}^T = \begin{bmatrix} V_\alpha & V_\beta & V_{x1} & V_{y1} & \dots & V_{x(n-3)/2} & V_{y(n-3)/2} & V_o \end{bmatrix}^T \cdot u_{DC}. \quad (3)$$

On account of:

$$\begin{bmatrix} V_\alpha & V_\beta & V_{x1} & V_{y1} & \dots & V_{x(n-3)/2} & V_{y(n-3)/2} & V_o \end{bmatrix}^T = \boldsymbol{X}\cdot\begin{bmatrix} u_{aN} & u_{bN} & u_{cN} & \dots & u_{nN} \end{bmatrix}^T \cdot \frac{1}{u_{DC}}, \quad (4)$$

the values of the coefficients $\boldsymbol{V}$ do not depend on the dc-link voltage.

The output voltages of an *n*-phase VSI should be generated using *n-1* active vectors (*n* is an odd number). Their duration must fulfil the following condition:

$$u_{DC}\cdot\boldsymbol{V}\cdot\boldsymbol{T} = T_s\cdot\boldsymbol{U}_{ref}, \quad (5)$$

where T_s is the switching period, $\boldsymbol{U}_{ref}$ are the reference voltage components, $\boldsymbol{T}$ are active voltage durations:

$$\boldsymbol{U}_{ref} = \begin{bmatrix} u_{\alpha ref} & u_{\beta ref} & \dots & u_{\alpha((n-3)/2)ref} & u_{\beta((n-3)/2)ref} \end{bmatrix}^T, \quad \boldsymbol{T} = \begin{bmatrix} t_1 & t_2 & \dots & t_{n-1} \end{bmatrix}^T, \quad (6)$$

where *n* is the number of inverter phases.

The matrix $\boldsymbol{V}$ with dimension *(n-1)*x*(n-1)* contains the coefficients of the utilized *(n-1)* active vectors:

$$\boldsymbol{V} = \begin{bmatrix} V_{\alpha 1} & V_{\alpha 2} & \dots & V_{\alpha(n-1)} \\ V_{\beta 1} & V_{\beta 2} & \dots & V_{\beta(n-1)} \\ \dots & \dots & \dots & \dots \\ V_{x((n-3)/2)(1)} & V_{x((n-3)/2)(2)} & \dots & V_{x((n-3)/2)(n-1)} \\ V_{y((n-3)/2)(1)} & V_{y((n-3)/2)(2)} & \dots & V_{y((n-3)/2)(n-1)} \end{bmatrix} \quad (7)$$

The duration of active vectors can be determined similarly to the classic SVPWM algorithms:

$$\boldsymbol{T} = \left(T_s\cdot\boldsymbol{V}^{-1}\right)\cdot\left(\frac{1}{u_{DC}}\cdot\boldsymbol{U}_{(ref)}\right). \quad (8)$$

The difference between classical and proposed approaches is in the selection of active vectors. In the classical SVPWM algorithms, the active vectors are selected based on the positions of reference voltage vectors. But the proposed approach herein bases on some preliminary selected active vectors for any position and length of the reference voltage vectors. As a result, the calculated vector durations, (8), can reach any value; they can be negative or greater than the switching period T_s. The resulting switching sequence will be optimised in the next steps of the algorithm to ensure non-negative vector durations. It is worth noting that the choice of active vectors is irrelevant. They can have any lengths and positions regardless of the length and positions of the reference vectors. The only requirement is that the components of these active vectors form an invertible matrix.

Because the vector coefficients, V, are not dependent on the dc-link voltage, the elements of the inverse matrix V-1 can be calculated once outside the inverter microprocessor and $\left(T_s\cdot\boldsymbol{V}^{-1}\right)$ can be treated as matrix of constant coefficients (8) (which reduces the computational efforts of the microprocessor. The influence of normalizing the reference vectors $\left(\boldsymbol{u}_{(ref)}/u_{DC}\right)$ on the computational efforts is negligible). Additionally, in the classical SVPWM algorithms, the components of all active vectors in all orthogonal spaces have to be stored in the processor memory. But the proposed solution requires only the elements of the inverted matrix (pre-selected vector components) to be stored in the memory.

III. Optimization of Switching Sequence

The proposed SVPWM scheme reverses the procedure used in classical SVPWM solutions. In the classical solutions, it is necessary to select optimally the active vectors for which the durations will be determined. The on-times for the inverter active switches are calculated based on these durations. In the

proposed solution, the optimal sequence of active vectors can be determined at the end of the algorithm, based on the previously calculated on-times. However, determining the sequence of active vector is only optional and is not required for the algorithm to work properly.

The calculated vector durations in (8) can reach any value; they can be negative or greater than the switching period T_s. It is essential that the active vectors are designated as:

$$v = 2^0 \cdot S_{aU} + 2^1 \cdot S_{bU} + \ldots + 2^n \cdot S_{nU} \tag{9}$$

and

$$v = 2^n - 1 - \left(2^0 \cdot S_{aU} + 2^1 \cdot S_{bU} + \ldots + 2^n \cdot S_{nU}\right) \tag{10}$$

in order to provide the same lengths and opposite directions in any orthogonal spaces. $S_{aU}...S_{nU}$ are the gate signals for upper switches, and v is vector identification number. This property is shown in Fig. 2 for five-phase VSI, where it is possible to generate 32 vectors (with the numbers 0 ... 31) and all the active vectors with the numbers v and 31-v provide the same lengths and opposite directions in both orthogonal spaces.

The property indicated above can be used when negative durations are determined. The active vectors with negative durations can be replaced with the vectors with opposite directions and positive durations:

$$if\ t_{(i)} < 0 \Rightarrow \begin{cases} t_{(i)} = -t_{(i)} \\ v = 2^n - 1 - v \end{cases}, i = 1...(n-1), \tag{11}$$

This makes all vector durations positive, but the duration of individual active vectors or their sum can be greater than the switching period, T_s.

In modulation algorithms, it is necessary to ensure equality of the inverter output voltage (averaged over the switching period) and the reference voltage. The average value of the inverter phase voltages does not depend on the active vector sequence (the switching order) but depends on the total on-times of upper and lower switches in the inverter phases and the DC-link voltage; because:

$$\begin{aligned} u_{x(AV)} &= \frac{1}{T_s} \cdot \sum_{i=1}^{n-1} \left(u_{DC} \cdot \left(S_{xU(i)} - S_{xL(i)}\right) \cdot t_{(i)}\right) = \\ & u_{DC} \cdot \frac{1}{T_s} \cdot t_{x(ON)} - u_{DC} \cdot \frac{1}{T_s} \cdot t_{x(OFF)}, \end{aligned} \tag{12}$$

where

$$\begin{aligned} t_{x(ON)} &= \sum_{i=1}^{n-1} \left(S_{xU(i)} \cdot t_{(i)}\right) = \sum_{i=1}^{n-1} \left(t_{(i)}\right) \Leftrightarrow S_{xU(i)} = 1, S_{xL(i)} = 0, \\ t_{x(OFF)} &= \sum_{i=1}^{n-1} \left(S_{xL(i)} \cdot t_{(i)}\right) = \sum_{i=1}^{n-1} \left(t_{(i)}\right) \Leftrightarrow S_{xU(i)} = 0, S_{xL(i)} = 1, \\ & x = a...n. \end{aligned} \tag{13}$$

and $u_{x(AV)}$ is an average value of the phase voltage, $t_{(i)}$ are the durations of active vectors determined in (8) (and (11) for the negative durations), S_{xu} are the gate signals for upper switches determined based on the identification number v, (9), of the preselected active vectors. Therefore, it is possible to shift the gate signals to create groups of zeroes (switch is turned-off) and ones (switch is turned-on) in any of the inverter phases

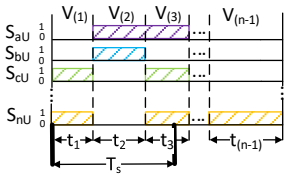

Fig. 3. Sequence of active voltage vectors of a *n*-phase VSI

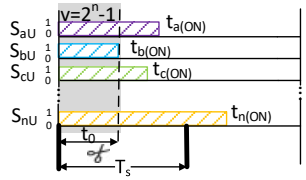

Fig. 4. Shifted gate signals for upper switches

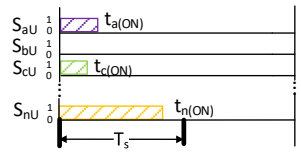

Fig. 5. Elimination of zero voltage vector $v=2^n-1$

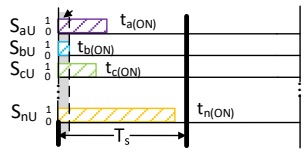

Fig. 6. Resulting sequence of gate signals of a *n*-phase VSI

without changing the average value of inverter phase voltages (and consequently without changing the output voltage vectors). The averaged output voltages obtained using the gates signals shown in Figures 3 and 4 are the same.

The obtained durations $t_{x(ON)}$ and $t_{x(OFF)}$, (13), are non-negative, but they can be greater than the switching period T_s. However, it can be seen that when all of the S_{xu} signals are equal to 1 (Fig. 4), a zero vector ($v=2^n-1$) is generated. Its duration is equal to:

$$t_0 = min\left(t_{a(ON)}...t_{n(ON)}\right), x = a...n. \tag{14}$$

Removing this vector from the switching sequence (Fig. 4) will not affect the generated output voltages. In result, a sequence of gate signals giving only the active vectors is obtained (Fig. 5). The durations of gate signals are equal to:

$$t_{x(ON)} = t_{x(ON)} - t_0, x = a...n. \tag{15}$$

The next step is to introduce two zero voltage vectors to the switching sequence. Their durations can be calculated as:

$$t_0 = 0.5 \cdot \left(T_s - max\left(t_{a(ON)}...t_{n(ON)}\right)\right), \tag{16}$$

and the durations of upper transistor gate signals are equal to:

$$t_{x(ON)} = t_{x(ON)} + t_0, x = a...n. \tag{17}$$

All the calculated durations are in the range of $0...T_s$. The obtained switching sequence requires only one switch gated in each inverter phase during the switching period (Fig. 6). The off-times of upper switches can be calculated as:

$$t_{x(OFF)} = T_s - t_{x(ON)}, x = a...n. \tag{18}$$

The determined on/off-times can be sent to the processor timers to generate the gate signals for inverter power switches. The resulting active and zero vectors can be determined with a simple algorithm. This algorithm is not necessary for implementation, because most processor units include the timers which can be used to count-down the switches' on/off-times in the individual inverter phases.

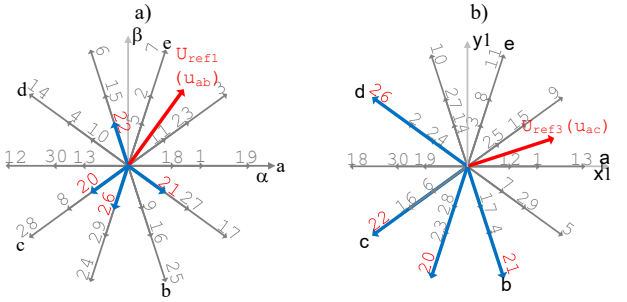

Fig. 7. The position of the reference voltage vectors and the active vectors selected in the first step of SVPWM algorithm

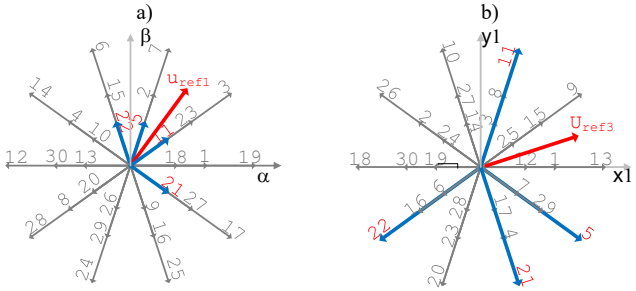

Fig. 8. The position of the reference voltage vectors and the replaced active vectors

IV. Generating Two Independent Voltage Vectors in a Five-phase VSI– Detailed Calculation Example

The properties of the proposed SVPWM algorithm will be shown on the example of a five-phase inverter, where two output voltage vectors should be generated using arbitrary selected four short active vectors v_1=21, v_2=26, v_3=22, v_4=20, (Fig. 7). The choice of active vectors is irrelevant. They can have any lengths and positions regardless of the length and positions of the reference vectors. The only requirement is that the components of these active vectors form an invertible matrix. When referring to a five-phase inverter, they can be long vectors, medium vectors, or any combination thereof, that will provide matrix inversion.

The worst case is analysed with respect to DC-link utilization, because the adjacent (u_{ab}) and non-adjacent line (u_{ac}) voltages reach the peak values at the same time, as shown in [25]. For the presented case, the components of the reference vectors are equal to:

$$\boldsymbol{U}_{ref} = \left[\left|\boldsymbol{u}_{ref\,1}\right|\cos\left(\tfrac{3\pi}{10}\right) \quad \left|\boldsymbol{u}_{ref\,1}\right|\sin\left(\tfrac{3\pi}{10}\right) \quad \left|\boldsymbol{u}_{ref\,3}\right|\cos\left(\tfrac{\pi}{10}\right) \quad \left|\boldsymbol{u}_{ref\,3}\right|\cos\left(\tfrac{\pi}{10}\right)\right]^T \quad (19)$$

while the matrix (7) for the preselected active vectors can be rewritten as:

$$\boldsymbol{V} = \begin{bmatrix} \overset{v=21}{0.391\cdot\cos\left(9\cdot\frac{2\pi}{10}\right)} & \overset{v=26}{\dots} & \overset{v=22}{\dots} & \overset{v=20}{0.391\cdot\cos\left(6\cdot\frac{2\pi}{10}\right)} \\ \dots & \dots & \dots & \dots \\ 1.023\cdot\sin\left(8\cdot\frac{2\pi}{10}\right) & \dots & \dots & 1.023\cdot\sin\left(7\cdot\frac{2\pi}{10}\right) \end{bmatrix}. \quad (20)$$

The durations of active vectors can be determined using (8):

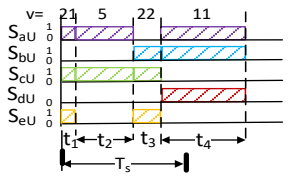

Fig. 9. The durations of active vectors

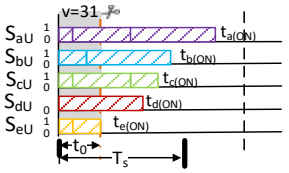

Fig. 10. Grouping of the gate signals

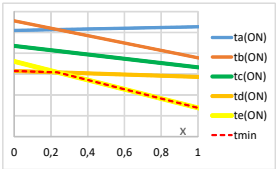

Fig. 11. The durations $ta_{(ON)}$…$te_{(ON)}$ as a function of the "x" factor and the minimum value of these durations (t_{min})

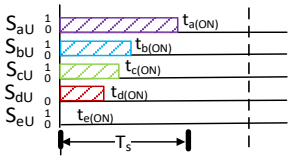

Fig. 12. Elimination of zero vector v=31

$$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \\ t_4 \end{bmatrix} = \frac{T_s}{u_{DC}} \cdot \begin{vmatrix} 0.6015\left|\boldsymbol{u}_{ref\,1}\right| - 0.3717\left|\boldsymbol{u}_{ref\,3}\right| \\ -0.3717\left|\boldsymbol{u}_{ref\,1}\right| - 0.6015\left|\boldsymbol{u}_{ref\,3}\right| \\ 1.2030\left|\boldsymbol{u}_{ref\,1}\right| - 0.7435\left|\boldsymbol{u}_{ref\,3}\right| \\ -1.5747\left|\boldsymbol{u}_{ref\,1}\right| + 0.1420\left|\boldsymbol{u}_{ref\,3}\right| \end{vmatrix}. \quad (21)$$

For the case, when:

$$\frac{\left|\boldsymbol{u}_{ref\,3}\right|}{\left|\boldsymbol{u}_{ref\,1}\right|} = x, \quad (22)$$

The equation (21) can be rewritten as:

$$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \\ t_4 \end{bmatrix} = \frac{T_s}{u_{DC}} \cdot \begin{vmatrix} (0.6015 - 0.3717x)\left|\boldsymbol{u}_{ref\,1}\right| \\ (-0.3717 - 0.6015x)\left|\boldsymbol{u}_{ref\,1}\right| \\ (1.2030 - 0.7435x)\left|\boldsymbol{u}_{ref\,1}\right| \\ (-1.5747 + 0.1420x)\left|\boldsymbol{u}_{ref\,1}\right| \end{vmatrix}. \quad (23)$$

In the analysed case, the duration t_1 is positive for $x<1.6180$, t_2 will be negative regardless of the x factor; t_3 will be positive for $x<1.6180$ and $t4$ will be positive for $x>11.0902$. Let us assume that $0 \le x \le 1$ and x is given in (22), then $t_1>0$, $t_2<0$, $t_3>0$ and $t_4<0$. Due to the negative duration of the pre-selected two active vectors v_2=26 and v_4=20, these vectors should be replaced with the opposite vectors as given in (11):

$$\begin{aligned} t_2 < 0 \Rightarrow \begin{cases} t_2 = -t_2 \\ v_2 = 2^5 - 1 - 26 = 5' \end{cases} \\ t_4 < 0 \Rightarrow \begin{cases} t_4 = -t_4 \\ v_4 = 2^5 - 1 - 20 = 11' \end{cases} \end{aligned} \quad (24)$$

The resulting active vectors v_1=21, v_2=5, v_3=22, v_4=11 are shown in Fig. 8. Their durations are equal to:

$$\begin{bmatrix} t_1 \\ t_2 \\ t_3 \\ t_4 \end{bmatrix} = \frac{T_s}{u_{DC}} \cdot \begin{vmatrix} (0.6015 - 0.3717x)\left|\boldsymbol{u}_{ref\,1}\right| \\ (0.3717 + 0.6015x)\left|\boldsymbol{u}_{ref\,1}\right| \\ (1.2030 - 0.7435x)\left|\boldsymbol{u}_{ref\,1}\right| \\ (1.5747 - 0.1420x)\left|\boldsymbol{u}_{ref\,1}\right| \end{vmatrix} \quad (25)$$

The resulting switching sequence is shown in Fig. 9. All the vector durations are positive, but they can be greater than the switching period T_s.

The average value of the inverter phase voltages does not depend on the sequence of active vector (the switching order) but depends on the total on-times of upper and lower switches and the dc-link voltage, (12). It is therefore possible to shift the gate signals to create groups of zeroes (switch is turned-off) and ones (switch is turned-on) in any of the inverter phases without changing the average value of inverter phase voltages (Fig. 10). The identification numbers v of pre-selected active vectors can be decoded using (9) (Fig. 9) as:

$$\begin{aligned}
&v_1 = 21 \Leftrightarrow\ S_{aU1}=1, S_{bU1}=0, S_{cU1}=1, S_{dU1}=0, S_{eU1}=1,\\
&v_2 = 5 \Leftrightarrow\ S_{aU2}=1, S_{bU2}=0, S_{cU2}=1, S_{dU2}=0, S_{eU2}=0,\\
&v_3 = 22 \Leftrightarrow S_{aU3}=0, S_{bU3}=1, S_{cU3}=1, S_{dU3}=0, S_{eU3}=1,\\
&v_4 = 11 \Leftrightarrow S_{aU4}=1, S_{bU4}=1, S_{cU4}=0, S_{dU4}=1, S_{eU4}=0,
\end{aligned} \tag{26}$$

Because of (13) and (26), the upper switches' on- times can be determined as (Fig. 10):

$$\begin{aligned}
t_{a(ON)} &= t_1 + t_2 + t_4 = \frac{T_s}{u_{DC}}\left(2.5480 + 0.0878\cdot x\right)\left|u_{ref1}\right|,\\
t_{b(ON)} &= t_3 + t_4 = \frac{T_s}{u_{DC}}\cdot\left(2.7778 - 0.8865\cdot x\right)\left|\boldsymbol{u}_{ref1}\right|,\\
t_{c(ON)} &= t_1 + t_2 + t_3 = \frac{T_s}{u_{DC}}\cdot\left(2.1763 - 0.5137\cdot x\right)\left|\boldsymbol{u}_{ref1}\right|,\\
t_{d(ON)} &= t_4 = \frac{T_s}{u_{DC}}\cdot\left(1.5747 - 0.1420x\right)\left|\boldsymbol{u}_{ref1}\right|,\\
t_{e(ON)} &= t_1 + t_3 = \frac{T_s}{u_{DC}}\left(1.8045 - 1.1152\cdot x\right)\left|\boldsymbol{u}_{ref1}\right|.
\end{aligned} \tag{27}$$

The shortest of the durations $t_{a(ON)}...t_{e(ON)}$ (27) is the duration of the zero voltage vector $v=31$ (all the gate signals $S_{aU}...S_{eU}$ are equal to one in Fig. 10). This zero vector can be eliminated without modifying the inverter output voltage, (15).

For the analysed case of a five-phase inverter, the selection of the phase with the shortest upper transistor' on-time depends on the value of the x coefficient in (22). For $0\le x<0.2361$, the shortest time is $t_{d(ON)}$ (27) and the zero vector duration is equal to: $t_0=t_{d(ON)}$; while for $0.2361<x\le 1.0$ the shortest time is $t_{e(ON)}$ (27) (Fig. 11) and the duration of zero vector is $t_0=t_{e(ON)}$. Considering the first of these cases where $t_0=t_{d(ON)}$ and removing the zero vector duration from the upper switches' on- times (27), the times of gate signals are equal to:

$$\begin{aligned}
t_{a(ON)} &= t_{a(ON)} - t_{d(ON)} = \frac{T_s}{u_{DC}}\left(0.9732 + 0.2298\cdot x\right)\left|u_{ref1}\right|,\\
t_{b(ON)} &= t_{b(ON)} - t_{d(ON)} = \frac{T_s}{u_{DC}}\cdot\left(1.2030 - 0.7435\cdot x\right)\left|\boldsymbol{u}_{ref1}\right|,\\
t_{c(ON)} &= t_{c(ON)} - t_{d(ON)} = \frac{T_s}{u_{DC}}\cdot\left(0.6015 - 0.3717\cdot x\right)\left|\boldsymbol{u}_{ref1}\right|,\\
t_{d(ON)} &= t_{d(ON)} - t_{d(ON)} = 0\\
t_{e(ON)} &= t_{e(ON)} - t_{d(ON)} = \frac{T_s}{u_{DC}}\left(0.2298 - 0.9732\cdot x\right)\left|\boldsymbol{u}_{ref1}\right|.
\end{aligned} \tag{28}$$

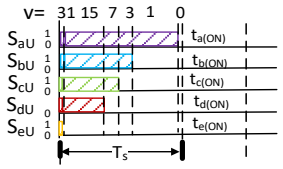

Fig. 13.Resulting switching pattern

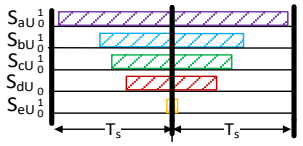

Fig. 14. An example of a switching sequence of the proposed SVPWM

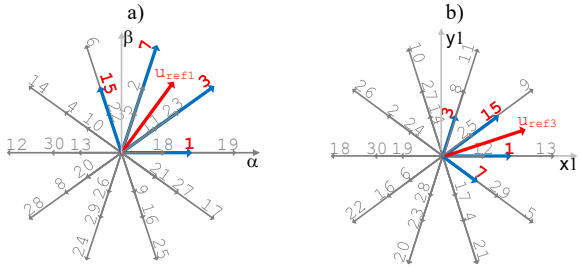

Fig. 15. The position of the reference voltage vectors and the active vectors obtained in the last step of SVPWM algorithm

For the case, where $0.2361<x\le 1.0$ the durations of zero vector is $t_0=t_{e(ON)}$ (27) and the times of gate signals are equal to (Fig. 12):

$$\begin{aligned}
t_{a(ON)} &= t_{a(ON)} - t_{e(ON)} = \frac{T_s}{u_{DC}}\left(0.7435 + 1.2030\cdot x\right)\left|u_{ref1}\right|,\\
t_{b(ON)} &= t_{b(ON)} - t_{e(ON)} = \frac{T_s}{u_{DC}}\cdot\left(0.9732 + 0.2298\cdot x\right)\left|\boldsymbol{u}_{ref1}\right|,\\
t_{c(ON)} &= t_{c(ON)} - t_{e(ON)} = \frac{T_s}{u_{DC}}\cdot\left(0.3717 + 0.6015\cdot x\right)\left|\boldsymbol{u}_{ref1}\right|\\
t_{d(ON)} &= t_{d(ON)} - t_{e(ON)} = \frac{T_s}{u_{DC}}\cdot\left(-0.2298 + 0.9732x\right)\left|\boldsymbol{u}_{ref1}\right|\\
t_{e(ON)} &= t_{e(ON)} - t_{e(ON)} = 0.
\end{aligned} \tag{29}$$

In the case of discontinuous modulation, the off-times for upper switches can be calculated as:

$$t_{x(OFF)} = T_s - t_{x(ON)},\ x = a...e, \tag{30}$$

and the algorithm ends.

In the case of continuous modulation, the vector sequence should contain both zero vectors: 00…0 (v=0) and 11…1 (v=31); their durations can be calculated using (16), and the upper switches' on-times can be determined using (17). In the analysed case, the highest values are achieved by the duration $t_{a(on)}$ or $t_{b(on)}$ regard of the x value (Fig. 11), and various equations must be analyzed depending on this coefficient value. For $0.2360<x\le 1.0$ the duration of zero vectors are calculated based on (29) and (16):

$$t_0 = 0.5\cdot\left(T_s - t_a\right) = T_s\left(0.5 - \frac{\left|u_{ref1}\right|}{u_{DC}}\left(0.3717 + 0.6015\cdot x\right)\right) \tag{31}$$

and the upper switches' on-times, including zero vector $v=31$, will be equal to (Fig. 13):

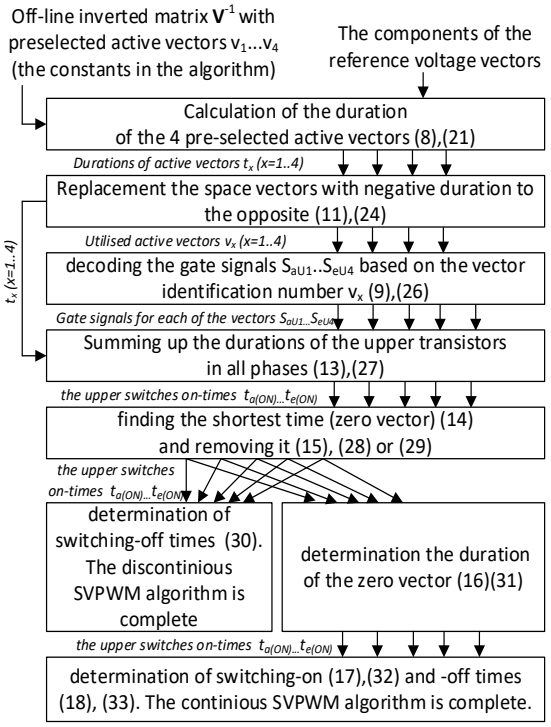

Fig. 16. Flowchart that illustrates the calculation steps in the proposed SVPWM algorithm

$$
\begin{aligned}
t_{a(ON)} &= T_s\left(0.5+\frac{|u_{ref1}|}{u_{DC}}\left(0.3717+0.6015\cdot x\right)\right),\\
t_{b(ON)} &= T_s\left(0.5+\frac{|\boldsymbol{u}_{ref1}|}{u_{DC}}\cdot\left(0.6015\text{-}0.3717\cdot x\right)\right),\\
t_{c(ON)} &= 0.5T_s\\
t_{d(ON)} &= T_s\left(0.5+\frac{|\boldsymbol{u}_{ref1}|}{u_{DC}}\cdot\left(\text{-}0.6015+0.3717x\right)\right)\\
t_{e(ON)} &= T_s\left(0.5+\frac{|\boldsymbol{u}_{ref1}|}{u_{DC}}\left(\text{-}0.3717\text{-}0.6015\cdot x\right)\right).
\end{aligned}
\tag{32}
$$

The off-times of upper switches can be calculated as:

$$t_{x(OFF)} = T_s - t_{x(ON)},\ x = a\ldots n. \tag{33}$$

The determined on/off-times can be sent to the processor timers to generate the gate signals for inverter power switches. The resulting switching pattern for $x=1.0$ (the same lengths of both reference vectors), shown in Fig. 13, can also be realized in the reverse order every odd switching period, resulting in the switching pattern shown in Fig. 14.

The resulting active and zero vectors, v, are shown in Figs. 13 and 15. They can be determined with a simple algorithm based on (9). This algorithm is not nece ssary for implementation, because most processor units include the timers which can be used to count-down the switches' on/off-times in the individual inverter phases. A flowchart that illustrates the calculation steps in the proposed SVPWM algorithm is shown in the Fig. 16.

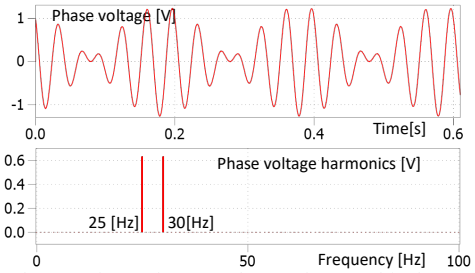

Fig. 17. The waveform of output phase voltage and its harmonics. The reference voltage frequencies are 30[Hz] (u_{ref1}) and 25[Hz] (u_{ref3}). The lengths of voltage vectors are the same – 1[V].

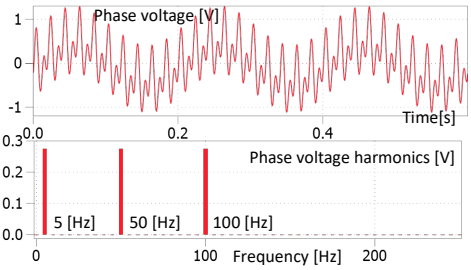

Fig. 18. The waveform of output phase voltage and its harmonics. The reference voltage frequencies are 50[Hz] (u_{ref1}) and 5[Hz] (u_{ref3}) and 100[Hz] (u_{ref5}).

Due to the x factor definition in (22), the analysis shown above is realised for $0 \le x \le 1$ (short $\mathbf{u_{ref3}}$ reference vector). The same analysis can be performed for short reference vector $\mathbf{u_{ref1}}$ by declaring the x factor as $x = \frac{|\boldsymbol{u}_{ref1}|}{|\boldsymbol{u}_{ref3}|}$.

V. DC-LINK UTILIZATION LIMITS OF A FIVE PHASE VSI

The above analysis was carried out for the worst case with respect to dc-link utilization, where the adjacent (u_{ab}) and non-adjacent line (u_{ac}) voltages reach the peak values at the same time, [25] (Fig. 7). The durations of upper transistors' gate signals generating only active vectors are given in (28) and (29). The largest of the durations $t_{a(ON)} \ldots t_{e(ON)}$ cannot exceed the switching period value T_s. In the analysed case, the highest values are achieved by the duration $t_{a(ON)}$ or $t_{b(ON)}$ regarding the x coefficient value (Fig. 11); but various equations must be analyzed depending on this coefficient value. For $0 < x < 0.2360$, (28) should be analysed. Substituting (22) in (28), one can obtain the relationship between the lengths of the reference vectors:

$$
\begin{aligned}
&t_{b(ON)} = T_s \ \text{and}\ 0 < \frac{|\boldsymbol{u}_{ref3}|}{|\boldsymbol{u}_{ref1}|} < 0.2360 \Rightarrow\\
&\Rightarrow \frac{1}{u_{DC}}\cdot\left(1.2030\left|\boldsymbol{u}_{ref1}\right| - 0.7435\cdot\left|\boldsymbol{u}_{ref3}\right|\right) = 1
\end{aligned}
\tag{34}
$$

For $|\boldsymbol{u}_{ref3}| = 0$, the maximum length of the $\mathbf{u_{ref1}}$ vector can be calculated as:

$$|u_{ref1}| = \frac{u_{DC}}{1.2030}. \tag{35}$$

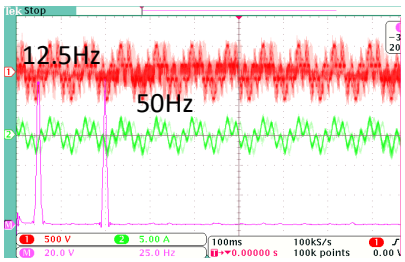

Fig. 19. The phase voltage, phase current and voltage harmonics when generating two reference voltage vectors ($f_{\alpha\beta}$=50Hz and f_{xy}=12.5Hz) using proposed SVPWM. The modulation indexes: $M_{\alpha\beta}=M_{xy}=0.5$

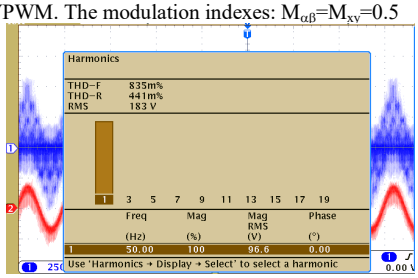

Fig.20. The results of THD analysis of a phase voltage when generating only the first output voltage harmonic. The modulation index $M_{\alpha\beta}$=0.5, M_{xy}=0, the reference frequency $f_{\alpha\beta}$=50Hz. Modulation method SVPWM

The vector u_{ref1} is located in orthogonal system. The above analysis is based on decoupling transformation matrix in power invariant form, [1],(2). Transformation of five phase voltages with the amplitudes equal to 1 gives the lengths of the voltage vector $\sqrt{2/5}$ time smaller:

$$u_{max} = \sqrt{\frac{2}{5}}|u|, \tag{36}$$

where u_{max} is maximum value of a phase voltages.

Equation (35) can be rewritten as:

$$u_{max} = \frac{u_{DC}}{1.203}\sqrt{\frac{2}{5}} = 0.5257u_{DC}. \tag{37}$$

The modulation index is defined in [20] as:

$$M = \frac{u_{max}}{0.5u_{DC}}. \tag{38}$$

Substituting (37) to (38) one can obtain:

$$M = 1.0515, \tag{39}$$

which is maximum value of modulation index in linear modulation region.

For 0.2360<x≤1.0, (29) should be analysed. Assuming, that the largest of the durations in (29), $t_{a(ON)}$, is equal to the switching period T_s and substituting (22) in (29), one can obtain the relationship between the lengths of the reference vectors:

$$t_{a(ON)} = T_s \text{ and } 0.2360 < \frac{|u_{ref3}|}{|u_{ref1}|} \le 1 \Rightarrow$$
$$\Rightarrow \frac{1}{u_{DC}}\left(0.7435|u_{ref1}| + 1.2030\cdot|u_{ref3}|\right) = 1. \tag{40}$$

[25]

When two reference voltage vectors with the same lengths $|u_{ref3}| = |u_{ref1}|$ (x=1) are generated, (40) can be rewritten as:

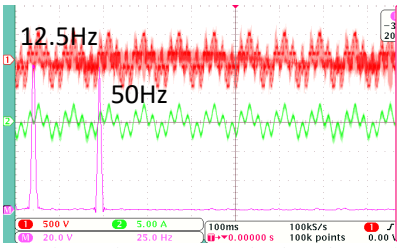

Fig.21. The phase voltage, phase current and voltage harmonics when generating two reference voltage harmonics ($f_{\alpha\beta}$=50Hz and f_{xy}=12.5Hz) using SPWM. The modulation indexes $M_{\alpha\beta}=M_{xy}=0.5$

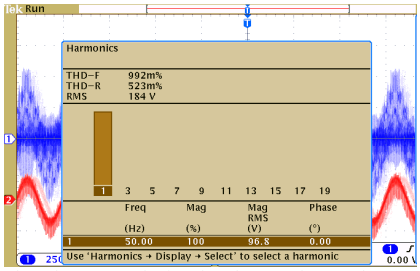

Fig.22. The results of THD analysis of a phase voltage when generating only the first output voltage harmonic. The modulation index $M_{\alpha\beta}$=0.5, M_{xy}=0, the reference frequency $f_{\alpha\beta}$=50Hz. Modulation method SPWM

Fig.23. The comparison of a phase voltage THDs of proposed SVPWM and SPWM with common-mode voltage injection when generating only the first output voltage harmonic (50Hz). The modulation indexes vary from 0.01 to 1.0515. Results of experimental tests.

TABLE I
NUMBER OF OPERATIONS COMPARISION IN SVPWM AND SPWM ALGORITHMS FOR 5-PHASE VSI

Operations:	+;-	*	Sin; cos	"if" conditions	computational time[c)]
SVPWM	33+(20)[a)]	20	0 [b)]	8+(20)[a)]	1.21µs
SPWM	26	33	0 [b]	8	1.18µs

[a)] The conditional operations are used for grouping ones in any of inverter phases. The "ones" are summed (or not) depending on the initial selection of active vectors. Not all these operations are performed during a single invocation of the SVPWM algorithm [b)] The components of both reference voltage vectors in both orthogonal spaces are determined in the higher-level control system. Both modulation methods are based on the same components of reference voltage vectors while the inverse Clark transformation is used to determine the reference phase voltages for SPWM algorithm; [c)] for ADSP21263 processor

$$|u_{ref1}| = |u_{ref3}| = \frac{u_{DC}}{1.9465}. \tag{41}$$

Hence from (36), the maximum phase voltage can be calculated as:

$$u_{max} = \frac{u_{DC}}{1.9465}\sqrt{\frac{2}{5}} = 0.3249u_{DC}, \tag{42}$$

and the modulation index, M, in(38) becomes:

$$M = 0.6498. \tag{43}$$

Thus, it can be observed that identical modulation index as shown in [25] can be obtained following the aforementioned

analytical steps.

The simulation waveform of averaged phase voltage for the switching period and its harmonics are shown in Figure 17 and 18. The lengths of both reference voltage vectors are equal to 1[V], and the dc-link voltage is equal to 1.9465 [V]; which, according to (41), provides maximum value of modulation index *M*. The Figure 18 presents the waveform of averaged phase voltage for the switching period and its harmonics, generated in a 7-phase VSI. The lengths of all reference voltage vectors was the same and equal to 0.831188[V], the dc-link voltage is equal to 1.9465 [V], which provides the maximum value of modulation index M=0.4565 given in [25]. The output voltage spectrum contains only the harmonics with the frequencies of the reference voltages.

VI. Results of experimental tests

The experimental tests of the SVPWM strategy were performed on star connected 5-phase RL (100Ω / 21mH) supplied by two-level VSI (dc-link voltage UDC=570 V, Ts=150 μs, switching frequency 3.33 kHz). Typical switching pattern is shown in the Fig 14.

On the same inverter, the SPWM method with common-mode voltage injection was implemented, which is commonly considered a replacement for space vector modulation methods.

The results of experimental tests of a five-phase VSI are compared in Figs. 19 to 23. The phase voltage, phase current and voltage harmonics when generating two reference voltage vectors with the same modulation indexes using proposed SVPWM and SPWM with common mode voltage injection are shown in Figs. 19 and 21 respectively. Figs. 20 and 22 show the THD of a phase voltage when generating only the first output voltage harmonic using both modulation strategies. The analysis of a voltage THD for both tested methods are shown on Fig. 23.

The presented results prove that the proposed SVPWM solution gives the generated voltage parameters similar to those obtained as a result of SPWM with common mode voltage injection. The same THD level of a phase voltage was achieved throughout the modulation range (Fig. 23). The slight differences in voltage THD values of the two modulation methods can only be seen if these values are approximated to 2 places of decimal fractions without a clear indication of the superiority of any of the solutions.

The computational effort is at par in both modulation schemes. The SPWM algorithm is realized in 1.18μs while the computation time of SVPWM algorithm does not exceed 1.21μs (ADSP21263 processor). Comparison of the arithmetic operation number is shown in Table I. In SVPWM, the conditional operations are used for grouping ones in any of inverter phases. The "ones" are summed (or not) depending on the initial selection of active vectors. The given execution time is a maximal time obtained during experimental test for freely chosen active vectors.

VII. Conclusions

Comparing with the classical SVPWM methods, the SPWM modulation methods are characterized by much lower processor speed and memory requirements. Therefore, it is generally accepted to use sinusoidal modulation algorithms as much easier to implement, especially in inverters with a greater number of phases and / or levels [26]. The main limitation of the applicability of SVPWM algorithms in such applications is the need to indicate the optimal sequence of active vectors before determining their durations, which in the case of multi-phase inverters turns out to be a complicated task. This problem relates to the necessity of indicating the optimal sequence of active vectors which can "be fitted" to the switching period, and for which the negative durations will not be determined. Because of this, the SVPWM methods are considered computationally complicated more than their SPWM counterparts. The SVPWM methods typically require higher speed and large memory-size processors.

This paper proposes relatively simple and fast SVPWM algorithm for multi-phase two level inverters. Compared to the classical SPWM methods with common-mode voltage injection, the proposed SVPWM algorithm has similar computational and memory-size requirements (the components of 'n-1' pre-selected vectors must be saved in memory, while the classic SPWM solutions do not require memorizing any coefficients. This means that the proposed method can be an alternative solution for widely used SPWM algorithms. It is worth noting, that the SVPWM methods provides much better insight into the behaviour of the inverter and the mapping of the voltage harmonics in different planes. In some situations, the space vector approach is useful in explaining the drive system behaviour, like in controlling of multi-motor drives supplied by the same inverter. SVPWM is a natural extension of the motor or active rectifier control algorithms, where the output variables are voltage vectors (or current vectors in the case of a Current Source Inverter, CSI) to be generated by the inverter.

The proposed solution gives output voltages with similar parameters (THD, DC-link voltage utilization) as in SPWM algorithms with zero sequence injection. Also the computational effort of the developed method is comparable to the computational effort of the SPWM method. The choice of the method has negligible effect on the quality of the output voltage. Therefore, it is impossible to clearly indicate a better method, its choice is an individual matter. For example, it may consist in the selection of the number and types of required mathematical operations.

The hybrid SVPWM solution, proposed in this paper, tries to reconcile both approaches: SVPWM and SPWM. It uses both the classical analysis known from SVPWM methods and the analysis performed separately for each inverter-leg; as obtainable in SPWM. In classical SVPWM solutions, after determining the optimal sequence of switching vectors, the

durations of active vectors are calculated and the switching times of transistors in inverter-legs are determined. The proposed algorithm reverses this process. The durations are calculated for arbitrary selected vectors, and the optimal sequence of active vectors is determined at the end of the algorithm. The optimization procedures are aimed at fitting non-optimally selected active vectors into the switching period and reducing the number of commutations. Consequently, the biggest problem of SVPWM is eliminated. There is no need to select the optimal sequence of active vectors for each position and length of the reference voltage vectors; which significantly increases computational effort of classical SVPWM algorithms. The optimal sequence of switching vectors (and therefore their optimal selection) is the result of simple transformations. As a result, the proposed method will be faster and more efficient than earlier reported SVPWM algorithms; wherein the main computational effort is focused on finding the optimal sequence of active vectors for which the durations are classically determined.

In SVPWM strategies, the minimum number of switch commutation of an *n*-phase inverter is equal to *n* (one commutation per leg in a single switching period). The commutations in '*n-1'* phases of an odd-phase inverter result in an activation/deactivation of active vectors, and one commutation causes switching-on the zero vector. If this condition is not met, a significant switching frequency change can be observed. The proposed algorithm makes it possible to generate the output voltage vectors in *n*-phase inverter utilizing *n-1* active vectors (n is an odd number). The resulting switching sequence provides only one commutation in each inverter phase-leg, and this commutation results in zero-vector activation. Thus, it can be concluded that the resultant switching sequence is optimal, and allows obtaining *(n-1)/2* reference output voltage vectors in an *n*-phase inverter (where *n* is an odd number).

The proposed solution allows an independent generation of output voltage vectors in a *n*-phase VSI. Moreover, the demonstrated method enabled the generation of sinusoidal output phase voltage (the nonzero length of output voltage vector is only in one orthogonal plane), as well as multi-frequency injection into the output voltage (the non-zero length of output voltage vectors is in several or in all orthogonal planes). The proposed solution can be utilized in drive systems where single motor with quasi-rectangular rotor field distribution or many motors with sinusoidal rotor field distribution is supplied by a single multi-phase VSI.

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