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Integrated Three-Level Dual-Phase Inverter

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Abstract: In view of reducing the number of inverter legs that provide dual-phase, three-level output voltages (as may be needed in an uninterruptible power supply), and that also provide a wide range of output frequencies (as needed in an advanced motor drive system with wide speed ranges), a three-level, dual-phase inverter topology is presented in this paper. Its three-level attribute was based on the F-type inverter topological concept, and its dual-output feature was based on the common representation of the inverter-leg concept. The proposed inverter could deliver single- and three-phase voltages to corresponding one- and three-phase loads, in common or different frequency modes of operation. A boundary between these modes of operation was established for the proposed inverter. An additional possibility of either operation in the one-phase or the three-phase system was offered by the inverter configuration. A modified carrier-based sinusoidal pulse-width modulation scheme is presented for the control of the inverter topology. The performances of the dual-phase inverter are given in the simulation results and demonstrated with a hardware prototype.

Keywords: multilevel inverter; sinusoidal pulse-width modulation; F-type inverter; total harmonic distortion

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1. Introduction

The use of a low number of power switches in nonconventional power electronics power-circuit configurations is a common concept in recent proposed converter topologies. Cost, size, and weight optimization are the prime driving factors behind this technological trend. In addition, a reduction in the failure rate probability of the converter system is also a contributing factor. This power electronics topological trend paved way to a series of two-in-one converter configurations; otherwise called dual-terminal converters. These are converters that have two AC terminals that are interfaced with DC in the power-conversion process: AC–DC–AC power-converter systems. Associated voltages and currents at the two AC terminals can have the same or different frequencies. For the time being, three conceptual approaches have been deployed in configuring these converter power circuits, namely: the split-capacitor-bank approach [1–4], the parallel-common-phase-leg approach [5], and the series-common-switch approach [6–9].

For two-level converter operation, a series of applications have been explored with these converter systems. The split-capacitor-bank-based dual-terminal converter configurations have been deployed in single- to three-phase rectifier/inverter [1], dual-inverter [4], and three-phase-rectifier/inverter [2,3] drive systems. Similarly, dual-terminal converter topologies based on the parallel-common-phase-leg approach have been utilized in single [5] and three-phase [6], rectifier/inverter drive systems. Extensive deployment of dual-terminal converter configurations with a series-common-switch background can be seen in these converter applications: power conditioner [10]; energy systems for distributed generation [11]; dual-output indirect matrix converter [12]; back-to-back converter for DFIG [13]; online UPS [14], and multi-phase drive systems [15].

In view of the general limitations of the operational performance indices of two-level inverters, multilevel inverters (MLIs) became alternative power-conditioning devices [16].

The diode- and capacitor-clamped MLI topologies conceptually fit into single-DC-source operation. Three-level variant configurations of these single-DC-sourced MLIs are used the most to serve MLI power circuits; as the synthesis of the output voltage level increases, the inherent undue voltage fluctuations in the constituting clamping capacitor banks become a limiting factor [17]. The three-level diode-clamped inverter, often referred to as the neutral-point-clamped (NPC) inverter, has been well researched and deployed in various industrial applications, including its derived dual-inverter system [18]. Though all the switches in an NPC inverter have a voltage rating of half the applied DC input voltage, the high conduction losses and occupied design space of the clamping diodes are of technical concern. In [19], a compact three-level, T-type MLI configuration was implemented with output characteristics that were on par with those of the NPC. The absence of the passive diodes in the T-type inverter topology is compromised with a full-input DC voltage rating of two of its constituting switches in a phase leg. In low- and medium-voltage high-power applications, the T-type inverter is the preferred choice, since within this voltage range, discrete IGBT switches and modules with up to 6.5 kV and 1200 A ratings exist, courtesy of the recent advancements in power-switch fabrication.

Similar to the power-conversion system in [18], the work in [20] presented a classical dual-output, three-level inverter system based on two independent T-type inverters that shared a common input DC source. Twenty-four active power switches were involved; of these, 50% had to withstand the overall input DC voltage stress, and were rated accordingly. In order to sustain a high tempo in the advanced search for optimized three-level, dual-terminal converter systems, commensurate power electronics power circuits with reduced component counts are imperative. Using the series-common-switch conceptual approach, the work in [21] explored the possibility of creating two independent load systems using an active-clamped NPC. Therein, the clamping diodes were replaced with active switches, and the two upper and lower switches in a classical NPC were separated by a common IGBT switch in each of the inverter phase legs. The cathode and emitter of this common switch were the respective output node terminals, in each phase, of the two independent inverters. Depending on their modulation indices, each inverter could generate three- or five-level output line voltage waveforms, and the control approach was explicitly classic and simplified. A similar dual-output inverter topology was presented in [22]. Therein, a mixture of diodes and shared active power switches were properly deployed to create two independent load systems. However, this series-common-switch approach inherently imposed limitations on this power circuit's switching-states operation. This limitation was reflected in its loose grip on the neutral-point voltage control, and also impeded its capability for different frequency modes of operation.

As demonstrated in [6], the number of inverter legs needed to configure a dual-terminal converter using the split-capacitor-bank conceptual approach was one less than that required in configuring the same dual-terminal converter using the parallel-common-phase-leg conceptual approach. However, the overall performance of this approach was superior to that of the configuration that used the split-capacitor-bank approach [6]. Considering all the aforementioned, this paper proposes a three-level, dual-phase inverter—3-L DPI—the topological concept of which hinged on the parallel-common-phase-leg approach, and its base conceptual power circuit was derived from the three-level F-type inverter, [23]. Two phase systems were involved in the dual-output power conversion: single- and three-phase. Both phase systems had a common three-level F-type inverter leg that resulted in a reduced component-count for the entire inverter system. A pair of three-level, one- and three-phase output voltage waveforms, of variable magnitudes and frequencies, could be generated using the proposed inverter power circuit, which had a total of 16 active power switches. The absence of one F-type inverter-leg translated to a savings of four active power switches in the 3-L DPI topology. Since the base inverter leg was the F-type, this newly configured power circuit had an inherent low cost and loss performance, as

demonstrated in [23]. The operational modulation index range for the 3-L DPI was developed that dictated the dynamic output-voltage level syntheses in both phase systems. Both inverters could simultaneously attain the maximum modulation indices of 1 and 1.1547 for one- and three-phase systems, respectively, if both inverters worked at the same frequency. For variable frequencies, either of these modulation indices could be reached by the corresponding inverters; the maximum modulation indices in the two inverters summed up to 1.5118 in this operation mode. These control attributes of the proposed 3-L DPI were enshrined in the developed boundary definitions of the operational modes of the inverter. Control of the neutral-point voltage imbalance and low-frequency oscillation of the DC-link capacitor voltages during operation were achieved by the deployment of carrier-based pulse-width modulation (CBPWM) [23]. In the next sections, the organization of this paper is as follows: the power circuit configuration and operational principle are presented in Section 2; the deployed CBPWM scheme is presented in Section 3; and the simulation and experimental results are presented in Section 4.

2. Proposed Three-Level Dual-Output Inverter Configuration

A leg of the proposed three-level dual-phase inverter is given in Figure 1a. It had three input terminals: P, n, and N, corresponding to the positive, midpoint (neutral-point), and negative-input DC (V_{dc}) rails. Normally, V_{dc} is split by capacitor banks with a midpoint of n. Node x is the output node terminal. In two-switch combinational operation, this unit leg configuration outputs three voltage values with reference to node n. $x_n = 0.5V_{dc}$ if g_1 and g_3 are turned on; $x_n = 0$ when g_2 and g_3 are in the on-state; and $x_n = -0.5\ V_{dc}$ if g_2 and g_4 are switched on. These voltage level syntheses are respectively referred to as the positive, zero, and negative voltage states of the inverter unit. The switching operational principle is summarized in Table 1. The unit inverter leg power circuit in Figure 1a was the F-type three-level inverter leg presented in [23]. Therein, the switching-state transitions between the voltage states of the inverter unit were explicitly demonstrated. Herein, this three-level, F-type inverter leg was utilized to configure a reduced-component-count 3-L DPI topology. Figure 1b shows the power-circuit configuration of the proposed three-level, dual-phase inverter. Precisely, it consisted of F-type-based one- and three-phase inverters that were classically fed from common-input DC bus rails. Both were respectively configured to deliver three-level, one- and three-phase output voltage waveforms to corresponding one- and three-phase loads. The common inverter leg dually and simultaneously served both phase systems: inverters 1 and 2. This resulted in the use of 16 active power switches to synthesize these output voltage waveforms with variable amplitudes and frequencies. These output parameter indices could be the same or quite different in the two inverters. The common inverter leg was not particularized to any phase in inverter 2; only one phase could be common in both phase systems in order to eliminate four power switches. Hence, this concept also could be extended to either phase b or c in inverter 2. In addition to component-count reduction, this inverter configuration offered the additional advantage of providing an optional possibility of generating only three output line voltages in the three-phase system, or only a voltage waveform in the single-phase system, if the need arose to isolate either of the phase systems. In other words, if, as shown in Figure 1b, inverter 1 was open/isolated from the circuit, three five-level line voltage waveforms were still generated properly by inverter 2. Similarly, if inverter 2 was open/isolated from the circuit, a single five-level voltage waveform was generated properly from inverter 1.

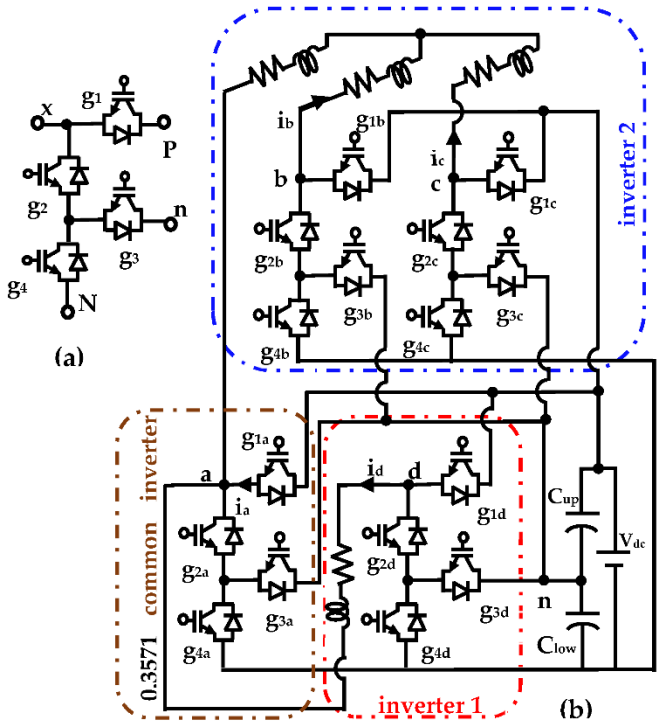

Figure 1. Power circuit of the proposed 3-level, dual-phase inverter: (**a**) inverter leg; (**b**) 3-level, dual-phase inverter.

Table 1. Operational switching state and output voltage generation in the unit inverter leg.

Inverter State	g_1	g_2	g_3	g_4	Output Voltage
Positive	1	0	1	0	$0.5\ V_{dc}$
Zero	0	1	1	0	0
Negative	0	1	0	1	$-0.5\ V_{dc}$

Similar dual-phase inverter configurations using the three-level diode-clamped and T-type inverter legs are shown in Figure 2. The operational principles (switching sequences) of these inverter legs were still conserved. Functionally, the same control/modulation approach could be deployed in all the inverter configurations shown in Figures 1 and 2. However, the topological features, including the cost and loss performances of these inverter legs, differed significantly, as explicitly demonstrated in [23].

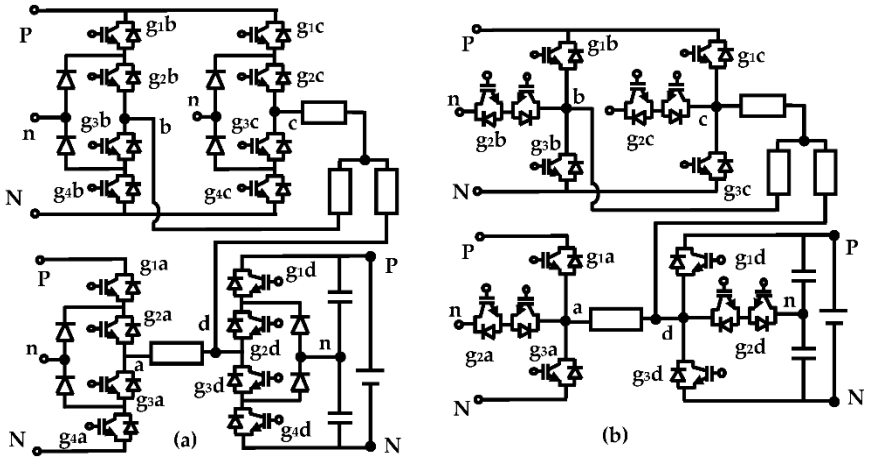

Figure 2. Dual-phase inverters with different inverter-legs; (**a**) 3-level diode-clamped; (**b**) T-type.

3. Sinusoidal PWM Strategy for the Proposed Three-Level, Dual-Phase Inverter

A lower computational burden, an individualized phase-leg operation, and ease of adaptability to multilevel/multiphase output voltage synthesis are the most cherished features of sinusoidal PWM (SPWM), and when viewed in relation to space vector PWM (SVPWM). These modulation schemes' performance equivalence has been shown [24], and the necessary criterion for this equality lay on the modification of the supposed sinusoidal reference signals in SPWM. Within the linear modulation region, extension of the modulation index range above unity with SPWM demanded addition of the zero-sequence component in the reference signals, following the min–max function principle [24]. This condition equates SPWM and SVPWM in view of the utilization of the DC-link voltage. The SPWM scheme presented in [23] fits well in the control of the proposed inverter. In addition to the min–max function modification, calculated off-set signals and voltage deviations were properly added to the modulating waveforms, which ensured stabilized and good operation of the inverter. In the proposed control scheme, inverters 1 and 2 were treated as two separate three-level, one- and three-phase F-type inverters. Since there were one and two F-type inverter legs in inverters 1 and 2, corresponding one and two reference sinusoidal waveforms, respectively, were needed to control these inverters. These references were obtained as follows.

If one- and three-phase, three-level F-type inverters were classically connected to deliver independent one- and three-phase output voltages, the needed reference signals were:

$$v_{a1} = m_1 \sin\ \omega_1 t \tag{1a}$$

$$v_{b1} = m_1 \sin(\ \omega_1 t - \pi) \tag{1b}$$

$$v_{a2} = m_2 \sin\ \omega_2 t \tag{2a}$$

$$v_{b2} = m_2 \sin(\ \omega_2 t - 2\pi/3) \tag{2b}$$

$$v_{c2} = m_2 \sin(\ \omega_2 t + 2\pi/3) \tag{2c}$$

where ω and m are the frequency and modulation index; subscripts 1 and 2 denote inverters 1 and 2, respectively.

The maximum modulation index value for the three-phase system was $(1/\cos(\pi/6)$; that is, 1.1547, [25]; and of course, 1 for the single-phase system. The voltage references in (1a,b) and (2a–c) were modified to fit appropriately in the control of the power circuit shown in Figure 1b. In this proposed circuit, one inverter leg was common to both inverters. Hence, modification of the reference phase voltage signals for the one-phase system was:

$$v_{a,\ inv1} = m_1 \sin\ \omega_1 t + m_2 \sin\ \omega_2 t \tag{3a}$$

$$v_d = m_1 \sin(\ \omega_1 t - \pi) + m_2 \sin\ \omega_2 t \tag{3b}$$

For the 3-phase system, the modification was:

$$v_{a,inv2} = m_2 \sin\ \omega_2 t + m_1 \sin\ \omega_1 t \tag{4a}$$

$$v_b = m_2 \sin(\ \omega_2 t - 2\pi/3) + m_1 \sin\ \omega_1 t \tag{4b}$$

$$v_c = m_2 \sin(\ \omega_2 t + 2\pi/3) + m_1 \sin\ \omega_1 t \tag{4c}$$

In the derived sets of reference waveforms, $v_{a,inv1}$ is equal to $v_{a,inv2}$. With reference to the neutral point, n, this implied that $v_{an,inv1}$ in inverter 1 is equal to $v_{an,inv2}$ in inverter 2. In addition, the corresponding output voltage of inverter 1, v_{ad}, is given in (5) and the output line voltages (v_{ab}, v_{bc}, v_{ca}) in inverter 2 are given in (6a–c):

$$v_{ad,} = v_{a,\ inv1} - v_{d,\ inv1} = m_1\{\sin\ \omega_1 t - \sin(\ \omega_1 t - \pi)\} \tag{5}$$

$$v_{ab} = v_{a,\,inv2} - v_{b,\,inv2} = m_2 \left\{ \begin{array}{c} \sin\ \omega_2 t \\ -\sin(\ \omega_2 t - 2\pi/3) \end{array} \right\} \tag{6a}$$

$$v_{bc} = v_{b,\,inv2} - v_{c,\,inv2} = \ m_2 \left\{ \begin{array}{c} \sin(\ \omega_2 t - 2\pi/3) \\ -\sin(\ \omega_2 t + 2\pi/3) \end{array} \right\} \tag{6b}$$

$$v_{ca} = v_{c,\,inv2} - v_{a,\,inv2} = \ m_2 \left\{ \begin{array}{c} \sin(\ \omega_2 t + 2\pi/3) \\ -\sin\ \omega_2 t \end{array} \right\} \tag{6c}$$

Hence, with four modulating signals $(v_{a,inv1}, v_d,\ v_b, v_c)$, the three-phase line voltages and a single-phase voltage were delivered at the load terminals of inverters 2 and 1, respectively, shown in Figure 1b. The frequencies and magnitudes of these voltage waveforms in both phase systems could be the same or different in both inverters, depicting two modes of frequency operation. Thus, there was a need to establish the limits and boundary between these operational modes.

The phasor diagram of the phase voltages in the three-phase system is shown in Figure 3a. Since the system was balanced, all the line voltages were of the same magnitude; it was sufficient to consider only v_{ab} referenced to phase $v_{a,inv2}$. As shown in Figure 3a, the line-phase voltage relationship is given in (7):

$$/v_{ab}/ = /v_{a,\ inv2}/\sqrt{3} \tag{7}$$

Considering the dual-phase system, the horizontal component of v_{ab} was in the same direction as the interfacing node $v_{a,inv1}$ voltage of inverter 1. The components of the system's voltage magnitude, v_s, are depicted in Figure 3b; the magnitude is given in (8) in terms of the shared node voltage. Note that (3a) and (4a) are equal.

$$\begin{array}{l} /v_s/ = \sqrt{\left(v_{ab}\sin\left(\frac{\pi}{6}\right)\right)^2 + \left(v_{ab}\cos\left(\frac{\pi}{6}\right) + v_{a,\ inv1}\right)^2} \\ = \sqrt{7}/v_{a,\ inv2}/ \end{array} \tag{8}$$

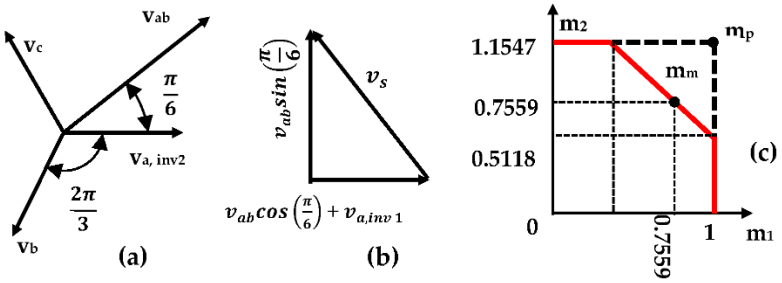

Figure 3. Operational boundary definition: (**a**) 3-phase phasor diagram; (**b**) components of the system's voltage magnitude, v_s; (**c**) boundaries of the different and common frequency modes of operation.

By definition, the phase system modulation index, m_s, is defined as the ratio of the phase voltage fundamental peak value, $/v_{a,inv2}/$, and one-half of the DC bus voltage, V_{dc}; that is:

$$m_s = \frac{/v_{a,\ inv2}/}{0.5V_{dc}} \tag{9}$$

For different frequency-mode operations in both phase systems, maximum utilization of the input DC voltage was reached when the peak value of the system's voltage magnitude, v_s, became equal to the input DC voltage, V_{dc}, a condition that set the limit of the linear modulation region. Thus:

$$/v_s/ = /v_{a,\ inv2}/\sqrt{7} = V_{dc} \tag{10}$$

When $/v_{a,\ inv2}/$ is substituted in (10) from (9), the system maximum modulation index, $m_{s,peak}$, is given as:

$$m_{s,peak} = 0.7559 \tag{11}$$

This is the maximum modulation index for inverters 2 and 1 in this different frequency-mode operation. If m_1 and m_2 are the modulation indices for inverters 1 and 2, respectively, then:

$$m_1 + m_2 \leq 1.5118 \tag{12}$$

Using (12), the variation in the modulation indices in the proposed dual-phase system is shown in Figure 3c. Therein, the area bounded by the solid-red-colored lines and the two axes defined the region where the different frequency operational mode was possible. Beyond this region, the dual-phase system had to be run in the common frequency mode operation. Depending on the combination of the modulation index values (m_1 and m_2) in this figure, three- or five-level single-phase and line-to-line three-phase voltage waveforms could be synthesized in inverters 1 and 2, respectively. Point m_m indicated the maximum equal modulation index values in both phase systems for different frequency operational modes; whereas at point m_p, the two inverters reached their respective attainable modulation index values within the linear modulation range. With v_d for inverter 1 leg, v_b and v_c for inverter 2 legs, and $v_{a,inv2}$ for the common inverter leg, the modulation concept presented for the F-type inverter in [23] was used individually to generate the gating pulses for the power switches in the proposed dual-phase power circuit. The typical reference phase voltage waveforms for inverters 1 and 2 are shown in Figure 4. $v_{a,inv2}$, v_b, v_c, and v_d were the needed phase voltage references for the modulation scheme. These waveforms depict $\omega_2 > \omega_1$ operations; those for $\omega_1 > \omega_2$ operations followed suit. Figure 4a–c corresponds to the same operational point whereby inverter 2 operated at a higher frequency than inverter 1. The obtained references, from (3a,b) and (4a–c), for inverters 1 and 2 are shown in Figure 4a,b, respectively. The needed phase voltage reference signals for the dual-phase system are combined in Figure 4c. Similar displays are shown in Figure 4d–f for the two inverters operating at different modulation indices and frequencies.

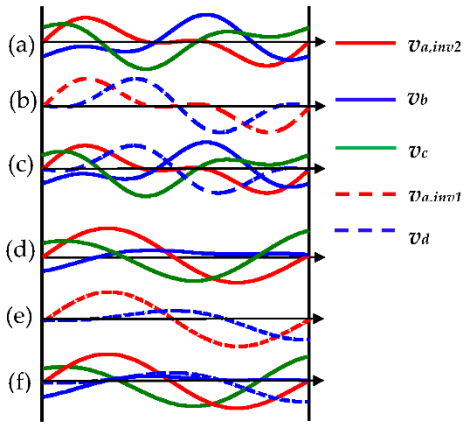

Figure 4. Typical reference phase voltage waveforms for inverters 1 and 2 for different frequency and modulation index operations.

$$(a\text{–}c)\ m_1 > m_2 \text{ and } \omega_2 = 2\omega_1;\ (\text{d–f})\ m_1 > m_2 \text{ and } \omega_2 = 1.25\omega_1.$$

It can be observed in Figure 4a,d that the lower-frequency-operated inverter's reference waveform periods were sectored into six equal intervals, as was obtained in [26,27]. Each sector spanned a 60° interval. Any sector N ($N = 1, 2, \ldots, 6$) was defined as

$$(N - 0.5) * 60^\circ \leq \theta < (N + 0.5) * 60^\circ \tag{13}$$

Similar interval sectoring was extended to the combined waveforms shown in Figure 4c,f. The four references, ($v_{a,inv2}$, v_b, v_c, and v_d) were sequentially compared to determine these sectors, as well as their intervals. For a period of the lower-frequency-operated inverter, the four references were sampled to determine the most positive (maximum) and most negative (minimum) reference waveforms. The determined maximum (max) and minimum (min) reference signals during the sampling period clearly specified the sectors. Simple comparison and logic AND expressions in (14) and (15) could be used to determine the max and min.

$$\left\{ \begin{array}{l} if \left\{ \begin{array}{l} (v_{a,\ inv1} > v_{b,\ inv1}).(v_{a,\ inv1} > v_{c,\ inv1}) \\ .(v_{a,\ inv1} > v_{a,\ inv2}).(v_{a,\ inv1} > v_{c,\ inv2}) \end{array} \right\} \max = v_{a,\ inv1} \\ \qquad\qquad . \\ \qquad\qquad . \\ \qquad\qquad . \\ if \left\{ \begin{array}{l} (v_{c,\ inv2} > v_{a,\ inv1}).(v_{c,\ inv2} > v_{b,\ inv1}) \\ .(v_{c,\ inv2} > v_{a,\ inv2}).(v_{c,\ inv2} > v_{b,\ inv2}) \end{array} \right\} \max = v_{c,\ inv2} \end{array} \right\} \tag{14}$$

$$\left\{ \begin{array}{l} if \left\{ \begin{array}{l} (v_{a,\ inv1} < v_{b,\ inv1}).(v_{a,\ inv1} < v_{c,\ inv1}) \\ .(v_{a,\ inv1} < v_{a,\ inv2}).(v_{a,\ inv1} < v_{c,\ inv2}) \end{array} \right\} \min = v_{a,\ inv1} \\ \qquad\qquad . \\ \qquad\qquad . \\ \qquad\qquad . \\ if \left\{ \begin{array}{l} (v_{c,\ inv2} < v_{a,\ inv1}).(v_{c,\ inv2} < v_{b,\ inv1}) \\ .(v_{c,\ inv2} < v_{a,\ inv2}).(v_{c,\ inv2} < v_{b,\ inv2}) \end{array} \right\} \min = v_{c,\ inv2} \end{array} \right\} \tag{15}$$

With max and min computed, the sectors $S_{max,min}$ were specified and tagged with two phase notations/labels (a,inv_2, b, c, and d) corresponding to the prevailing maximum and minimum phase voltage references given in Figure 4c or Figure 4f during the comparison period of the four reference signals. As mentioned earlier, the number of sectors, $S_{\max,\min}$, precisely depended upon the frequency of the higher-frequency-operated inverter. Each of the four reference signals were compared with the max and min to determine the sectors and their intervals. A generalized expression for the sector computations is given in (16):

$$\left\{ \begin{array}{l} if \left\{ \begin{array}{l} (v_{a,\ inv2} == \max).(v_b == \min)\ S_{a,\ inv2;b} = 1 \\ (v_{a,\ inv2} == \max).(v_c == \min)\ S_{a,\ inv2;c} = 1 \\ (v_{a,\ inv2} == \max).(v_d == \min)\ S_{a,\ inv2;d} = 1 \end{array} \right\} \\ \qquad\qquad . \\ \qquad\qquad . \\ \qquad\qquad . \\ if \left\{ \begin{array}{l} (v_d == \max).(v_{a,\ inv2} == \min)\ S_{d;a,\ inv2,} = 1 \\ (v_d == \max).(v_b == \min)\ S_{d;b} = 1 \\ (v_d == \max).(v_c == \min)\ S_{d;c} = 1 \end{array} \right\} \end{array} \right\} \tag{16}$$

In the following, a recap of the modulation scheme in [23] and its modifications to adapt to the control of the dual-phase, three-level inverter are presented.

Each inverter leg had two modulating waveforms that were used to generate the positive and negative half-cycles of the inverter-leg output voltage. These waveforms, given in (17a,b), were obtained by subtracting the max and min values in (14) and (15) from the inverter-leg reference voltage waveforms derived in (3a,b) and (4a–c). Subscript x in (17a,b) connotes the phase notations (a,inv_2, b, c); and pos, neg denotes the positive and negative half-cycles.

$$MOD_{x,pos} = 0.5 * (v_x - \min) \tag{17a}$$

$$MOD_{x,neg} = 0.5 * (v_x - \max) \tag{17b}$$

Restoration of the balance over the DC-link capacitor voltages was achieved by adding an unbalanced compensation signal, $v_{com}i_x$, to (17a,b), and modifying these equations as:

$$MOD^{*}_{x,pos} = 0.5 * (v_x - \min) - v_{com}i_x \quad (18a)$$

$$MOD^{*}_{x,neg} = 0.5 * (v_x - \max) - v_{com}i_x \quad (18b)$$

$$v_{com} = (v_{C,low} - v_{C,up})k_{com} \quad (18c)$$

where i_x is the respective phase current; $v_{C,low}$ and $v_{C,up}$ are the lower and upper splitting capacitor bank voltages in Figure 1b; and k_{com} is a proportional gain. The effects of the unbalanced compensation signal in (18a–c) were accommodated by incorporating offset signals $v_{com}i_{pos}$ in (18a) and $v_{com}i_{neg}$ to (18b), resulting in:

$$MOD^{**}_{x,pos} = 0.5 * (v_x - \min) - v_{com}(i_x - i_{pos}) \quad (19a)$$

$$MOD^{**}_{x,neg} = 0.5 * (v_x - \max) + v_{com}(i_x - i_{neg}) \quad (19b)$$

The currents i_{pos} and i_{neg} were determined in every sector as the currents of the particular phases for which their voltage reference signals attained their minimum and maximum values, respectively, in Figure 4c or Figure 4f. These currents could be determined at each of the sectors in (16) shown in Table 2.

Table 2. Sector-dependent currents.

	i_{pos}	i_{neg}
$S_{a,inv2;b}$	i_b	$i_{a,inv2}$
$S_{a,inv2;c}$	i_c	$i_{a,inv2}$
$S_{d;b}$	i_b	i_d
$S_{d;c}$	i_c	i_d

In Figure 5, the modulation signals of inverter legs b and d were typified for $m_1 > m_2$ and $\omega_2 > \omega_1$; such existed for other inverter legs. The switching signals to the power switches in Figure 1b were obtained by comparing the respective modulating waveforms with the triangular carrier signal in a simple logic operations as:

$$g_1 = mod^{**}{}_{x,pos} > T \quad (20a)$$

$$g_2 = !g_1 \quad (20b)$$

$$g_4 = mod^{**}{}_{x,neg} < T \quad (20c)$$

$$g_3 = !g_4 \quad (20d)$$

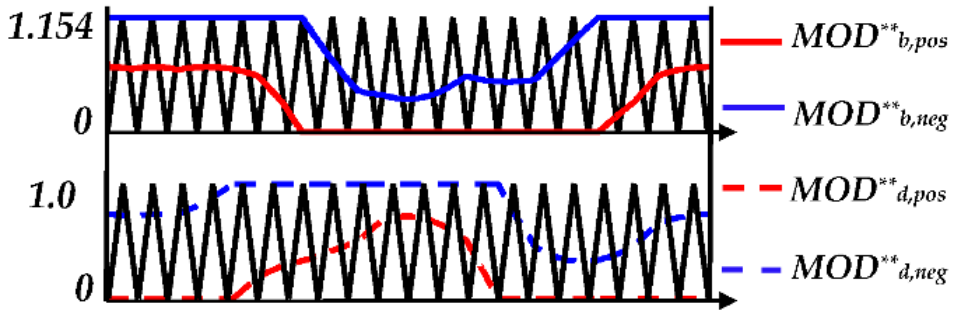

Figure 5. Typical modulating waveforms for inverter legs b and d for $m_1 > m_2$ and $\omega_2 > \omega_1$.

A flowchart that shows all the necessary steps for generating the gating signals of the inverter power switches is given in Figure 6.

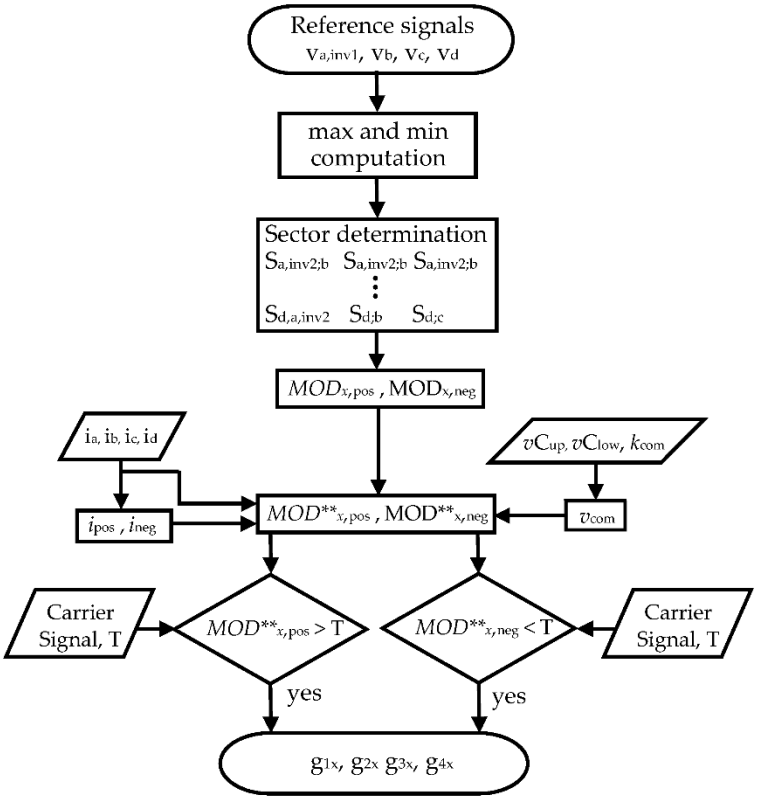

Figure 6. Flowchart of the modulating scheme.

4. Simulation and Experimental Results

In this section, a simulation and experimental investigations of the working and control principles of the dual-phase, three-level inverter are carried out. In these studies, the adopted modified SPWM modulation scheme was appropriately executed in the control algorithms. A laboratory prototype of the dual-phase, three-level inverter was built, wherein the experimental inverter output waveforms were obtained. These laboratory waveforms matched well with the inverter-simulated output waveforms.

4.1. Simulation Results

In a PLECS simulation environment, power and control circuit models of the dual-phase, three-level inverter shown in Figure 1b were developed. These models were in conformity with the configuration, operational principles, and control scheme of the dual-phase inverter outlined in Sections 2 and 3. The DC-link voltage value was 400 V, and the splitting capacitor banks' capacitance values were 1000 µF each. Inverter 2 was loaded with a three-phase RL load with 20 Ω resistance and 20 mH inductance; inverter 1 had the same single-phase load value. Both phase systems had a carrier frequency of 5 kHz at varying modulation indices.

The simulated output voltage and current waveforms for the dual-phase system's operation at points m_p and m_m given in Figure 3c are shown in Figure 7a. For point m_p, a 50 Hz fundamental frequency was used in both inverters at peak modulation indices of 1.1547 and unity for inverters 2 and 1, respectively. Frequencies of 50 and 100 Hz were used at point m_m for inverters 2 and 1; and both had the same modulation index of 0.7559. Figure 7b shows the output voltage waveforms of the two inverters for another set of different frequency operations, as indicated in the figure caption. Their respective load current waveforms are shown in Figure 7c. The capacitor banks' voltage waveforms are shown in Figure 7d. These voltage profiles depict the tight grip of the presented SPWM control scheme on the neutral-point voltage balancing as the inverter transited from one point of operation to another.

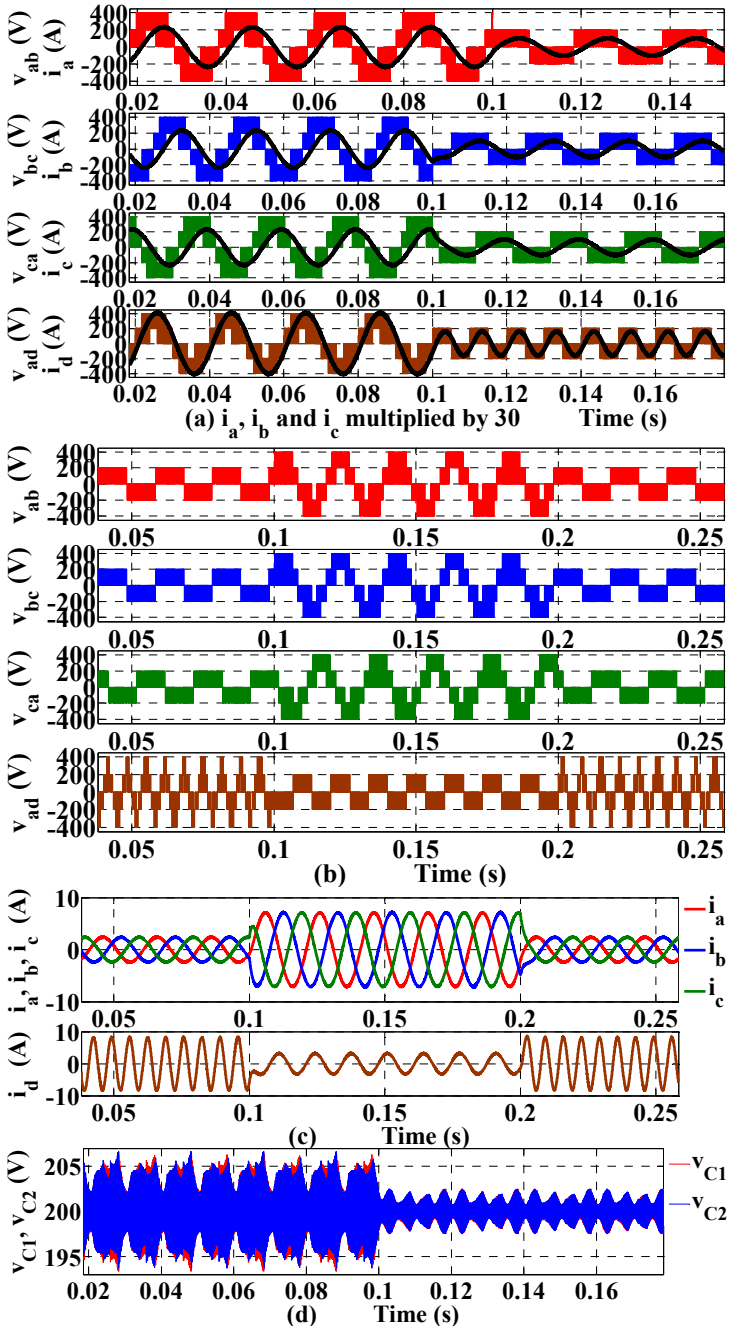

Figure 7. Simulated output voltage and current waveforms of the dual-phase inverter for common and different frequency operations. (**a**) Common 50 Hz and modulation indices of 1.1547 and 1 at frequencies of 50 and 100 Hz, with common modulation index of 0.7559; (**b**,**c**) different frequencies of 50 and 150 Hz, with modulation indices of 0.35 and 0.8 at different frequencies of 50 and 75 Hz, with modulation indices of 1.05 and 0.25; (**d**) capacitor banks' voltages in (**a**).

As noted in Section 1, the proposed inverter offered an additional advantage of providing an optional possibility of isolating either of the constituting inverters if the need for this operating condition arose. However, the common inverter leg was required to be in place in order to explore this operation. Figure 8a shows the output voltage and current waveforms for either operation of inverters 1 and 2. The result of the FFT analysis of the line voltage, v_{ab}, of inverter 2 is displayed in Figure 8b.

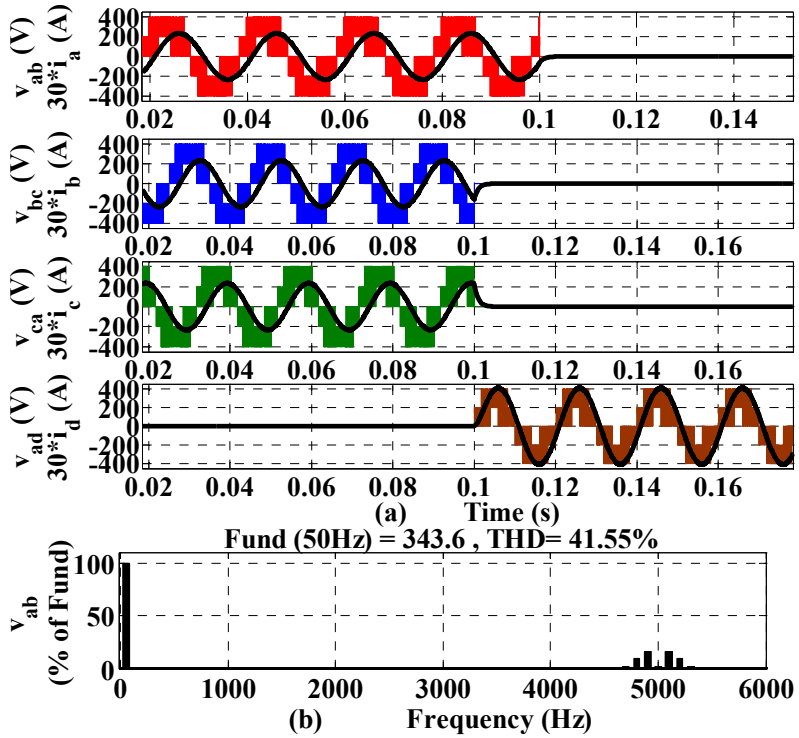

Figure 8. (**a**) Simulated voltage and current waveforms for either operation of the two inverters for common frequency of 50 Hz and modulation indices of 1.1547 and 1, (**b**) corresponding FFT profile of the line voltage waveform, v_{ab}, for this point of operation.

4.2. Experimental Results

Following the determination of the dual-phase inverter's power circuit simulation parameters, a laboratory prototype of the inverter was built; a photo of this prototype is shown in Figure 9a. An onboard ADSP21363L DSP processor and an Altera Cyclone II FPGA were used to implement the SPWM control scheme. Table 3 gives the prototype parameters and specifications. The dual-phase inverter's operational points m_p and m_m (depicted in Figure 3c) were experimentally demonstrated at a common frequency of 50 Hz for point m_p and at 75 and 100 Hz for point m_m. The output voltage and current waveforms are shown in Figure 9b,c. The corresponding capacitor banks' voltage variations are shown in Figure 9d.

Table 3. Prototype specifications.

Component	Specification
Power switches	NGTB25N120FL3WG
Fundamental frequencies	50, 75, 100, 150 Hz
Carrier frequency	5 kHz
Capacitor bank	1000 μF, 600 V
switching frequency	5 kHz
Carrier frequency	
RL load	20 Ω, 20 mH
DC-link voltage	400 V

The displayed dynamic capacitor voltage profiles depicted a good performance of the deployed modulation scheme. Further dynamic variation and swapping of the inverters' modulation index values at different frequency-mode operations are typified in the output voltage and current waveforms shown in Figure 10.

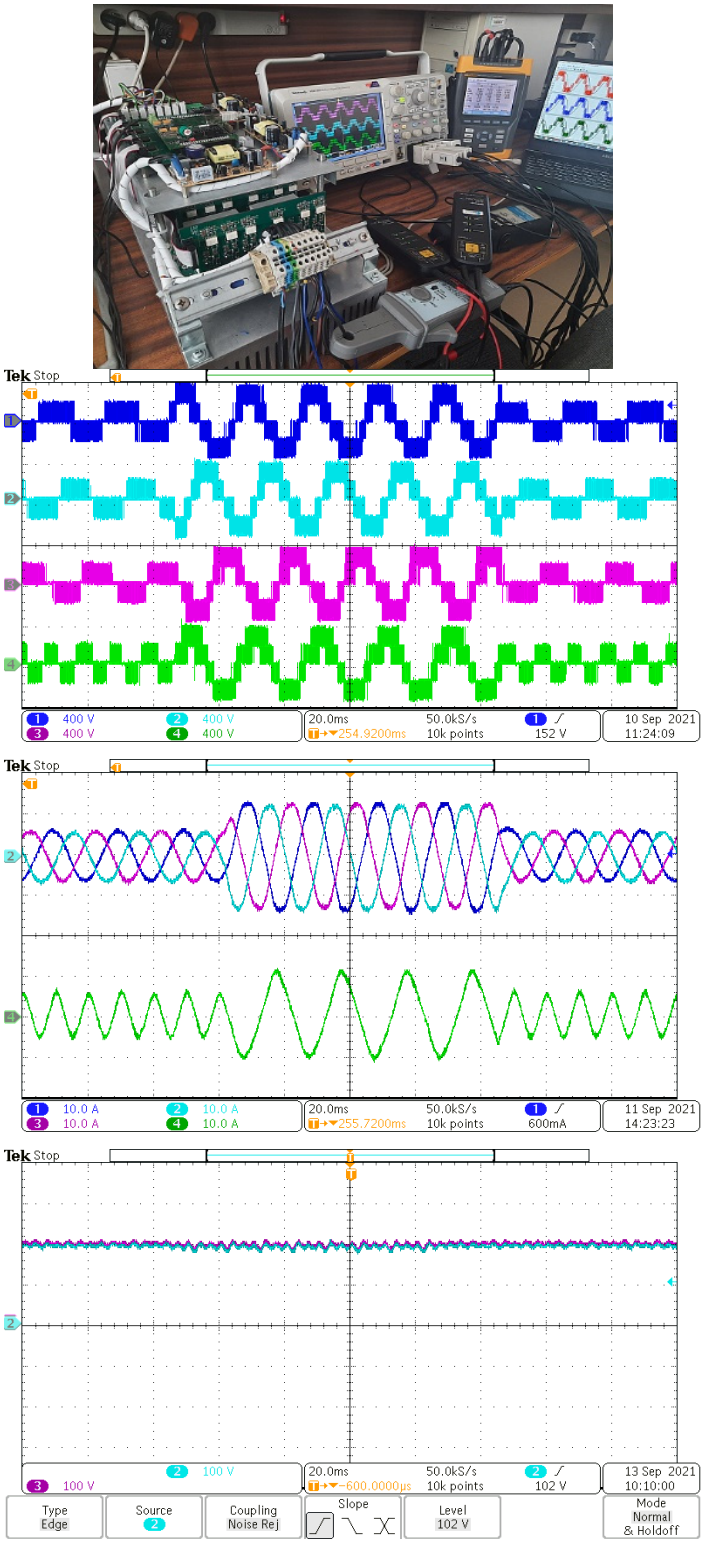

Figure 9. Prototype setup, experimental output voltage and current waveforms of the dual-phase inverter for common and different frequency operations, and capacitor-bank voltages. (**a**) Inverter prototype setup; (**b**,**c**) output voltages and current waveforms for common-frequency (50 Hz) operation and different modulation indices of 1.1547 and 1, and for the common modulation index (0.7559) and different 50 and 100 Hz frequency operations for inverters 1 and 2; (**d**) corresponding capacitor banks' voltage waveforms.

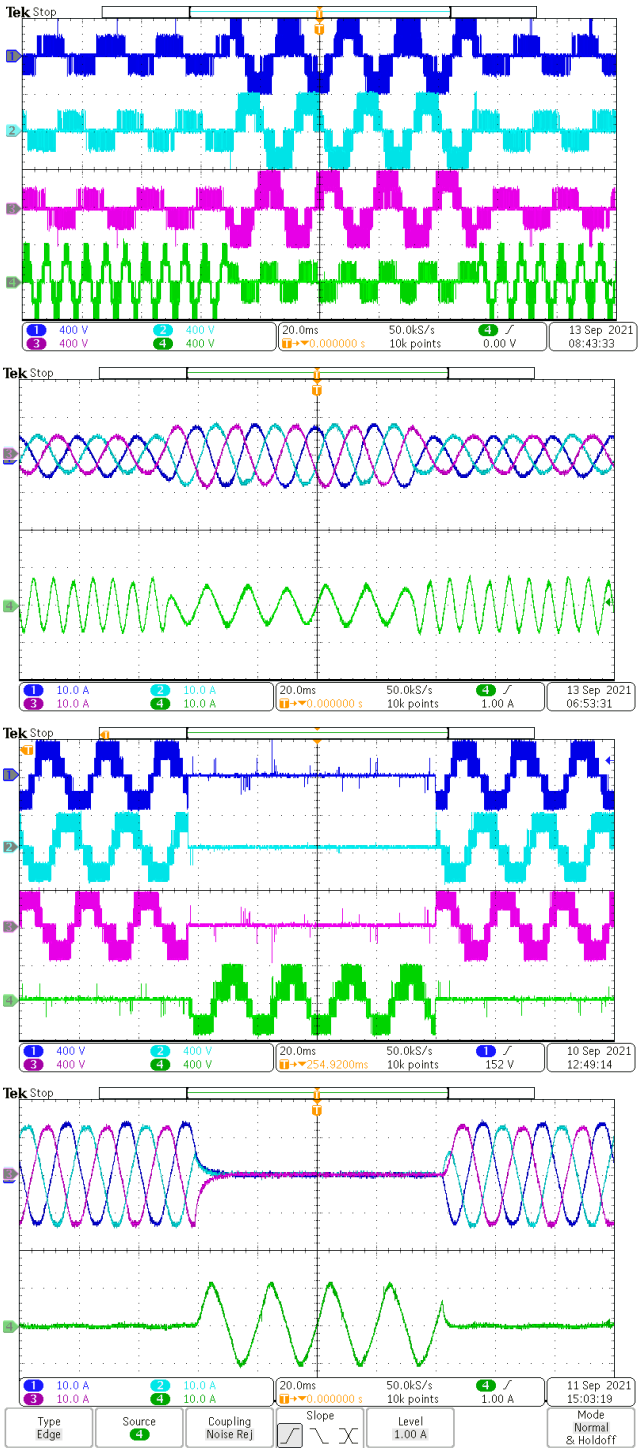

Figure 10. Experimental output voltage and current waveforms of the dual-phase inverter for different frequencies and modulation indices. (**a**,**b**) Output voltage and current waveforms for frequencies and modulation indices for inverters 1 and 2 of: 50 and 150 Hz, with modulation indices of 0.35 and 0.8 (50 Hz), and 50 and 75 Hz, with modulation indices of 1.05 and 0.25; (**c**,**d**) either operation of the two inverters at a common frequency of 50 Hz and modulation indices of 1.1547 and 1.

An experimental demonstration of the possibility of isolating either of the two inverters is shown in Figure 10c,d. Therein, an output frequency of 50 Hz at point m_p was used. For the same peak-point operation ($m_1 = 1$ and $m_2 = 1.1547$), the inverter input power was experimentally measured with the power analysis application module MDO3PWR using

an MDO3034 oscilloscope. The same module was used to measure the power delivered to the one-phase load; while a Fluke 434/435 three-phase power-quality analyzer was used to measure the power delivered to the three-phase loads. The results of these power measurements are displayed in Figure 11a–c, and depict an inverter efficiency of 98.6647%. Furthermore, load variation in the dual-phase system was demonstrated with a 40 Ω resistor in series with a 20 mH inductor in each phase of the three-phase system; and a 20 Ω resistor in series with a 20 mH inductor in the single-phase system. The appropriate power measurements were taken, and these are displayed in Figure 11d–f; an inverter efficiency of 98.6856% was calculated.

Figure 11. Dual-phase-inverter measured input and output powers: (**a**) measured single-phase output power; (**b**) measured output power delivered to the three-phase loads; (**c**) measured input power.

5. Conclusions

A three-level, dual-phase inverter configuration has been presented in this paper. Detailed operational principles and a control scheme for the inverter have been given. The reduced complexity in both the power circuit's component count and the modulation approach were innate attractive features of the proposed dual-phase inverter. In expansive simulated and experimental investigations, the inverter showed smooth transitions between the specified ranges of operational modulation indices for both equal and different frequency operations. Moreover, the additional possibility of the alternate generation of one out of the two sets of one- and three-phase output voltage waveforms was offered by the proposed dual-phase inverter configuration. For the experimental measured input and output powers, an efficiency of 98.6647% was achieved in the inverter prototype's operation. The performance of the proposed dual-output inverter has been presented through simulations and scaled-down experiments using a prototype unit, and the results have been adequately presented.

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