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Reduced-Cost Optimization-Based Miniaturization of Microwave Passives by Multi-Resolution EM Simulations for Internet of Things and Space-Limited Applications

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Abstract: Stringent performance specifications along with constraints imposed on physical dimensions make the design of contemporary microwave components a truly onerous task. In recent years, the latter demand has been growing in importance with the innovative application of areas such as the Internet of Things coming into play. The need to employ full-wave electromagnetic (EM) simulations for response evaluation, reliable, yet CPU-heavy, only aggravates the issue. This paper proposes a reduced-cost miniaturization algorithm that employs a trust-region search procedure and multi-resolution EM simulations. In our approach, the resolution of the EM model is adjusted throughout the optimization process based on its convergence status starting from the lowest admissible fidelity. As the algorithm converges, the resolution is increased up to the high-fidelity one, used at the final phase to ensure reliability. Four microwave components have been utilized as verification structures: an impedance matching transformer and three branch-line couplers. Significant savings in terms of the number of EM analyses required to conclude the size reduction process of 41, 42, 38 and 50 percent have been obtained (in comparison to a single-fidelity procedure). The footprint area of the designs optimized using the proposed approach are equal to 32, 205, 410 and 132 mm^2, in comparison to 52, 275, 525 and 213 mm^2 of the initial (and already compact) design.

Keywords: microwave design; compact microwave components; simulation-driven design; EM-based miniaturization; Internet of Things; multi-resolution simulations

Citation: Pietrenko-Dabrowska, A.; Koziel, S.; Raef, A.G. Reduced-Cost Optimization-Based Miniaturization of Microwave Passives by Multi-Resolution EM Simulations for Internet of Things and Space-Limited Applications. *Electronics* **2022**, *11*, 4094. https://doi.org/10.3390/electronics11244094

Academic Editor: Sohail Mumtaz

Received: 4 November 2022
Accepted: 7 December 2022
Published: 8 December 2022

1. Introduction

Nowadays, the design of microwave components has become an intricate process that has to satisfy stringent performance requirements, but must also enable the implementation of additional functionalities. Performance specifications pertinent to electrical characteristics of the circuit are typically related to operating frequency and/or frequencies (in the case of multi-band structures), bandwidth, power split ratio, insertion loss levels, allocation of transmission zeros, etc. [1–3]. Additional functionalities may include multi-band operation [4,5], tunability [6] or harmonic suppression [7]. Meeting these requirements can be even more challenging due to growing demands for compact size [8,9], which is imperative for emerging applications (e.g., 5G communications [10], Internet of Things (IoT) [11], energy harvesting [12] or sensors [13]). Various methods for miniaturization of microwave components have evolved, including topological modifications, such as transmission line folding [14], employment of compact microstrip resonant cells using the slow-wave phenomenon [15], defected ground structures [16] and high-permittivity substrates [17]. Consequently, compact microwave structures usually feature intricate geometries characterized by large numbers of geometry parameters, simultaneous adjustment of which is indispensable to ascertain the component's best achievable performance.

This, in turn, is of paramount importance, especially for cutting-edge technologies (5G/6G, Internet of Things).

In practice, the tuning process must be executed with the use of full-wave electromagnetic (EM) simulation tools. The employment of EM analysis for the design of compact components is necessary to represent EM cross-coupling effects in tightly packed layouts of miniaturized circuits [18], the effects of environmental components (e.g., connectors) [19], or simply because equivalent network models are grossly inaccurate in characterizing topologically involved structures. On the other hand, rigorous numerical optimization using EM simulations tends to be CPU-heavy. Nevertheless, it is the only approach allowing for the efficient handling of a number of performance figures (e.g., return loss, bandwidth or operating frequency/frequencies), and, at the same time, ensuring control over the physical size of the circuit under study. As the design objectives typically stay in conflict, in practice, the obtained designs constitute trade-offs between the considered performance figures. From a numerical perspective, miniaturization tasks are constrained problems with the constraints being expensive to evaluate. Handling such optimization tasks is numerically demanding, as designs featuring minimum size normally reside at the feasible region boundary. The aforementioned factors make simulation-based miniaturization of microwave components challenging.

The high cost of EM-driven optimization of microwave components, including size-reduction-oriented tasks, is troublesome both in the case of local [20–22] and global search [23], especially when using population-based metaheuristics [24–26]. Among the techniques designed for streamlining local gradient-based search algorithms, adjoint sensitivities [27,28] and sparse sensitivity updates [29–31] may be listed. A completely different strategy is fostered by surrogate-assisted schemes. The surrogate (or a metamodel) is a faster, yet accurate representation of the component under design. There are two kinds of surrogates: physics-based [32] and data-driven [33]. The former involves a low-fidelity representation of the system, e.g., an equivalent circuit. The low-fidelity model is corrected to improve its misalignment with the high-fidelity (EM) model. Representative techniques of this class are space mapping [34], feature-based optimization [35,36] or adaptive response scaling [37]. The second group of surrogates is more generic, as their construction does not require any problem-specific knowledge. The popularity of data-driven models comes from an easy access and versatility (mainly via third-party Matlab toolboxes of many kinds, e.g., SUMO [38], DACE [39], UQlab [40]). Multiple modelling techniques are available, including kriging [41], radial basis functions (RBF) [42], Gaussian process regression [43], support vector regression [44] or neural networks [45–48]. Still, their applicability is limited by the curse of dimensionality. Setting up reliable surrogates for contemporary microwave devices of intricate topologies and featuring a large number of variables is hardly possible, particularly if the model has to cover broad ranges of operating and geometry parameters (which is imperative from the standpoint of design usability of the model).

This paper proposes an efficient and reliable algorithm for simulation-driven miniaturization of compact microwave components. Our methodology employs multi-fidelity EM simulations selected over a specified range of allowable resolutions: from the minimal (still ensuring satisfactory accuracy) to the high-fidelity model [49]. In addition, the formulation of the design task permits an efficient treatment of design constraints while directly handling size reduction of the structure under design. The entire procedure is embedded into a trust-region gradient-based framework. During the optimization process, the model discretization level is set contingent upon the algorithm convergence status. Adopting the aforementioned mechanisms permits sizeable computational savings without degrading the process reliability. The proposed technique has been employed to miniaturize four compact microwave components: a three-section impedance matching transformer, as well as three branch-line couplers, and is compared to single-fidelity trust-region gradient-based algorithm. The computational cost has been reduced by nearly 50 percent.

The proposed approach enables a rapid rendition of minimum-size microwave components. By means of simultaneous adjustment of all geometry parameters, it allows for

additional miniaturization beyond what is possible by pure topology selection of the circuit. Short running time and generality of the presented algorithm make it useful for yielding top-quality structures and to reduce circuit development time, both being of paramount importance for academic research and even more for industry, particularly, in the context of rapidly growing areas including, e.g., the Internet of Things.

The novelty and the technical contributions of the work under review include: (i) development of an algorithm for direct optimization-based miniaturization of microwave components with multi-fidelity EM simulations, (ii) implementation of the size reduction algorithm integrating local gradient-based search with automated adjustment of the model discretization level and (iii) demonstrating a significant speedup of the search process with only a minor increase in the device footprint area with respect to the reference procedure.

2. Miniaturization of Microwave Passives by Multi-Fidelity Simulations

This section describes the proposed miniaturization procedure with multi-resolution EM simulations. The section begins with a formulation of optimization-based miniaturization of microwave passives (Section 2.1). Section 2.2 recalls the standard trust-region algorithm employed in this work as a search engine. The delineation of the multi-fidelity model adjustment scheme and the entire miniaturization framework in Sections 2.3 and 2.4, respectively, concludes this part of the manuscript.

2.1. Problem Formulation

Nowadays, the design of compact microwave components is more often than not performed through rigorous numerical optimization. Circuit miniaturization is no exception here. In this work, the size reduction task is tackled by solving

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} U(\boldsymbol{x}), \tag{1}$$

which may also be subject to the inequality constraints $g_k(\boldsymbol{x}) \leq 0$, $k = 1, \ldots, n_g$, as well as equality constraints $h_k(\boldsymbol{x}) = 0$, $k = 1, \ldots, n_h$. In (1), U is the scalar objective function quantifying the design quality, and $\boldsymbol{x}$ denotes the vector of design variables. For size reduction, $U(\boldsymbol{x}) = A(\boldsymbol{x})$, with A being the circuit size. Here, we adopt a penalty approach [50], in which the constraints are dealt with in an implicit manner. Thus, the reformulated objective function U_P is employed, which accounts for the primary objective (here, the component's footprint) and other requirements. We have

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} U_P(\boldsymbol{x}), \tag{2}$$

where the function U_P is defined as follows

$$U_P(\boldsymbol{x}) = U(\boldsymbol{x}) + \sum_{k=1}^{n_g+n_h} \beta_k c_k(\boldsymbol{x}) \tag{3}$$

with $c_k(\boldsymbol{x})$, $k = 1, \ldots, n_g + n_h$, representing the penalty functions that quantify constraint violations, whereas β_k denotes the penalty coefficients. In (3), the primary objective (size reduction) is supplemented by the contributions proportional to suitably quantified constraint violations. The coefficients β_k are typically set up based on designer's experience on a case-to-case basis.

2.2. Search Engine: Trust-Region Local Search

This section recalls the standard trust-region (TR) algorithm [51], which is exploited here as a search engine. The TR algorithm iteratively yields a series of approximations $\boldsymbol{x}^{(i)}$,

$i = 0, 1, \ldots,$ to $\boldsymbol{x}^*$ (i.e., the optimal solution), where $\boldsymbol{x}^{(0)}$ denotes the initial design. Each consecutive vector $\boldsymbol{x}^{(i)}$ is established by solving

$$\boldsymbol{x}^{(i+1)} = \arg \min_{\boldsymbol{x};\ -\mathbf{d}^{(i)} \le \boldsymbol{x} - \boldsymbol{x}^{(i)} \le \mathbf{d}^{(i)}} U_L^{(i)}(\boldsymbol{x}), \tag{4}$$

where $U_L{}^{(i)}$ is defined as U_P, but with linear model $L^{(i)}$ of the circuit response $\boldsymbol{R}(\boldsymbol{x})$. Our principal objective is to reduce the circuit size $A(\boldsymbol{x})$, which can be evaluated analytically based on the parameter vector $\boldsymbol{x}$. Thus, there is no need to use the linear model to assess it. Still, when calculating the constraints, the linear expansion model $L^{(i)} = \boldsymbol{R}(\boldsymbol{x}^{(i)}) + \boldsymbol{J_R}(\boldsymbol{x}^{(i)})\cdot(\boldsymbol{x} - \boldsymbol{x}^{(i)})$ needs to be employed.

2.3. Model Fidelity Arrangement

Our algorithm exploits multi-fidelity model simulations to expedite miniaturization of microwave passives. Although variable-fidelity frameworks have been employed in antenna [52] and microwave design [53], they typically utilize two levels of resolution: low- and high-fidelity models. Here, we follow the concept introduced in [49], where a continuous range of resolution levels is exploited, delimited by two boundary levels: the lowest one that is still practically useful and the one corresponding to the high-fidelity model. The actual selection of the two levels is of paramount importance. The lowest resolution $r_{\min}$ has to ensure adequate accuracy of the associated model while offering sufficient computational savings, whereas the highest resolution $r_{\max}$ needs to provide an accurate representation of the system outputs.

The model fidelity arrangement utilized in this work is based on the following suppositions: (i) the procedure is initiated with $r_{\min}$ (for the sake of computational savings); (ii) in the consecutive iterations, the resolution r is increased step-by-step, contingent upon the convergence status of the optimization procedure; and (iii) close to the termination, $r_{\max}$ is enforced (for the sake of reliability).

The following factor assessing the convergence status is defined as

$$Q^{(i)}(\varepsilon_x, \varepsilon_U) = \max\left\{ \frac{\varepsilon_x}{||\boldsymbol{x}^{(i+1)} - \boldsymbol{x}^{(i)}||}, \frac{\varepsilon_U}{|U_P(\boldsymbol{x}^{(i+1)}) - U_P(\boldsymbol{x}^{(i)})|} \right\} \tag{5}$$

with ε_x and ε_U referring to the user-defined termination thresholds. The optimization procedure has reached convergence if the following holds: $||\boldsymbol{x}^{(i+1)} - \boldsymbol{x}^{(i)}|| < \varepsilon_x$ (the design shift between iterations is small) OR $||\boldsymbol{d}^{(i)}|| < \varepsilon_x$ (the TR size is sufficiently reduced) OR $|U_P(\boldsymbol{x}^{(i+1)}) - U_P(\boldsymbol{x}^{(i)})| < \varepsilon_U$ (the change of the merit function value between iterations is minor). The factor $Q^{(i)}$ serves for adjusting the value of the model discretization level $r^{(i+1)}$ for the next algorithm iteration according to

$$r^{(i+1)} = \begin{cases} r_{\min} \ \text{ if } \ Q^{(i)}(\varepsilon_x, \varepsilon_U) \le M \\ \max\left\{ r^{(i)}, r_{\min} + (r_{\max} - r_{\min}) \left[Q^{(i)}(\varepsilon_x, \varepsilon_U) - M \right]^{\frac{1}{\alpha}} \right\} \end{cases} \tag{6}$$

In (6), M governs the onset of the model resolution increase (with respect to the algorithm convergence) and α is a shape parameter. By setting $M = 10^{-2}$ and $\alpha = 3$ (as in Section 3), the model resolution starts to increase (relatively rapidly) two decades prior to convergence, which is beneficiary for computational efficiency.

Nevertheless, Formula (6) does not guarantee that the final iterations are performed using the highest model resolution (which is mandatory from the standpoint of reliability). Thus, a safeguard mechanism must be implemented, which works as follows: in the final iteration, if $r^{(i)} < r_{\max}$, then the termination condition is ignored. Consequently, for the next (supplemental) iteration, the model resolution is set to $r^{(i+1)} = r_{\max}$ and the TR size is set as $\boldsymbol{d}^{(i+1)} = M_d\, \boldsymbol{d}^{(i)}\, \varepsilon_x / ||\boldsymbol{d}^{(i)}||$, where the multiplier M_d determines the increase in the TR size

to ensure sufficient space for design tuning after shifting to the maximum resolution. Here, we adopt $M_d = 10$.

To achieve additional speedup, response gradients are evaluated at a resolution $r_{FD} = \max\{r_{\min}, \lambda r^{(i)}\}$, which is lower than the current resolution used for simulation of the model outputs. The factor λ assumes positive values below 1; in our work, we set $\lambda = 2/3$.

Given a typical time evaluation ratio between the highest- and lowest-fidelity model to be about three, one can estimate the expected reduction of the computational cost of the optimization process at a level of about fifty percent. This is because most of the operations will be performed using lower-fidelity EM simulations, yet the last few iterations executed using the high-fidelity model will contribute to perhaps half of the total cost. That half, as being spanned over 1/5 to 1/4 of the overall iteration span, allows us to estimate the total cost as being half of that corresponding to the high-fidelity only version of the algorithm. This is, clearly, a very rough estimate, which highly depends on several factors, including the said time evaluation ratio.

2.4. Miniaturization Framework

The operational flow of the optimization-based multi-fidelity miniaturization algorithm discussed here is presented in Figure 1, whereas its pseudocode is presented in Algorithm 1. The algorithm exploits two main components: the trust region algorithm of Section 2.2 and the multi-fidelity model arrangement formulated in Section 2.3. The algorithm control parameters are gathered in Table 1.

Algorithm 1: Operation of the proposed multi-fidelity size reduction algorithm.

1. Set the iteration counter $i = 0$, and $r^{(i)} = r_{\min}$;
2. Evaluate component response $\boldsymbol{R}(\boldsymbol{x}^{(i)})$ at the discretization level $r^{(i)}$;
3. Evaluate component sensitivities $\boldsymbol{J}_R(\boldsymbol{x}^{(i)})$ at the discretization level r_{FD};
4. Construct a linear model $\boldsymbol{L}^{(i)}(\boldsymbol{x}) = \boldsymbol{R}(\boldsymbol{x}^{(i)}) + \boldsymbol{J}_R(\boldsymbol{x}^{(i)}) \cdot (\boldsymbol{x} - \boldsymbol{x}^{(i)})$;
5. Obtain the design $\boldsymbol{x}^{(i+1)}$ by solving (4);
6. Evaluate component response $\boldsymbol{R}(\boldsymbol{x}^{(i+1)})$ at the discretization level $r^{(i)}$;
7. Update trust-region size vector $\boldsymbol{d}^{(i)}$;
8. **If** $U_P(\boldsymbol{x}^{(i+1)}) < U_P(\boldsymbol{x}^{(i)})$,
   compute $r^{(i+1)}$ using (6);
   Set $i = i + 1$;
end
9. **If** $||\boldsymbol{x}^{(i+1)} - \boldsymbol{x}^{(i)}|| < \varepsilon_x$ OR $||\boldsymbol{d}^{(i)}|| < \varepsilon_x$ OR $|U_P(\boldsymbol{x}^{(i+1)}) - U_P(\boldsymbol{x}^{(i)})| < \varepsilon_U$
if $r^{(i)} < r_{\max}$
   Set $r^{(i)} = r_{\max}$ and modify $\boldsymbol{d}(i)$; go to 3;
else
   Go to 10;
end
else
   Go to 3;
end
10. END.

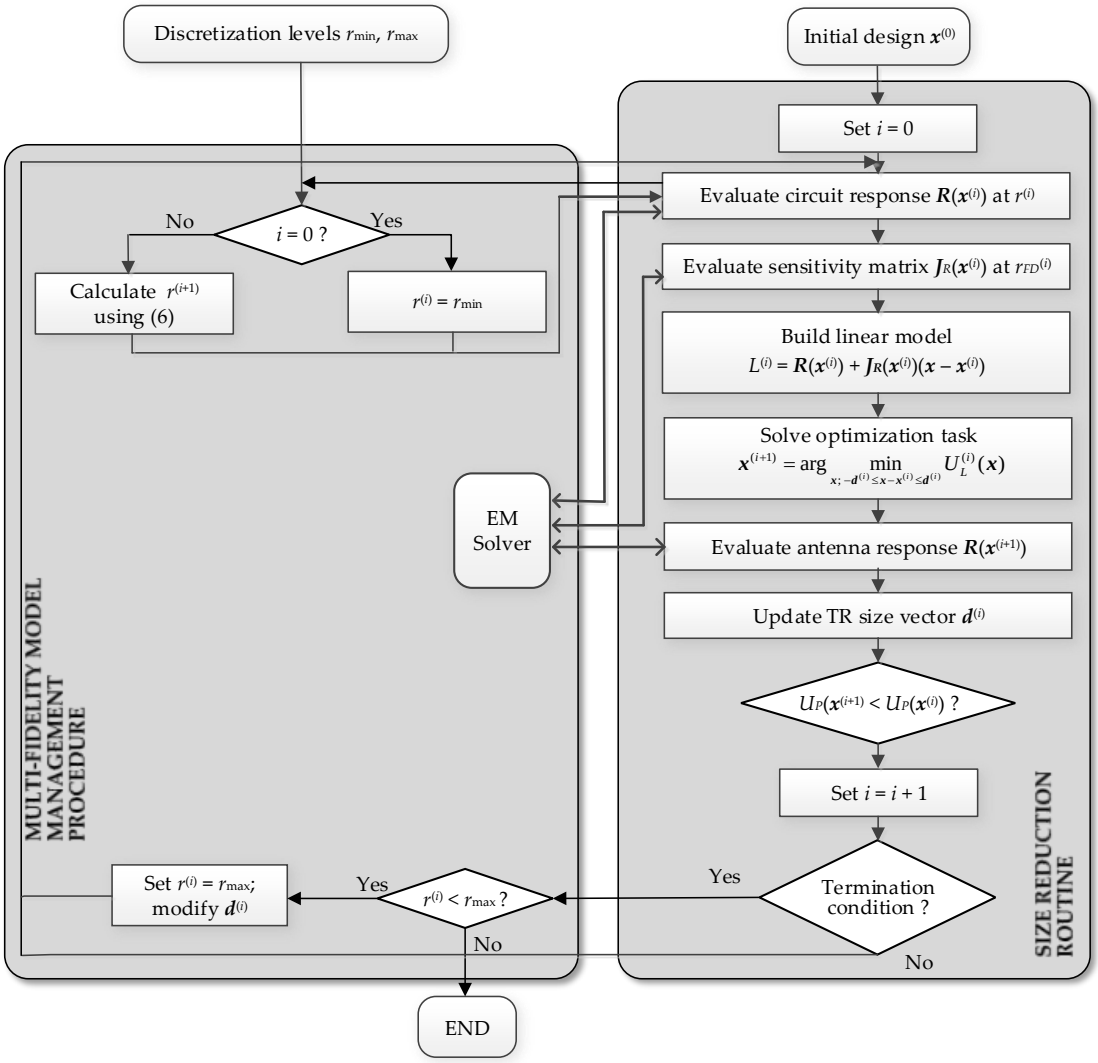


Figure 1. Operational flow of the proposed optimization-based miniaturization framework with multi-resolution EM simulations (one-headed arrows indicate the procedure flow, whereas two-headed arrows show where the procedure accesses the EM solver).

Table 1. Control parameters of the proposed algorithm.

Parameter	Purpose	Default Value
r_{min}	Governing EM-model discretization level (minimum value)	Problem specific [1]
r_{max}	Governing EM-model discretization level (maximum value)	Problem specific [1]
M	Launching the discretization level increase	10^{-2}
α	Adjustment of EM-simulation model resolution	3
λ	Setting discretization level for FD	2/3
M_d	TR radius increase (near convergence)	10
ε_x, ε_U	Algorithm termination	10^{-3}

[1] Established through a visual inspection of the family of circuit responses.

We employed CST Microwave Studio for evaluation of the computational models of the considered devices. Hence, the model discretization is parametrized by LPW (lines per wavelength), utilized in CST to govern the mesh density. The boundary resolution levels r_{min} and r_{max} were decided upon through the grid convergence studies, as presented in Section 3. The maximum resolution level r_{max} is the resolution increasing above,

which leads to no meaningful changes of the component characteristics, whereas r_{min} is assessed as the lowest resolution for which the evaluated responses outputs are still adequately rendered.

3. Results

This section provides the results obtained using the introduced size-reduction algorithm with multi-resolution EM-simulations for four microwave passive devices: a three-section impedance transformer and three branch-line couplers. The design goals for the transformer are footprint minimization and in-band matching enhancement. For the couplers, we have three design objectives: (i) footprint minimization, (ii) minimization of matching and isolation and (iii) enforcement of an assumed power split (equal in the case of two couplers, and unequal for the third one).

Figure 2 shows the geometries of four microwave devices utilized here as verification case studies: a three-section impedance transformer comprising three compact microstrip resonant cell (CMRC) sections (Circuit I), a compact branch-line coupler (Circuit II), a branch-line coupler with microstrip cells (Circuit III) and a branch-line coupler with unequal power division (Circuit IV). Table 2 gathers all the necessary information pertaining to all circuits: the geometry parameters (the relative and unit-less parameters are indicated by the subscript *r*; the remaining ones are absolute and expressed in mm), the substrate they are implemented on, the design goals, the objective function formulation and variable-fidelity simulations setup.

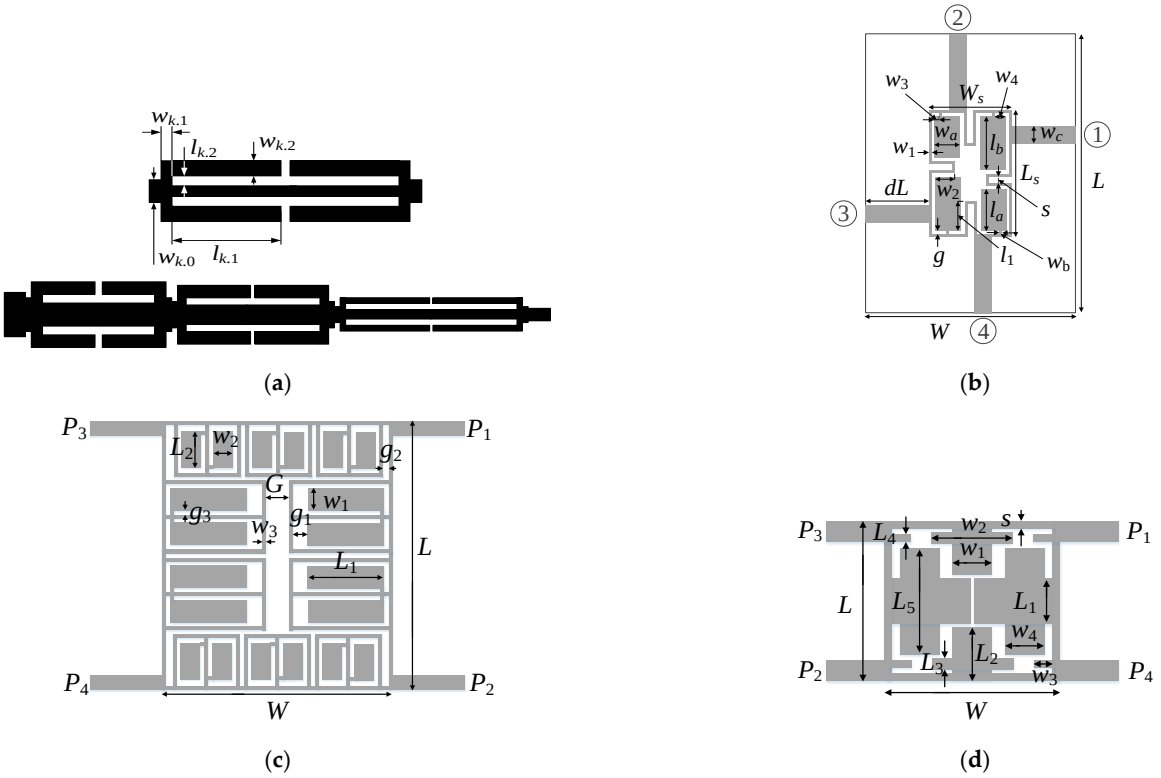


Figure 2. Verification structures: (**a**) three-section impedance matching transformer: (top) compact microstrip resonant cell (CMRC), (bottom) geometry of the circuit using CMRCs (Circuit I) [54]; (**b**) compact branch-line coupler (Circuit II) [55]; the numbers in circles show ports; (**c**) branch-line coupler with microstrip cells (Circuit III) [56], (**d**) compact branch-line coupler with unequal power division (Circuit IV) [57].

Table 2. Details of microwave structures used as verification cases.

	Case Study			
	Circuit I	**Circuit II**	**Circuit III**	**Circuit IV**
Substrate	RF-35 substrate (ε_r = 3.5, h = 0.762 mm)	RO4003 (ε_r = 3.38, h = 0.76 mm)	FR4 (ε_r = 4.4, h = 1.0 mm)	FR4 (ε_r = 4.4, h = 1.0 mm)
Design parameters	$\boldsymbol{x}$ = [$l_{1.1}$ $l_{1.2}$ $w_{1.1}$ $w_{1.2}$ $w_{1.0}$ $l_{2.1}$ $l_{2.2}$ $w_{2.1}$ $w_{2.2}$ $w_{2.0}$ $l_{3.1}$ $l_{3.2}$ $w_{3.1}$ $w_{3.2}$ $w_{3.0}$]^T	$\boldsymbol{x}$ = [g l_{1r} l_a l_b w_1 w_{2r} w_{3r} w_{4r} w_a w_b]^T	$\boldsymbol{x}$ = [G g_1 g_2 g_3 w_1 w_3 L_1 L_2]^T	$\boldsymbol{x}$ = [W w_{1r} w_{2r} w_3 w_4 L L_{1r} L_{2r} L_3 L_4 L_{5r} s]^T
Other parameters	–	$L = 2dL + L_s$, $L_s = 4w_1 + 4g$ + s + l_a + l_b, $W = 2dL + W_s$, $l_1 = l_{b1}$1r, $W_s = 4w_1 + 4g + s + 2w_a$, $w_2 = w_a w_{2r}$, $w_3 = w_{3r} w_a$, $w_4 = w_{4r} w_a$, w_c = 1.9 mm	$L = 4w_1 + 10w_3 +$ $+ 15g_3 + 2L_2$, $W = 4w_3 + 2L_1 +$ $+ G + 2g_1 + 2g_3$	$w_1 = w_{1r}w_2$, $w_2 = w_{2r}(W\text{-}2w_3)$, $l_1 = L_{1r}(L\text{–}2s\text{–}2l_4)$, $l_2 = L_{2r}(L\text{–}l_1)/2$, L_5=$L_{5r}(L\text{–}2(W_0\text{–}l_4/2)\text{–}mx)$, mx=$\lvert l_4 - l_3 \rvert /2$+$(l_4$+$l_3)/2$
Operating parameters	F = [1.75 4.25] GHz	f_0 = 1.5 GHz	f_0 = 1.0 GHz	f_0 = 2.0 GHz
	Design goals			
F_1	Minimization of footprint area			
F_2	Minimization of matching $\lvert S_{11} \rvert$ within bandwidth F	Minimization of matching $\lvert S_{11} \rvert$ and isolation $\lvert S_{41} \rvert$ at f_0		
F_3	–	Equal power split at f_0: $\lvert S_{31} \rvert - \lvert S_{21} \rvert$ = 0 at f_0		Unequal power split at f_0: $\lvert S_{31} \rvert - \lvert S_{21} \rvert$ = 3 dB at f_0
Objective function (cf. (3))	$U_P(\boldsymbol{x}) = A + \beta\left(\frac{\lvert S_{11} \rvert + 20}{20}\right)^2$, β = 300	$U_P(\boldsymbol{x}) = A + \beta_1\left(\frac{\lvert S_{11} \rvert + 20}{20}\right)^2 + \beta_2\left(\frac{d_s - d_{s\max}}{d_{s\max}}\right)^2$, β_1 = 10,000, β_2 = 30, $d_{s\max}$ = 0.1	β_1 = 1000, β_2 = 30, $d_{s\max}$ = 0.1	β_1 = 10,000, β_2 = 100, $d_{s\max}$ = 3.0
	Low-fidelity model			
$r_{\min}$	14	16	15	16
Simulation time [s] #	80.3	130.0	215.6	188.5
	High-fidelity model			
$r_{\max}$	28	30	28	26
Simulation time [s] #	160.4	237.4	960.3	283.6
Time evaluation ratio	2.0	1.8	4.5	1.5
Initial design	$\boldsymbol{x}^{(0)}$ = [3.58 0.19 0.79 0.38 0.3 3.75 0.24 0.33 0.39 1.46 3.9 0.18 0.23 0.28 1.0]^T	$\boldsymbol{x}^{(0)}$ = [0.59 0.7 6.7 8.3 0.84 0.91 0.72 0.13 3.3 0.63]^T	$\boldsymbol{x}^{(0)}$ = [1.0 1.0 0.6 0.25 2.4 0.25 9.0 3.75]^T	$\boldsymbol{x}^{(0)}$ = [15.0 0.63 0.93 3.45 3.0 12.4 0.42 0.81 1.50 1.0 0.9 0.5]^T

EM-simulations were performed on an Intel Xeon 2.1 GHz dual-core CPU with 128 GB RAM.

Table 2 also provides the values of the penalty coefficients (cf. (3)), which determine the contribution of the penalty terms to make them commensurable to that of the main objective (here, footprint miniaturization). The said values have been set up for each verification case individually. The computational models are evaluated using the time-domain solver of CST Microwave Studio and I dependence of the simulation time on the parameter LPW is presented in Figure 3. The proposed framework utilizes the default control parameter values provided in Table 1.

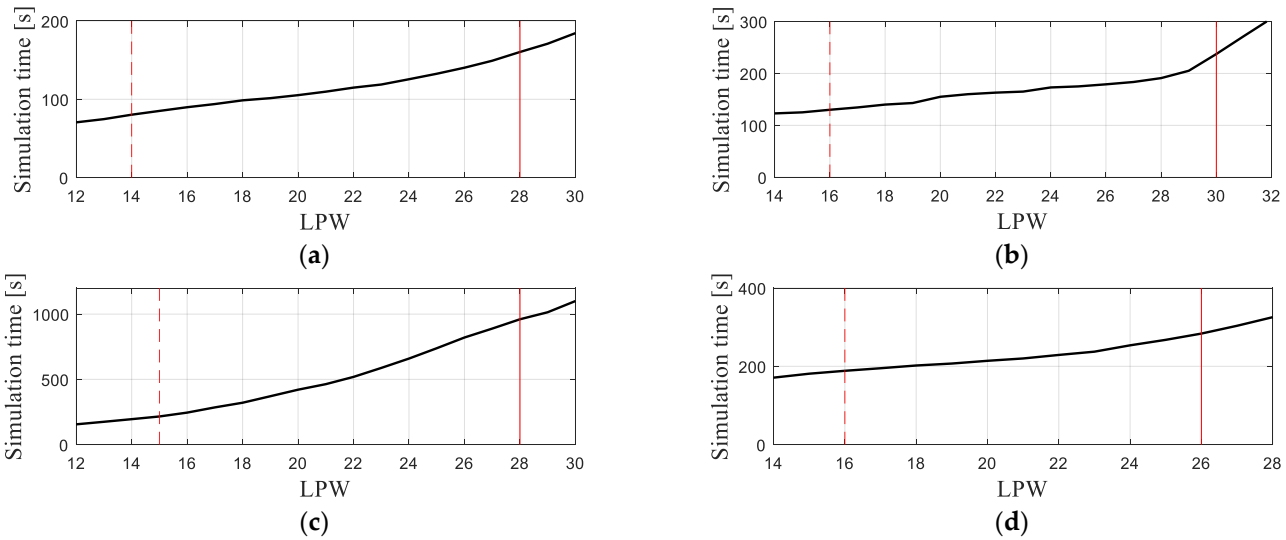


Figure 3. The dependence on the simulation time versus model resolution expressed using LPW: (**a**–**d**) Circuit I through IV, respectively; the low-fidelity model (- - -) and the high-fidelity model (—) are shown using vertical lines.

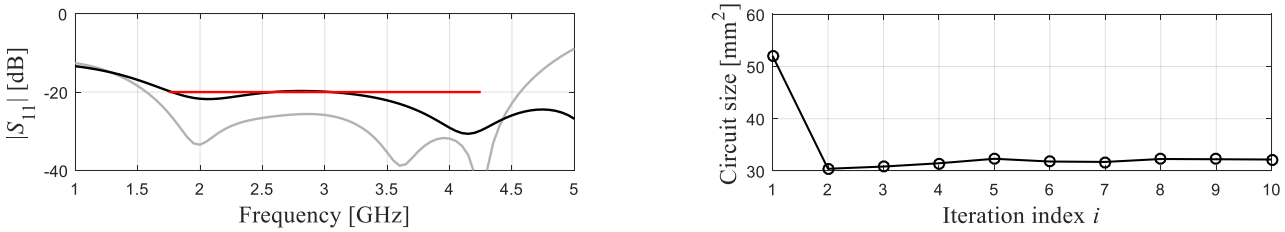
Our procedure is benchmarked against the conventional single-fidelity trust-region procedure with numerical derivatives to verify the acceleration rate achieved due to the involvement of variable-resolution models, as well as to investigate possible design quality degradation. The following performance factors are taken into account: the footprint of the circuit at the optimal design, along with the computational cost of rendering it. As far as multi-fidelity algorithm is concerned, the actual model simulation times for each resolution level are assessed as the equivalent number of simulations of the highest resolution $r_{\max}$.

Table 3 gathers the optimization results obtained for all circuits using the introduced algorithm and the conventional TR algorithm utilized here as a reference routine. The results comprise the expenditures of the optimization procedure expressed as the equivalent number of high-fidelity circuit analyses (evaluated using the time evaluation curves of Figure 3), along with the savings with regard to the TR search. Moreover, Table 3 provides the footprint of all the verification structures. Figures 4–7 present the responses of the respective circuits at the initial and optimized designs, as well the evolution of circuit size throughout the algorithm runs.

Table 3. Numerical results.

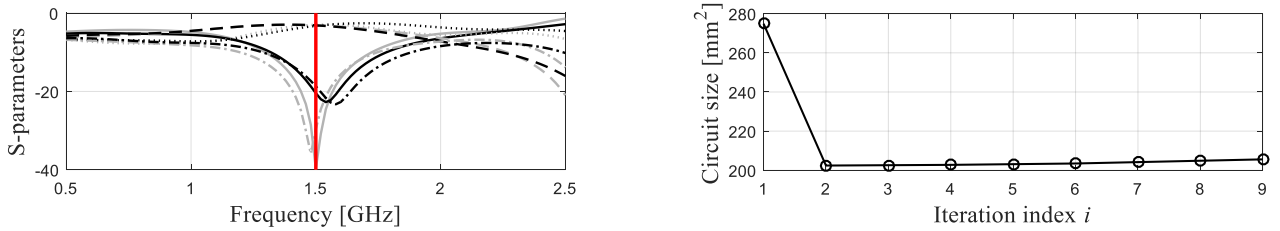
Circuit	Algorithm	Cost [1]	Cost Savings [2]	Footprint Area A [mm^2] [3]
I	Conventional TR search	158	–	30.0
	Multi-fidelity (this work)	93	41.1	32.2
II	Conventional TR search	67	–	182.0
	Multi-fidelity (this work)	39	41.8	205.5
III	Conventional TR search	73	–	407.1
	Multi-fidelity (this work)	45	38.4	409.8
IV	Conventional TR search	152	–	143.1
	Multi-fidelity (this work)	87	50.3	131.9

[1] Number of equivalent high-fidelity EM simulations. [2] Relative computational savings in percent with respect to the reference algorithm. [3] Obtained footprint area.



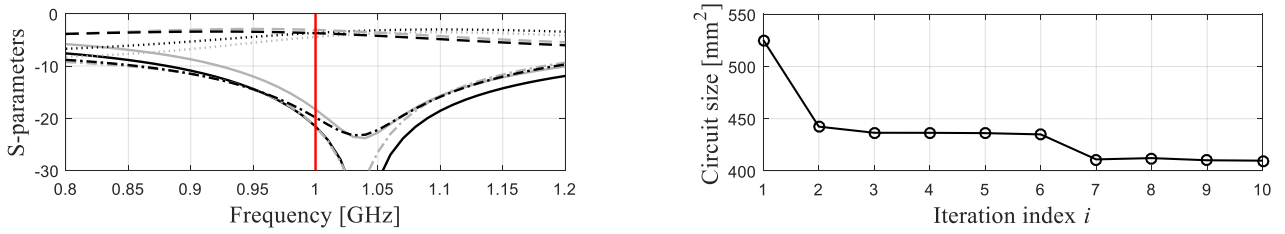
(**a**) (**b**)

Figure 4. Circuit I: (**a**) responses at the initial (A_0 = 52 mm^2) (gray) and design optimized using the proposed algorithm (reduced size: A_{opt} = 31 mm^2) (black); the red horizontal line marks the design specifications; (**b**) evolution of the circuit size throughout the optimization run.



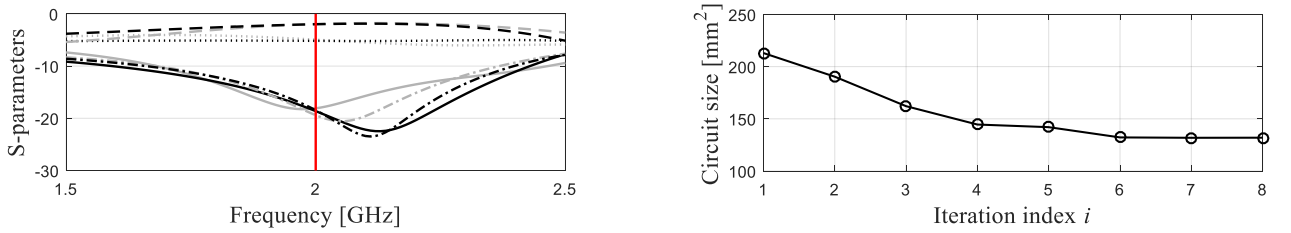
(**a**) (**b**)

Figure 5. Circuit II: (**a**) responses at the initial (A_0 = 275 mm^2) and design optimized using the proposed algorithm (reduced size: A_{opt} = 205 mm^2), indicated using gray and black, respectively; *S*-parameters marked as $|S_{11}|$ (—), $|S_{21}|$ (····), $|S_{31}|$ (- - -), $|S_{41}|$ (- .); the vertical line marks the circuit operating frequency; (**b**) evolution of the circuit size throughout the optimization run.



(**a**) (**b**)

Figure 6. Circuit III: (**a**) responses at the initial (A_0 = 525 mm^2) and design optimized using the proposed algorithm (reduced size: A_{opt} = 409 mm^2), indicated using gray and black, respectively; *S*-parameters marked as $|S_{11}|$ (—), $|S_{21}|$ (····), $|S_{31}|$ (- - -), $|S_{41}|$ (- .); the vertical line marks the circuit operating frequency; (**b**) evolution of the circuit size throughout the optimization run.



(**a**) (**b**)

Figure 7. Circuit IV: (**a**) responses at the initial (A_0 = 213 mm^2) and design optimized using the proposed algorithm (reduced size: A_{opt} = 132 mm^2), indicated using gray and black, respectively; *S*-parameters marked as $|S_{11}|$ (—), $|S_{21}|$ (····), $|S_{31}|$ (- - -), $|S_{41}|$ (- .); the vertical line marks the circuit operating frequency; (**b**) evolution of the circuit size throughout the optimization run.

Comparison of the proposed miniaturization framework based on multi-fidelity simulations with the conventional single-fidelity trust-region gradient based algorithm allows us to draw the following conclusions: our approach allows for achieving significant miniaturization rates equal to around 38, 25, 22 and 38 percent (31 percent on average) for Circuits I through IV, respectively, with respect to the initial (and already compact) structure size, whereas for the benchmark TR algorithm, we have 42, 34, 22 and 33 (33 on average). Thus, the size of the optimized designs with respect to the area of the initial design for the proposed and benchmark procedure, are comparable. In the case of Circuits I through III, the footprints of the optimal designs are only 7, 11 and 1 percent larger than those rendered by the conventional TR algorithm, whereas the area of the Circuit IV is eight percent smaller. For the sake of comparison, the footprints of the initial and optimized designs are shown in Figure 8.

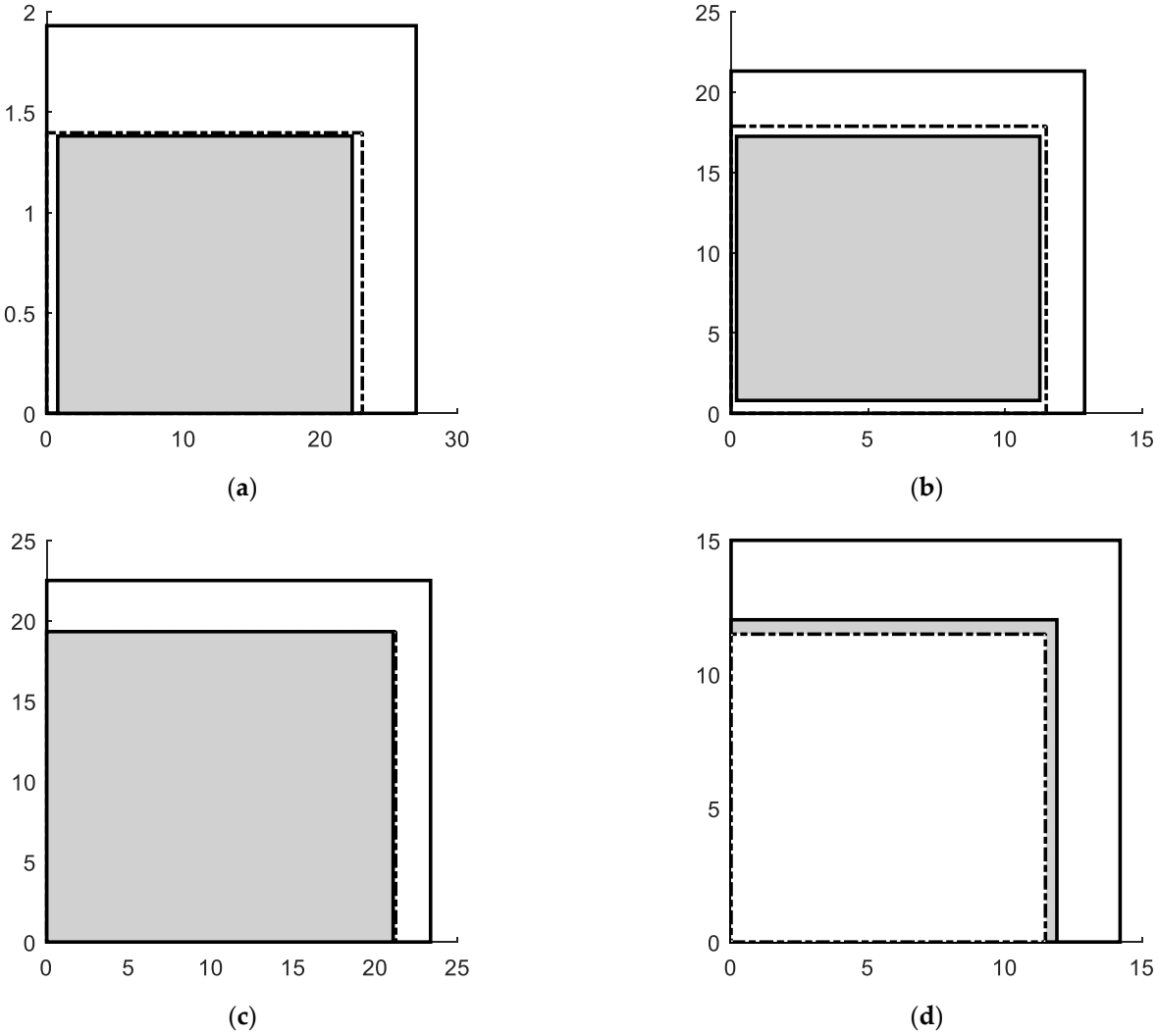


Figure 8. Footprint areas of the initial design (white rectangle, solid line), as well as the designs optimized using the proposed (white rectangle, dash-dotted line), and the basic TR routine (grey rectangle, solid line): (**a**) Circuit I, (**b**) Circuit II, (**c**) Circuit III, and (**d**) Circuit IV.

The said miniaturization rates are accompanied by a considerable computational savings of around 43 percent on the average (see Table 3). This means that incorporating multi-resolution EM simulations allows for accelerating the optimization-based miniaturization process almost twice on the average at the cost of slightly degraded miniaturization rates. Measuring in absolute numbers, the average CPU cost corresponds to around sixty

high-fidelity EM simulations, meaning that the typical execution time only takes around three hours.

4. Conclusions

The paper proposed a novel framework for optimization-based EM-driven size reduction of microwave circuits. Our approach exploits multi-fidelity EM simulations, which are embedded into the core gradient-based optimization algorithm. The management of the circuit discretization level during the optimization run is contingent upon its convergence status: from the lowest one, used when the procedure is launched, to the highest resolution utilized near reaching optimum. Consequently, a significant speedup of the miniaturization procedure been obtained in comparison to a single-fidelity version with similar miniaturization rates. The performance of the proposed size-reduction framework has been comprehensively verified using four microwave devices: an impedance transformer and three branch-line couplers, all optimized for a minimum size. Additionally, minimization of matching within the frequency band of interest has been carried out in the case of the transformer, whereas the couplers have been optimized for best matching and isolation. The savings, with respect to a single-fidelity procedure, have been equal to 41, 42, 38 and 50 percent, across the benchmark set. In the proposed approach, optimal designs feature truly compact sizes: 32, 205, 410 and 132 mm^2 (in comparison to 52, 275, 525 and 213 mm^2 of the initial design). It should be emphasized that size reduction of microwave components has become critical for a number of applications, including the Internet of Things. The proposed approach offers a design enhancement solution that is fast to execute, fully automated and complements traditional design methods (here, the initial development of compact circuit topology). These features make it an attractive tool, especially in an industrial context, but also in academic research.

Author Contributions: Conceptualization, A.P.-D. and S.K.; methodology, A.P.-D. and S.K.; software, A.P.-D. and A.G.R.; validation, A.P.-D. and S.K.; formal analysis, A.P.-D. and S.K.; investigation, A.P.-D.; resources, S.K.; data curation, A.P.-D. and A.G.R.; writing—original draft preparation, A.P.-D. and S.K.; writing—review and editing, A.P.-D. and S.K.; visualization, A.P.-D. and A.G.R.; supervision, S.K.; project administration, S.K.; funding acquisition, S.K. All authors have read and agreed to the published version of the manuscript.

Funding: The research leading to these results has received funding from the Norway Grants 2014-2021 via the National Centre for Research and Development, grant NOR/POLNOR/HAPADS/0049/2019-00. This work was also supported in part by the Icelandic Centre for Research (RANNIS) Grant 217771.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Data sharing not applicable.

Acknowledgments: The authors thank Dassault Systemes, France, for making the CST Microwave Studio available.

Conflicts of Interest: The authors declare no conflict of interest. The funders had no role in the design of the study; in the collection, analyses or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

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