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Low-Voltage LDO Regulator Based on Native MOS Transistor with Improved PSR and Fast Response

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Abstract: In this paper, a low-voltage low-dropout analog regulator (ALDO) based on a native n-channel MOS transistor is proposed. Application of the native transistor with the threshold voltage close to zero allows elimination of the charge pump in low-voltage regulators using the pass element in a common drain configuration. Such a native pass transistor configuration allows simplification of regulator design and improved performance, with supply voltages below 1 V, compared to commonly used regulators with p-channel MOS transistors. In the presented design of ALDO regulator in 180 nm CMOS X-FAB technology, an output voltage of 0.7 V was achieved with an output current of 10 mA and a supply voltage of 0.8 V. Simulation results show that despite the low supply voltage, output voltage spikes do not exceed 70 mV at the worst technology corner when output current transients from 100 µA to 10 mA. Under such conditions, stable operation and power supply rejection PSR = 35 dB were achieved with an output capacitance of 0–500 pF. The proposed regulator allows to push the limit of ALDO regulator applications to voltages below 1 V with only slight degradation of its performance.

Keywords: CMOS; low voltage; low power; low-dropout (LDO)

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1. Introduction

Low-Dropout (LDO) regulators integrated on a chip are an essential part of modern microelectronic systems on chip (SoC). LDO regulators are especially required for internet of things (IoT) systems, where power is harvested from the environment (photovoltaic, thermoelectric or RF energy). In these applications, the regulators provide voltage stabilization regardless of the actual amount of acquired power. These regulators are also used in battery-powered mobile SoCs and complex analog-digital SoCs requiring clean supply voltages of different levels. In all these applications, the voltage drop across the regulator and the quiescent current should be as low as possible while maintaining good output voltage regulation and noise suppression. LDO regulators are often required to be completely integrated without the need for external capacitors, and capacitorless regulators are preferred for this reason [1–5]. Designing LDO regulators for modern nanometer CMOS processes is becoming increasingly difficult due to the requirement of low supply voltage (less than 1 V) and short response time, which is required due to the high switching speed of powered circuits. In recent decades, this problem has been tried to be solved by using analog ALDO [1–6] or digital DLDO [7,8] low-dropout regulators. The designs of both types of regulators developed so far show that there is no single best solution. DLDO regulators are attractive because of their low-voltage operation, ease of automatic synthesis, and ability to be easily upgraded to modern technologies. On the other hand, the time response of DLDO regulators is relatively slow, especially in synchronous regulators. Additionally, these regulators have significant limitations in achieving good power supply rejection (PSR). For these reasons, DLDO regulators are mostly used to supply digital circuits where a certain level of supply voltage interference is tolerated. On the other hand, ALDO regulators allow greater suppression of interference and provide a better power-speed trade-off.

However, these favorable features are increasingly difficult to maintain under low-voltage supply conditions. In ALDO regulators at low supply voltages, achieving sufficiently high gain necessary for strong noise suppression and good voltage regulation becomes very difficult. Similarly, the degradation of response time is a result of difficulty in generating large amplitude current pulses that enable the fast charging of parasitic capacitances. To overcome these difficulties, ALDO regulators in which the error amplifier is supplied with boosted voltage obtained by a charge pump have been proposed [1,2,9,10]. With such a solution, improvement in the operating conditions of the regulator is achieved at the cost of reduced power conversion efficiency and increased chip area.

This paper proposes the use of a native n-channel transistor and an effective circuit detecting output voltage spikes to generate strong current pulses, significantly reducing undershoots of the output voltage. Native or zero (near-zero) threshold voltage MOS transistors are available in many modern CMOS processes, and are used in ultra-low-voltage circuits [11,12]. Most often these are n-channel transistors with a threshold voltage close to zero or even negative. This very feature makes these transistors very attractive for application to low-voltage ALDO regulators. The main disadvantage of native transistors is relatively high channel length, which for technological reasons is about 2–4 times larger than in low-threshold voltage transistors. However, despite these limitations, the use of native transistors in ALDO regulators offers new opportunities that have not yet been exploited.

2. Problems Related to Low Supply Voltage of LDO Regulators

Figure 1 shows simplified configurations of the most commonly used LDO regulators [1,2]. Figure 1a,b shows ALDO regulators, while Figure 1c shows a portion of a DLDO regulator for steady-state when the appropriate set of transistors in the array is turned on [6]. In the regulator in Figure 1b, with an n-channel pass transistor M_{PASS}, a charge pump (CP) is required to boost the voltage supplying the error amplifier (A_{err}) to provide sufficient voltage to control the gate of the n-channel transistor.

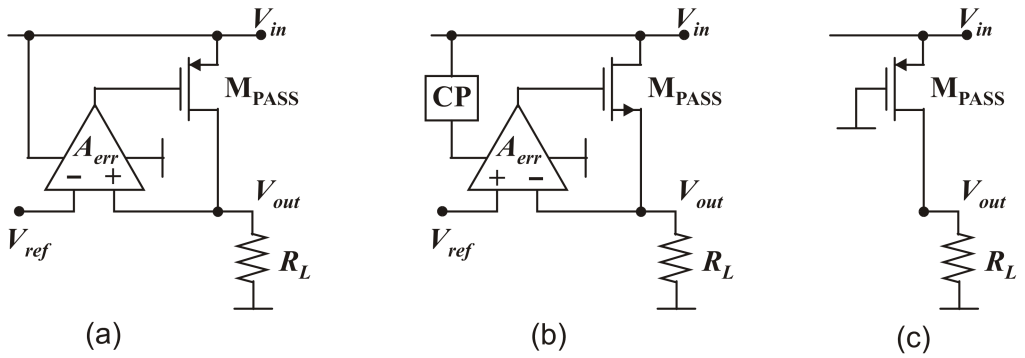


Figure 1. Simplified configurations of the most commonly used LDO regulators: (**a**) ALDO with p-MOS pass transistor, (**b**) ALDO with n-MOS pass transistor, and (**c**) portion of a DLDO.

In ALDO regulators at low frequencies, PSR can be approximated by

$$PSR = \frac{\Delta V_{in}}{\Delta V_{out}} \cong (1 + g_{ds}R_L)A_{err}(g_m/g_{ds}) = (1 + g_{ds}R_L)A_{err}A_{self} \quad (1)$$

where: R_L is a load resistance, g_{ds} and g_m are the output conductance and transconductance of the pass transistor M_{PASS}, A_{err} is the voltage gain of the error amplifier, and $A_{self} = g_m/g_{ds}$ is so called self-gain of M_{PASS}. Equation (1) was derived assuming that A_{err} and PSR of the error amplifier are high, and therefore the interference transfer from the amplifier supply voltage is negligibly small. In regulators of this type, the only way to improve PSR is by increasing the gain A_{err} of the error amplifier and increasing the self-gain A_{self} of the pass transistor M_{PASS}. With a low voltage drop across the regulator and a large output current, the pass transistor enters the deep triode region, where the self-gain becomes very small. To compensate for the decrease in the self-gain, it becomes necessary to increase

the gain of the error amplifier A_{err}, which in turn worsens the stability conditions of the control loop. In such a situation, sophisticated multi-loop methods of compensating the frequency characteristics of the error amplifier [1,13] become necessary. A side effect of such compensation is slowing down the time response of the regulator. In modern technologies, with low supply voltages, increasing voltage gain and implementing complex multi-loop compensation circuits become particularly difficult.

An even worse situation is in DLDO regulators (Figure 1c), for which the PSR at low frequencies can be expressed as:

$$PSR = \frac{\Delta V_{in}}{\Delta V_{out}} \cong \frac{(1 + g_{ds}R_L)}{(g_m + g_{ds})R_L} = \frac{(1/g_{ds} + R_L)}{(A_{self} + 1)R_L} \quad (2)$$

In this case, the PSR is relatively low, close to unity, in both regions of the pass transistor operation (triode and saturated). For this reason, hybrid analog-digital regulators [1,14], are often used to improve PSR and the time response.

From the Equation (1), it can be deduced that from the PSR improvement point of view, it is advantageous to use transistors that provide a high value of A_{self} over the entire operating range. Figure 2 shows A_{self} plots for a low-threshold voltage p-channel transistor (p-MOS) and a native n-channel transistor (n-MOS) as a function of drain current. Both transistors are a parallel connection of 60 transistors, each with W = 100 µm channel width, which is equivalent to a single transistor with a channel width of W = 6000 µm. The minimum channel lengths for each transistor type were assumed, which for the selected process (X-FAB CMOS 180 nm) are respectively L = 0.22 µm for the low-threshold voltage p-channel transistor and L = 1 µm for the native n-channel transistor. It is worth noting that for the p-channel transistor, similar results are also obtained when the channel length is L = 1 µm. These plots show that for both transistors, A_{self} is relatively high in the saturation region (I_D < 5 mA) and decreases when the transistors enter the triode region (I_D > 5 mA). The advantage of the native n-MOS transistor is clearly evident, for which A_{self} is higher, and thus the PSR that can be achieved in LDO regulator with such a transistor will be better.

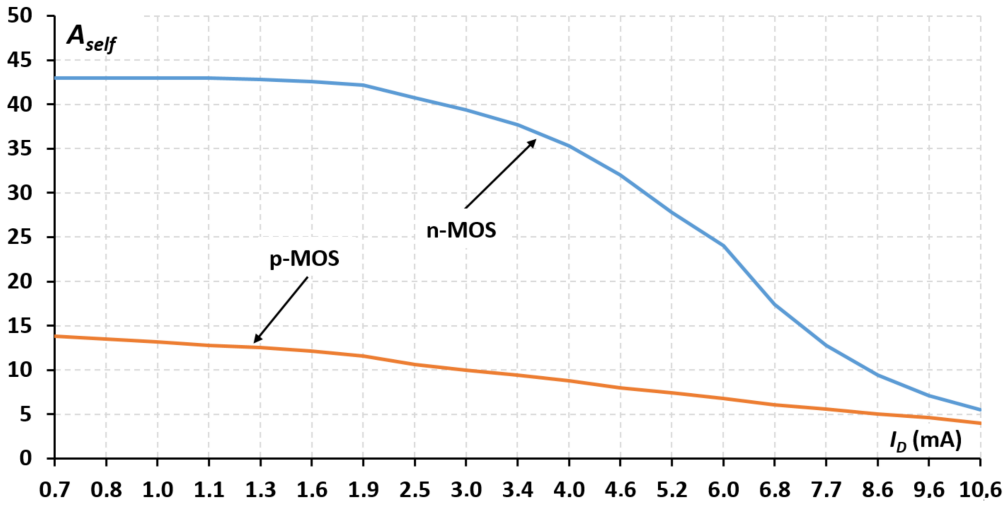


Figure 2. Plots of A_{self} for low-threshold voltage p-channel transistor (p-MOS) and a native n-channel transistor (n-MOS), V_{DS} = 0.1 V, V_{BS} = 0 for p-MOS and V_{BS} = −0.9 V for n-MOS.

At low supply voltages, it is very difficult to achieve good trade-off of stable frequency compensation and fast time response. As a result, large voltage undershoots and overshoots may appear at the regulator output when the output current changes rapidly. To better explain this problem, let us determine the equivalent impedance Z_G seen from the gate of the pass transistors M_{PASS} for the ALDO regulators shown in Figure 1a,b. The schematics of the equivalent impedances for each configuration are shown in Figure 3.

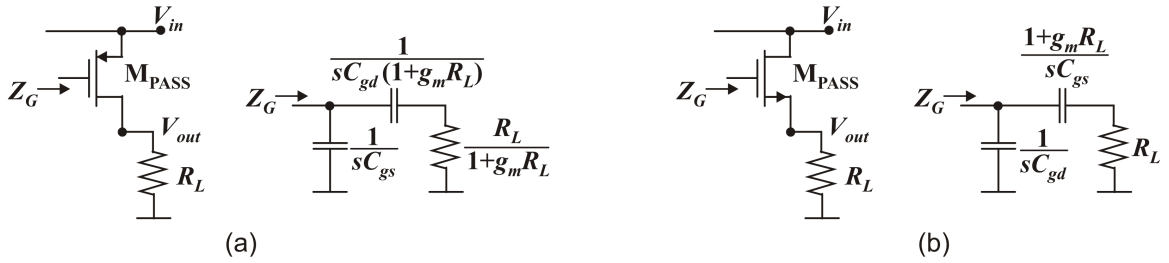


Figure 3. Schematics of the equivalent impedances Z_G seen from the gate of the pass transistors in ALDO regulators with: (**a**) p-MOS pass transistor and (**b**) n-MOS pass transistor.

The calculations took into account the internal capacitances of the transistors (C_{gs} and C_{gd}) and the load resistances R_L connected to the regulator output. From these schematics, it is seen that a regulator with the pass transistor in a common-source configuration (Figure 3a) has a much higher input capacitance resulting from the Miller effect. However, a much worse problem is the very large range of capacitance changes. The capacitance is relatively small when the transistor is in the triode region ($g_mR_L < 1$), and increases many times when the transistor reaches the saturation ($g_mR_L >> 1$). Such large variation of this capacitance makes the design of optimal frequency compensation much more difficult, and is the main cause of the response speed reduction. The situation is much more favorable in a regulator with the pass transistor M_{PASS} in a common drain configuration (Figure 3b), where the capacitance seen from the gate is much smaller, and in addition, its variation is small (maximum change is approximately two times). Unfortunately, such a configuration can only be used with low supply voltage if the voltage supplying the error amplifier is boosted by means of a charge pump [1,9,10], which in turn reduces the power conversion efficiency and increases chip area. The problem of using a pass transistor in a common drain configuration with a low supply voltage can alternatively be solved by using a native n-channel transistor. However, in order to avoid degradation of time response caused by longer channel of the native transistor, it is necessary to use effective circuits for output voltage spike suppression. Such circuits are needed to detect rapid spikes in output voltage and generate high amplitude current pulses to accelerate the response of the regulator. Figure 4 shows the spike detection circuits that are commonly used to reduce the response time of LDO regulators [15,16]. Each circuit detects a voltage spike ΔV_{out} at the output of the regulator and generates a current pulse ΔI_{D1} in response. Such a current pulse can be used to quickly charge the parasitic capacitance at the gate of the pass transistor M_{PASS} (Figure 3).

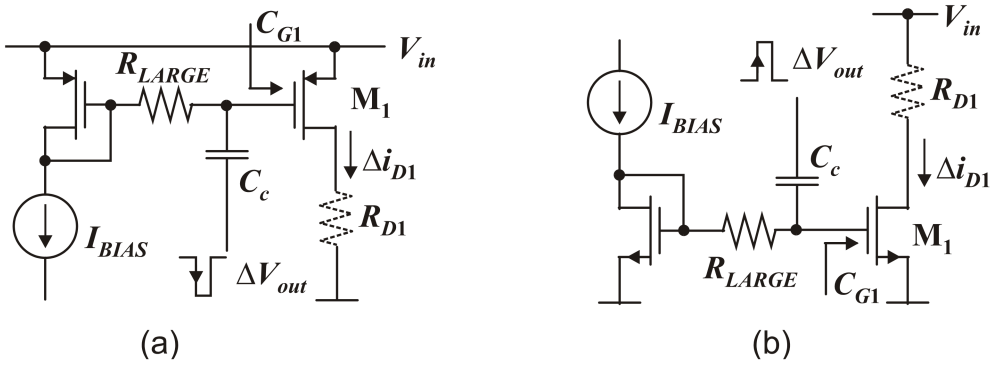


Figure 4. Most commonly used circuits for detection: (**a**) undershoots and (**b**) overshoots.

The main advantage of these circuits is their simple design, though they are inefficient in operation and implementation. The amplitude of the current pulse generated by these circuits can be approximated by

$$\Delta i_{D1} \cong \frac{g_{m1} C_c \Delta V_{out}}{C_c + C_{G1}} = \frac{g_{m1} C_c \Delta V_{out}}{C_c + C_{gs1} + C_{gd1}(1 + g_{m1} R_{D1})} \quad (3)$$

where: ΔV_{out} is the voltage spike at the output of the regulator, C_c is the capacitance coupling the spike detection circuit with the regulator output, C_{gs1}, C_{gd1} and g_{m1} are the internal capacitances and transconductance of M_1 transistor, and R_{D1} is affective resistance seen at the drain of M_1.

Based on Equation (3), it is apparent that, as in the circuit in Figure 3a, the capacitance C_{G1} seen from the gate of transistor M_1 is large due to the Miller effect. It is important to note that generation of high amplitude current pulse requires the use of M_1 with large transconductance g_{m1}, which means large channel width. Increasing the width of the channel leads to even larger capacitance C_{G1}, and thus requires a large capacitance C_c occupying a large chip area. A more effective solution to this problem is presented in the next section.

3. ALDO Regulator with a Native n-MOS Transistor and Spike Detection Circuits

The general block diagram of the proposed ALDO regulator is shown in Figure 5. The pass element is a native n-channel MOS transistor M_{PASS}, which is controlled by an error amplifier Aerr. Because of the low threshold voltage of M_{PASS}, the error amplifier Aerr can be directly supplied from the input voltage V_{in}. In this regulator, an additional loop consisting of a comparator (Cmp) and an M_{15} transistor is used to reduce output voltage undershoots. The comparator threshold voltage is shifted by V_{off} below the required output voltage $V_{out} = V_{ref}$. Therefore, when there is no V_{out} undershoot, this loop is at idle and transistor M_{15} is off. When V_{out} drop occurs, the transistor M_{15} is switched on only for a short time to reduce V_{out} undershoot.

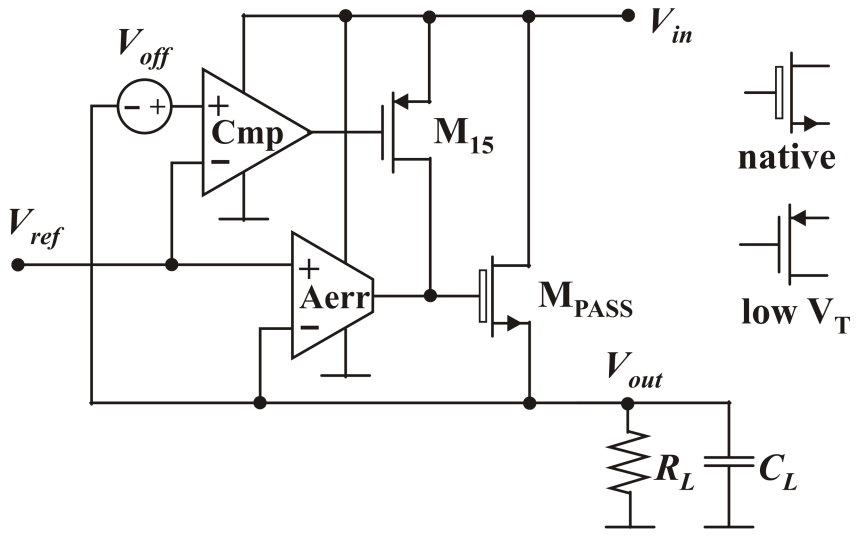


Figure 5. Block diagram of ALDO regulator with a native n-MOS pass transistor.

Figures 6 and 7 show two variants of the error amplifier (A_{err}), used for high (V_{out} > 0.85 V) and low (0.7 < V_{out} < 0.85 V) output voltages of ALDO regulator, respectively. Both amplifiers consist of two stages, the first being an input differential pair (M_1–M_3) with a cascode stage (M_4, M_5) and a dynamic load (M_6–M_9) and the second consisting of M_{10}–M_{13} transistors. In the regulator for higher output voltages, there are additional voltage shifters (M_{1A}, M_{3A}, M_{2A}, M_{3B}), which increase the voltage drop across the cascode stage, and thus improves PSR and enables a smaller voltage drop across the pass transistor (M_{PASS}).

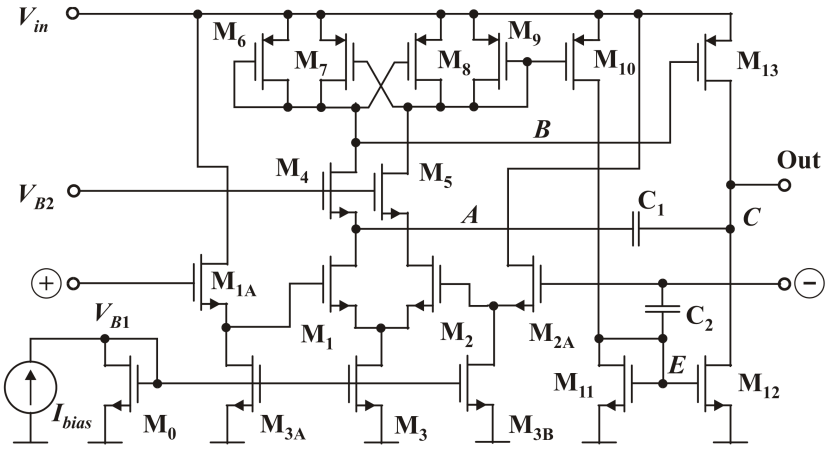


Figure 6. Schematic of the error amplifier for V_{out} > 0.85 V.

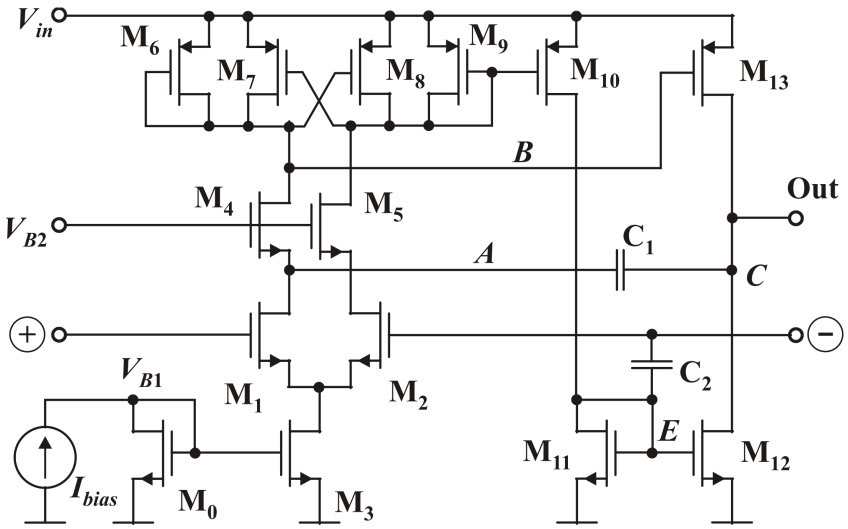


Figure 7. Schematic of the error amplifier for 0.85 V > V_{out} > 0.7 V.

In the regulator for lower voltages, the inputs of the differential pair (M_1, M_2) are directly connected to the reference voltage V_{ref} and the regulator output V_{out}. In this case, the available voltage drop across the cascode stage (M_4, M_5) is limited by the low supply voltage V_{in}. For this reason, there is a slight degradation of PSR and the required voltage drop across the pass transistor (M_{PASS}) is higher. Figure 8 shows the biasing circuit used in both regulators. This circuit generates the voltage V_{B2}, which is 0.8 V and 0.75 V for the high- and low-output voltage variants of the ALDO regulator. The bias currents of the particular amplifier stages were determined as a compromise between the minimization of the total power consumption and the speed of the transient response. The first amplifier stage consumes a current of 4 µA (4.4 µA with the voltage shifters), while the second stage consumes 10 µA. The highest current (8 µA) is consumed by a branch composed of transistors M_{13} and M_{12}, so as to achieve a sufficient rate of discharging large input capacitance of the M_{PASS} transistor. The capacitor C_2, together with transistors M_{11} and M_{12}, form a standard spike detection circuit (shown in Figure 4b), and help reduce the regulator output voltage overshoots.

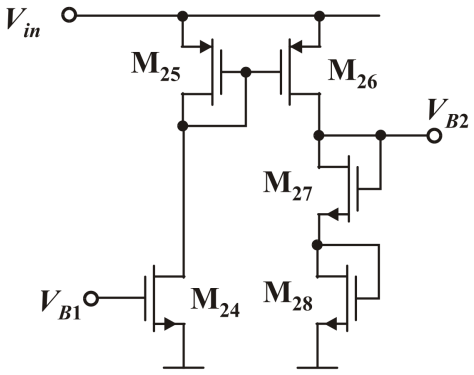


Figure 8. Schematic of the circuit generating bias voltage V_{B2}.

The compensation circuit of both error amplifiers includes capacitors C_1, C_2 and transistor M_4 acting as a current buffer. This is a simple and effective method of frequency compensation [17,18] that provides a relatively high phase margin which guarantees stable operation of the error amplifier and the complete ALDO regulator. More details about compensation and stability will be given when analyzing the negative feedback loop of the complete regulator.

Figure 9 shows a schematic of the comparator (Cmp) used in the output voltage undershoots suppression loop, depicted in Figure 5. It is a classical comparator consisting of an input differential pair (M_{19}, M_{20}) with a dynamic load (M_{21}, M_{22}) and an output inverter (M_{16}, M_{17}). The comparator was deliberately unbalanced to achieve an offset voltage V_{off} = 10 mV to protects the suppression loop from generating series of pulses that could destabilize ALDO regulator during transients. The offset voltage is achieved by increasing the channel width of the transistor M_{19} by 50% compared to M_{20}. To accelerate the switching of the comparator, the capacitor C_3 was added to increase the peak drain current of the transistor M_{21} during V_{out} undershoots. With the high gain of the comparator, it is possible to generate high-current pulses using a small-size M_{15} transistor, and as a result reduce the regulator output voltage undershoots. The static current consumption of the comparator is 2 µA.

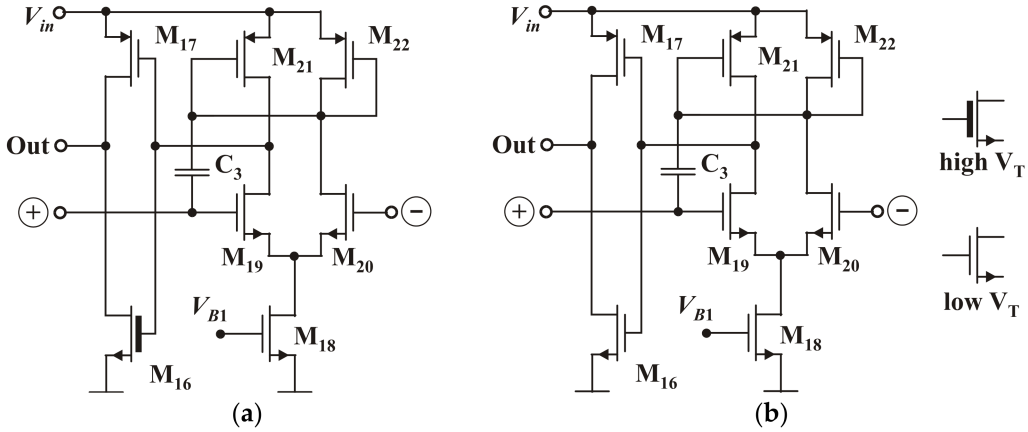


Figure 9. Schematics of the comparator (Cmp) used in the spike detection circuit for: (**a**) V_{out} > 0.85 V and (**b**) 0.85 V > V_{out} > 0.7 V.

Complete schematics of ALDO regulators are shown in Figures 10 and 11, where the undershoot detection circuit is surrounded by a dashed line. The frequency characteristics of the negative loop are mainly determined by 5 poles and one transmission zero, which are associated with the nodes labeled A–E.

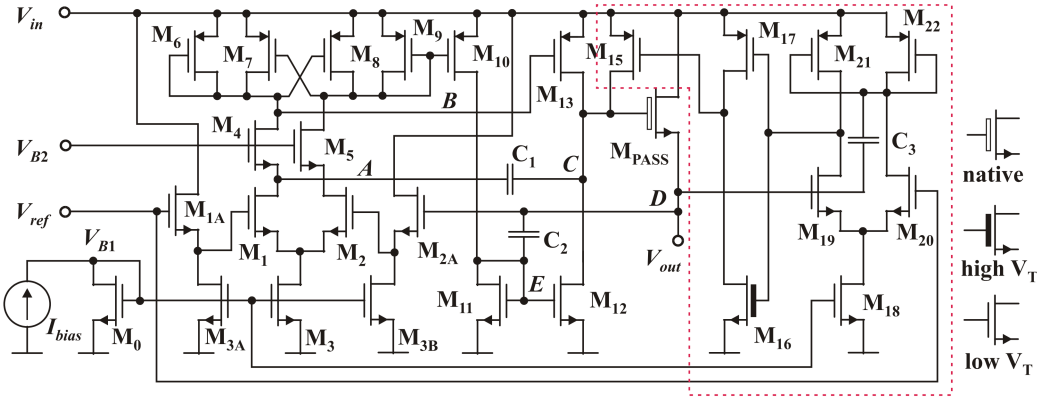


Figure 10. Complete schematic of LDO regulator with a native n-channel transistor and spike detection circuits for V_{out} > 0.85 V.

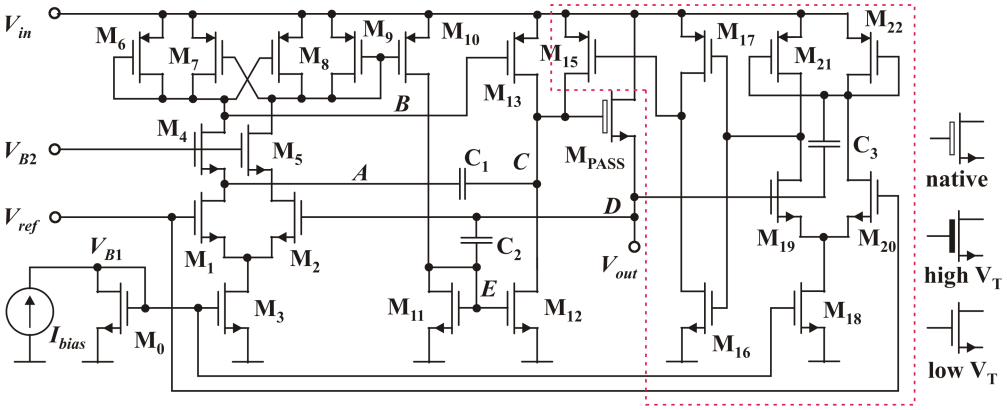


Figure 11. Complete schematic of LDO regulator with a native n-channel transistor and spike detection circuits for 0.85 V > V_{out} > 0.7 V.

Based on the method described in [17,18], the approximated equations describing the poles and zero were determined

$$p_D \approx \frac{1}{g_{m13} R_C R_B C_1} \tag{4}$$

$$z \approx \frac{g_{m4}}{C_1} \tag{5}$$

$$p_2 \approx \frac{g_{m13} C_1}{C_C C_B} \tag{6}$$

$$p_3 \approx \frac{g_{m4}}{C_C} \tag{7}$$

$$p_4 \approx \frac{g_{m12} C_2}{C_E^2} \tag{8}$$

$$p_5 \approx \frac{g_{mPASS}}{2C_L + C_{gsPASS}} \tag{9}$$

where:

$$R_B \approx \frac{1}{g_{m6} - g_{m7} + g_{ds6} + g_{ds7}} \tag{10}$$

$$R_C \approx \frac{1}{g_{ds13} + g_{ds12}} \tag{11}$$

$$C_B \approx C_{gs6} + C_{gs8} + C_{gs13} \tag{12}$$

$$C_C \approx \begin{cases} C_{gdPASS} & \text{—low } I_{out} \\ C_{gdPASS} + C_{gdPASS} & \text{—high } I_{out} \end{cases} \tag{13}$$

$$C_E \approx C_{gs11} + C_{gs12} + C_{gd10} \tag{14}$$

Equation (4) defines the dominant pole p_D. The effect of poles p_2 and p_4 on stability can be neglected, because they are always well above the unity-gain bandwidth (UGB), which is approximately UGB $\approx g_{m1}/C_1$, while $C_B << C_1$, $C_E << C_1$ and $C_E << C_2$. The stability conditions are most influenced by the p_3 and p_5 poles, with the position depending on the gate capacitance C_C and transconductance $g_{m\mathrm{PASS}}$ of the pass transistor $\mathrm{M_{PASS}}$ and the load capacitance C_L, connected to the regulator output. The most critical conditions occur when the capacitance C_L is large and the output current I_{out} is low, and therefore $g_{m\mathrm{PASS}}$ is small. Under such conditions, both poles approach the UGB reducing the phase margin. In the presented ALDO regulator, the position of the dominant pole (4) and consequently the UGB was adjusted by selecting C_1 = 1.8 pF to achieve the worst-case phase margin greater than 45 degrees. Details of the circuits in Figures 10 and 11 are given in Table 1.

Table 1. Parameters of the circuits in Figures 8–11.

Component	*W*/*L* (µm)	Component	*W*/*L* (µm)	Component	*W*/*L* (µm)
M_1, M_2	50/0.22	M_7, M_8	4/0.22	M_{15}–M_{17}	2/0.22
M_{1A}, M_{2A}	20/0.22	M_{10}	10/0.22	M_{18}	10/0.5
M_3	20/0.5	M_{11}	2/0.22	M_{19}	3/0.22
M_{3A}, M_{3B}	2/0.5	M_{12}	8/0.22	M_{20}–M_{22}	2/0.22
M_4, M_5	20/0.22	M_{13}	40/0.22	M_{24}	1.5/0.5
M_6, M_9	5/0.22	M_{PASS}	50 × 100/1	M_{25}, M_{26}	3/0.5
				M_{27}, M_{28}	2/2
C_1 = 1.8 pF	C_2 = 1.5 pF	C_3 = 80 fF	I_{bias} = 0.75 µA		

4. Results of LDO Regulator Simulations

Properties of the regulators shown in Figures 10 and 11 were verified by a series of simulations performed using the Spectre simulator from the Cadence package. Figure 12 shows the time responses of ALDO regulators with the output voltage V_{out} = 0.9 V and 0.7 V, when the output current changes between 0 and 10 mA with the rise and fall times of 100 ns. The dropout voltage is V_{drop} = 80 mV for the V_{out} = 0.9 V regulator and V_{drop}=100 mV for the V_{out} = 0.7 V regulator. From the figure, it can be seen the overshoot and undershoot with amplitudes $+\Delta V_{out}$ = 66 mV and $-\Delta V_{out}$ = 54 mV for V_{out} = 0.9 V and V_{out} = 0.7 V regulator. Magnified sections of the V_{out} plot showing details of voltage spikes for V_{out} = 0.9 V regulator are presented in Figure 13. These plots also show the drain currents of the transistors M_{15} and M_{12}.

Figure 13a shows the moment when the voltage V_{out} drops below the comparator threshold voltage, and at this time the transistor M_{15} generates a high-current pulse with short rise and fall times, which quickly charges the input capacitance of the pass transistor $\mathrm{M_{PASS}}$, causing a significant reduction in the output voltage undershoot. Note that due to the delay in switching off the comparator, a parasitic voltage overshoot of about 30 mV amplitude is also generated.

Figure 13b shows the details of V_{out} overshoot. In this case, the current pulse generated by M_{12} is approximately two times smaller in amplitude and has much longer rise and fall times, resulting in a wider overshoot of V_{out}. In this regulator, only the simpler solution shown in Figure 4b was used to suppress overshoots, due to the main effort to reduce the total quiescent current. If a stronger overshoot reduction is required, a comparator-based spike suppression circuit can also be used.

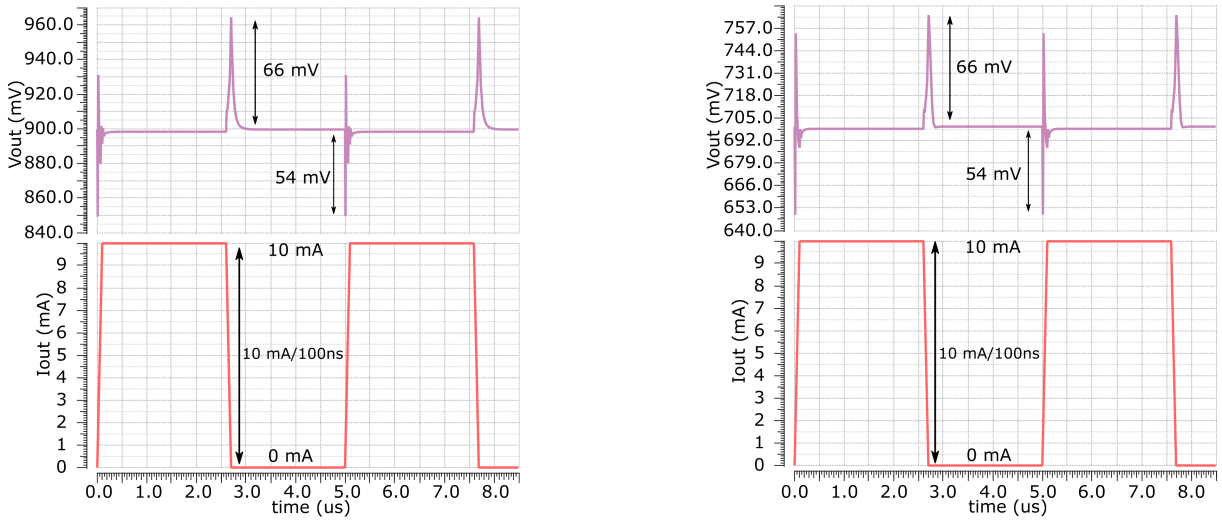


Figure 12. Time waveform of the output voltage V_{out} when the output current changes between 0 and 10 mA with a rise and fall times of 100 ns. The response for ALDO with: (**a**) V_{out} = 0.9 V and (**b**) V_{out} = 0.7 V.

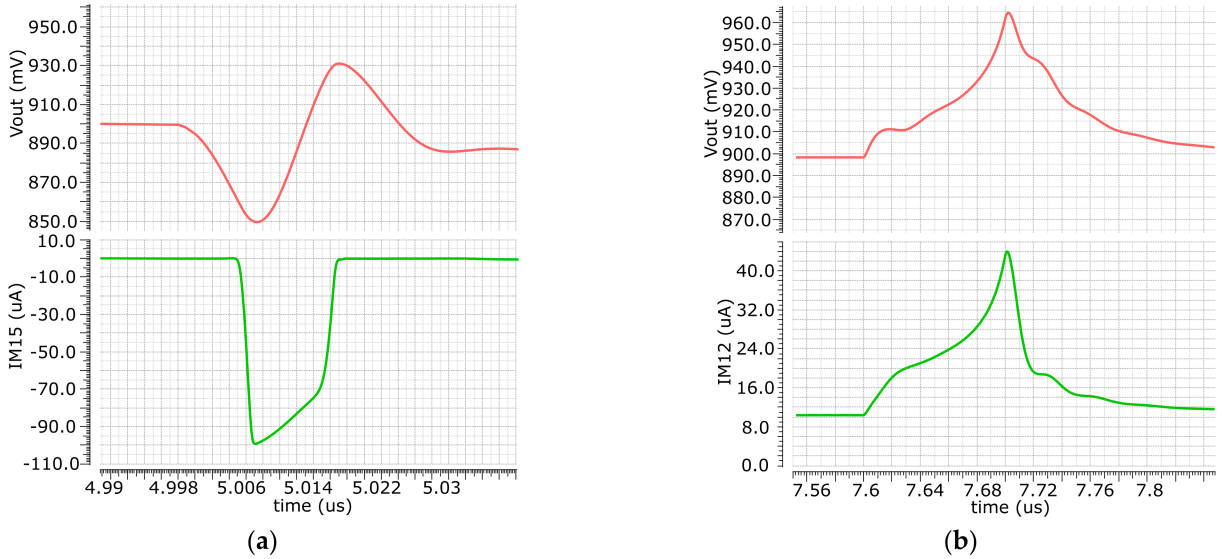


Figure 13. Details of V_{out} time response showing voltage spikes and accompanying drain currents of the transistors M_{15} and M_{12}. ALDO with V_{out} = 0.9 V: (**a**) voltage undershoot details and (**b**) voltage overshoot details.

Plots of PSR as a function of frequency for selected values of the output current I_{out} (0, 2.5 mA, 5 mA, 7.5 mA, 10 mA) are shown in Figure 10. The plot in Figure 14a shows the characteristics of the regulator with a native transistor (Figure 10). For comparison, Figure 14b shows PSR characteristics of an analogous regulator with a low-threshold voltage p-channel pass transistor (M_{PASS}). This regulator was created on the basis of the schematic in Figure 10 by swapping the inputs of the differential pair (M_1, M_2) and adjusting capacitances (C_1 = 3 pF, C_2 = 0) to achieve stable operation. Figure 14a shows that at low frequencies, PSR reaches the highest value for the smallest current (0 mA), which is 61.5 dB and 43 dB for the regulator with the native n-channel and p-channel transistors, respectively. PSR decreases to 46.5 dB for the regulator with the native n-channel transistor when the current increases to 10 mA. Even in this case, PSR is about 6 dB better than the value obtained for the regulator with the p-channel transistor.

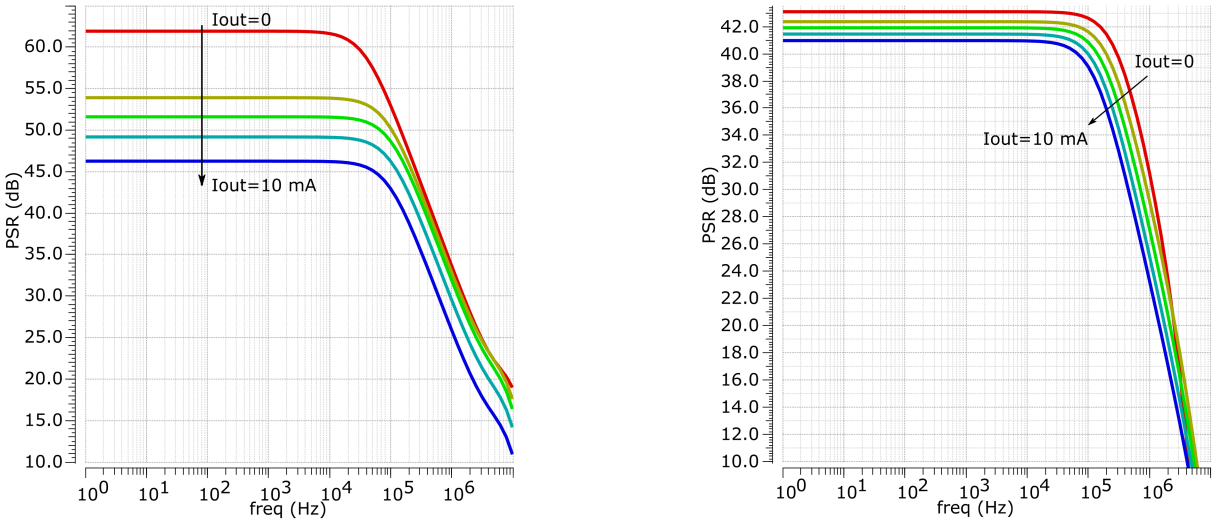


Figure 14. PSR as a function of frequency and the output current I_{out}: (**a**) ALDO regulator in Figure 10 and (**b**) ALDO regulator with p-channel pass transistor.

The following Figures 15 and 16 show plots of the amplitude-phase frequency characteristics of the negative feedback loop for the regulators in Figures 10 and 11.

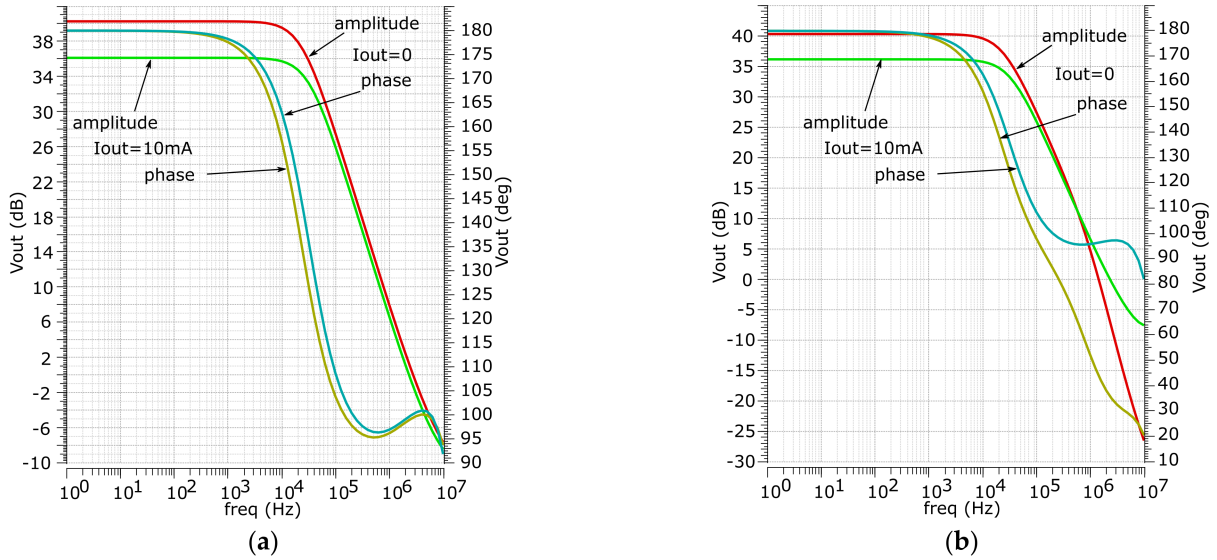


Figure 15. Frequency characteristics of a regulation loop for V_{out} = 0.9 V: (**a**) C_L = 5 pF and (**b**) C_L = 500 pF.

For the regulator with the output voltage V_{out} = 0.9 V, the smallest phase margin is 75 degrees for I_{out} = 0 mA and C_L = 500 pF, whereas the highest margin is 101 degrees for I_{out} = 0 mA and C_L = 5 pF. For all intermediate values in the range I_{out} = 0–10 mA and C_L = 0–500 pF, the feedback loop is stable with the phase margin greater than 75 degrees, and the unity-gain bandwidth in the range of 2–5 MHz. Figure 16 shows the amplitude-phase frequency characteristics of the low-voltage version of the regulator (Figure 11) for V_{out} = 0.7 V. In this case, the smallest phase margin is 45 degrees for I_{out} = 0 mA and C_L = 500 pF and the highest is 77 degrees for I_{out} = 0 mA and C_L = 5 pF. Furthermore, in this case, the regulator is stable for all values in the range I_{out} = 0–10 mA and C_L = 0–500 pF, with the unity-gain bandwidth in the range of 1.8–4 MHz.

A summary of the most important parameters of the proposed LDO regulator along with the values obtained for the process corners (slow nMOS & pMOS transistors, tempera-

ture 0 °C or 50 °C) is summarized in Table 2. In the worst-case corner, the voltage regulator with V_{out} = 0.9 V can operate with a minimal drop voltage of 90 mV with output voltage spikes of less than 70 mV and PSR = 38 dB. The low-voltage version of the regulator, when supplied with V_{in} = 0.8 V, provides an output voltage of V_{out} = 0.7 V with a slightly worse PSR = 35 dB.

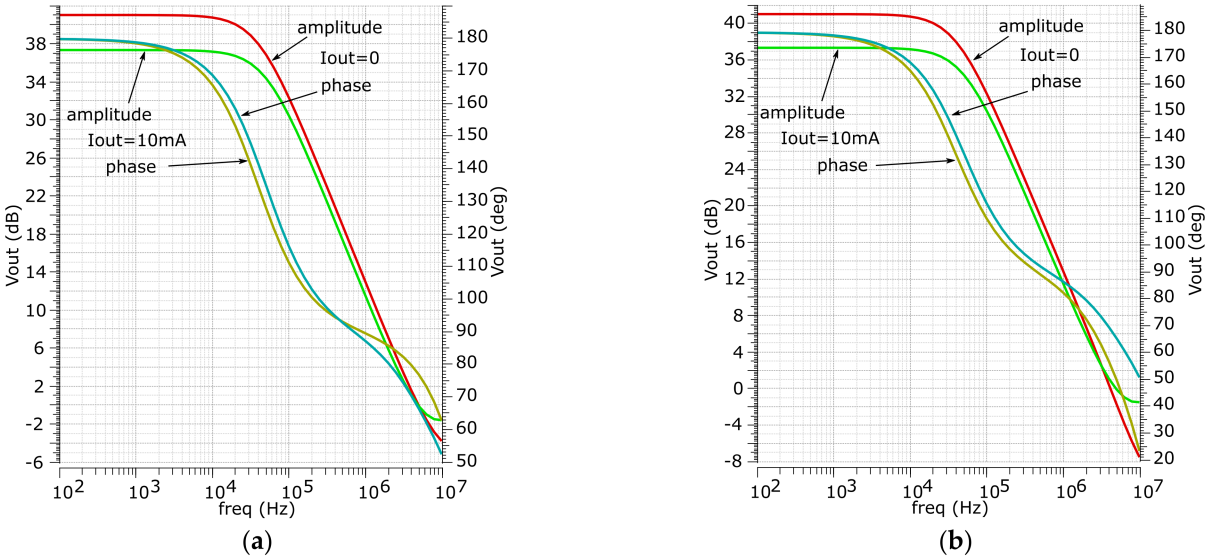


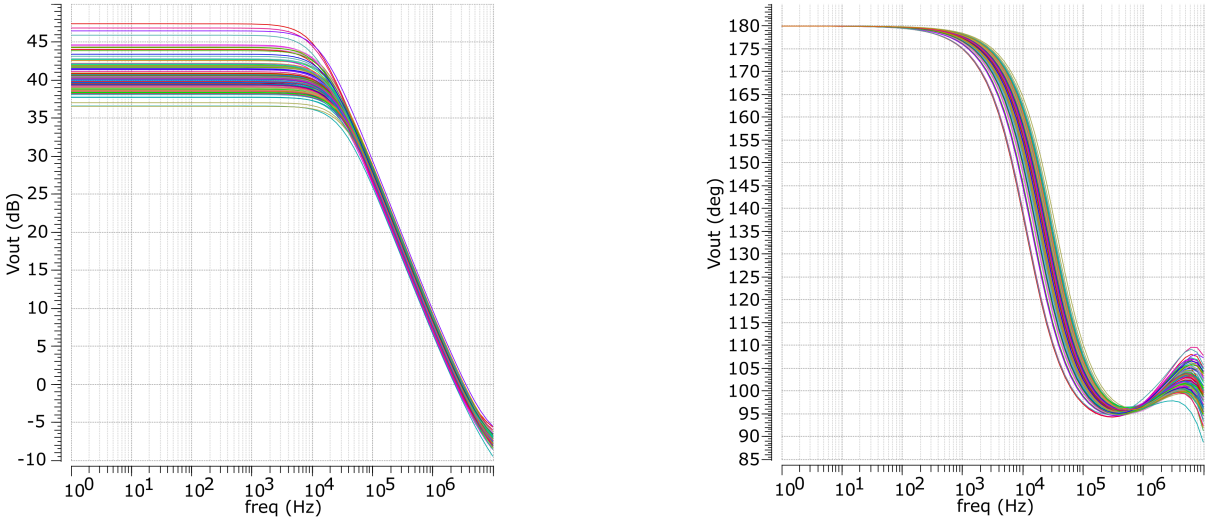
Figure 16. Frequency characteristics of a regulation loop for V_{out} = 0.7 V: (**a**) C_L = 5 pF and (**b**) C_L = 500 pF.

Table 2. Summary of the most important parameters of the LDO regulators.

LDO Regulator for V_{out} = 0.9 V (Figure 5)			
Parameter	**Typical Mean, 27 °C**	**Slow nMOS pMOS, 0 °C**	**Slow nMOS pMOS, 50 °C**
V_{in}	1.8–0.98 V	1.8–0.98 V	1.8–0.98 V
V_{drop}	80 mV	80 mV	90 mV
C_L	0–500 pF	0–500 pF	0–500 pF
$+\Delta V_{out}$	64 mV	62 mV	69 mV
$-\Delta V_{out}$	51 mV	62 mV	65 mV
I_Q	18 µA	18 µA	18 µA
$max\ I_{out}$	10 mA	10 mA	10 mA
η @ I_{max}	99.8%	99.8%	99.8%
$\Delta V_{out}/\Delta I_{out}$	0.15 V/A	0.13 V/A	0.16 V/A
$\Delta V_{out}/\Delta V_{in}$	3.6 mV/V	6 mV/V	6.9 mV/V
$PSR@I_{max}$	46 dB	40 dB	38 dB
LDO Regulator for V_{out} = 0.7 V (Figure 6)			
Parameter	**Typical Mean, 27 °C**	**Slow nMOS pMOS, 0 °C**	**Slow nMOS pMOS, 50 °C**
V_{in}	1.8–0.8 V	1.8–0.8 V	1.8–0.8 V
V_{drop}	100 mV	100 mV	100 mV
C_L	0–500 pF	0–500 pF	0–500 pF
$+\Delta V_{out}$	64 mV	63 mV	70 mV
$-\Delta V_{out}$	52 mV	63 mV	68 mV
I_Q	18 µA	18 µA	18 µA
$max\ I_{out}$	10 mA	10 mA	10 mA
η @ I_{max}	99.8%	99.8%	99.8%
$\Delta V_{out}/\Delta I_{out}$	0.16 V/A	0.18 V/A	0.2 V/A
$\Delta V_{out}/\Delta V_{in}$	4.1 mV/V	6.5 mV/V	7.5 mV/V
$PSR@I_{max}$	43 dB	37 dB	35 dB

The influence of technology parameter variation and component mismatch is illustrated in Figure 17. The plots show the amplitude and phase characteristics of the control loop for 100 Monte Carlo analysis runs. These results show that the gain of the control loop may change from 36 dB to 47 dB, while the phase margin varies from 97 to 110 degrees. Such a range of changes will not result in a loss of loop stability, but may

result in about 50% deterioration of parameters such as line regulation or the regulator output resistance.



(**a**) (**b**)

Figure 17. Results of Monte Carlo simulations of frequency characteristics of a regulation loop for V_{out} = 0.9 V, C_L = 5 pF, I_{out} = 0: (**a**) amplitude and (**b**) phase.

5. Comparison to The State-of-the-Art and Conclusions

The simulation results of the parameters obtained in the proposed voltage regulator were compared with the measurement results of similar solutions described in the literature. A comparative summary is provided in Table 3. The proposed regulator, compared to the regulator with p-channel pass transistor [3] designed in similar 180 nm technology, has a smaller voltage drop V_{drop}, a smaller total on-chip capacitance, and a better response speed, as it is indicated by a smaller FOM and a shorter settling time. Compared to the charge-pump based regulators [10,19], the proposed regulator is better in power efficiency η and has a much smaller total on-chip capacitance. The regulator with a hybrid configuration (ALDO + DLDO) [6] features a very low quiescent current, high efficiency and relatively fast response, though these favorable characteristics were obtained due to a large voltage drop V_{drop} = 300 mV, large total on-chip capacitance 220 pF and a relatively high output voltage V_{out} = 2.7–3.3 V, which can be a significant limitation in low-voltage circuits. ALDO regulators described in papers [4,5,20] use low-voltage p-MOS pass transistors and are designed for low output voltages (0.6 V−0.9 V). Comparing the parameters of these regulators with the proposed regulator, it is seen that the proposed regulator is more favorable in terms of minimum dropout voltage (100 mV versus 150–200 mV). In the solution [20], a particularly low quiescent current (16 nA) was obtained, but this was achieved at the cost of a large (1 µF) off-chip capacitor and degraded transient response (FOM = 0.11). The regulators [4,5] have a favorable transient response, though they require a relatively high quiescent current (112 µA and 65 µA). It should also be noted that in implementations of regulators [4,6,19], the output current must not be less than the minimum value (100 µA, 10 µA, 120 µA), otherwise the regulator may lose stability. The proposed regulator is free from this limitation, which is particularly severe in SoCs with implemented sleep function. This comparison shows that the proposed regulator allows to achieve a satisfactory compromise of parameters important for SoCs powered with a voltage below 1 V.

Table 3. Comparison of ALDO.

Parameters	**[3]**	**[6]**	**[10]**	**[19]**
CMOS tech (nm)	180	500	65	180
Topology	ALDO, p-MOS	hybrid	CP + ALDO, n-MOS	CP + ALDO, n-MOS
Max I_{out} (mA)	50	50	30	10
Min I_{out} (µA)	0	100	0	10
V_{out} (V)	1.6	2.7–3.3	1	1.2
V_{drop} (mV)	200	300	50	600
Quiescent curr. I_Q (µA)	55	0.01	161	265
On-chip cap. (pF)	28	220	540	40
Load cap. C_L (pF)	100	N.A.	260	no limit
PSR (dB@freq. MHz)	70@1	N.A.	12.8@100	41@1
ΔV_{out}/fall time (mV/ns)	75/100	75/10	195/0.2	44/500
Transient load (mA/ns)	50/100	49/10	N.A.	10/500
Load reg. $\Delta V_{out}/\Delta I_{out}$ (V/A)	0.14	1.2	0.2	4
Line reg. $\Delta V_{out}/\Delta V_{in}$ (mV/V)	N.A.	N.A.	N.A.	36.7
Max efficiency η (%)	99.99	99.99	76.2	97.4
FOM [2] (ps)	8000	0.003	0.085	120
Settling time (ns)	600	60	0.254	300
Parameters	**[20]**	**[4]**	**[5]**	**This Work [1]**
CMOS tech (nm)	55	130	65	180
Topology	ALDO, p-MOS	ALDO, p-MOS	ALDO, p-MOS	ALDO, native n-MOS
Max I_{out} (mA)	10	25	20	10
Min I_{out} (µA)	N.A.	120	0	0
V_{out} (V)	0.6	0.8	0.9	0.7–0.9
V_{drop} (mV)	200	200	150	90–100
Quiescent curr. I_Q (µA)	0.016	112	65	18
On-chip cap. (pF)	28	0.73	1.4	3.38
Load cap. C_L (pF)	1 µF	25	0–100	0–500
PSR (dB@freq. MHz)	42.7@50k	57/1	23@1	25@1
ΔV_{out}/fall time (mV/ns)	70/20	22/10	88/5	64/100
Transient load (mA/ns)	10/20	25/10	19.9/5	10/100
Load reg. $\Delta V_{out}/\Delta I_{out}$ (V/A)	1.05	0.17	N.A.	0.15
Line reg. $\Delta V_{out}/\Delta V_{in}$ (mV/V)	0.5	2.25	N.A.	3.6
Max efficiency η (%)	99.99	99.55	99.7	99.8
FOM [2] (ps)	0.11	0.002	0.03	0.058
Settling time (ns)	N.A.	<190	100	120

[1] Results of simulations. [2] FOM = $(C_L \cdot \Delta V_{out} \cdot \mathrm{IQ}/(I_{out,max})^2$.

In this paper, a low-voltage ALDO regulator based on a native n-MOS transistor as a pass element is proposed as a promising alternative to known solutions. In such a regulator, the pass transistor can operate in a common drain configuration, which improves the circuit performance and simplifies its design. The fact that the native transistor, depending on the technology used, has a threshold voltage close to zero or even negative eliminates the need for a charge pump boosting the voltage supplying the error amplifier. Elimination of the charge pump avoids the use of relatively large on-chip capacitors necessary for the pump operation.

The total capacitance used in such pumps can reach several hundred pF, which is a major disadvantage of this type of solution. The proposed regulator under low-voltage conditions allows obtaining satisfactory parameters as compared to the regulators with charge pumps, and classical regulators with a p-channel transistor as a pass element. It is worth noting that the proposed regulator allows to push the limit of application of ALDO regulators to voltages below 1 V with only slight degradation of output voltage spikes, response speed and PSR, which is very difficult to achieve in previously known solutions.

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References

1. Torres, J.; El-Nozahi, M.; Amer, A.; Gopalraju, S.; Abdullah, R.; Entesari, K.; Sánchez-Sinencio, E. Low drop-out voltage regulators: Capacitor-less architecture comparison. *IEEE Circ. Syst. Mag.* **2014**, *2*, 6–26. [CrossRef]
2. Chyan, T.Y.; Ramiah, H.; Muhamad Hatta, S.F.W.; Lai, N.S.; Lim, C.-C.; Chen, Y.; Mak, P.-I.; Martins, R.P. Evaluation and perspective of analog low-dropout voltage regulators: A review. *IEEE Access* **2022**, *10*, 114469–114489. [CrossRef]
3. Park, C.-J.; Onabajo, M.; Silva-Martinez, J. External Capacitor-Less Low Drop-Out Regulator With 25 dB Superior Power Supply Rejection in the 0.4–4 MHz Range. *IEEE J. Solid-State Circ.* **2014**, *49*, 486–501. [CrossRef]
4. Bu, S.; Guo, J.; Leung, K.N. A 200-ps-response-time output-capacitorless low-dropout regulator with unity-gain bandwidth >100 MHz in 130-nm CMOS. *IEEE Trans. Power Electron.* **2018**, *33*, 3232–3246. [CrossRef]
5. Liu, N.; Chen, D. A Transient-Enhanced Output-Capacitorless LDO with Fast Local Loop and Overshoot Detection. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2020**, *67*, 3422–3432. [CrossRef]
6. Huang, J.-R.; Wen, Y.-H.; Yang, T.-H.; Lee, J.-J.; Liu, G.-T.; Chen, K.-H.; Lin, Y.-H.; Lin, S.-R.; Tsai, T.-Y. A 10 nA ultra-low quiescent current and 60 ns fast transient response low-dropout regulator for internet-of-things. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2022**, *69*, 139–147. [CrossRef]
7. Takram, M.A.; Hwang, I.-C.; Ha, S. Architectural advancement of digital low-dropout regulators. *IEEE Access* **2020**, *8*, 137838–137855. [CrossRef]
8. Zhao, J.; Gao, Y.; Zhang, Y.-T.; Son, H.; Heng, C.-H. A 310-nA quiescent current 3-fs-FoM fully integrated capacitorless time-domain LDO with event-driven charge pump and feedforward transient enhancement. *IEEE J. Solid-State Circ.* **2021**, *56*, 2924–2933. [CrossRef]
9. Tan, Y.; Zhan, C.; Wang, G. A fully-on-chip analog low-dropout regulator with negative charge pump for low-voltage applications. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2019**, *66*, 1361–1365. [CrossRef]
10. Lu, Y.; Ki, W.-H.; Yue, C.P. An NMOS-LDO regulated switched-capacitor DC–DC converter with fast-response adaptive-phase digital control. *IEEE Trans. Power Electron.* **2016**, *31*, 1294–1303. [CrossRef]
11. Blakiewicz, G.; Jakusz, J.; Jendernalik, W. Starter for Voltage Boost Converter to Harvest Thermoelectric Energy for Body-Worn Sensors. *Energies* **2021**, *14*, 4092. [CrossRef]
12. Galup-Montoro, C.; Schneider, M.C.; Machado, M.B. Ultra-Low-Voltage Operation of CMOS Analog Circuits: Amplifiers, Oscillators, and Rectifiers. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2012**, *59*, 932–936. [CrossRef]
13. Garimella, A.; Rashid, M.W.; Furth, P.M. Reverse Nested Miller Compensation Using Current Buffers in a Three-Stage LDO. *IEEE Trans. Circuits Syst. II Exp. Briefs* **2010**, *57*, 250–254. [CrossRef]
14. Chen, F.; Lu, Y.; Mok, P.K.T. A Fast-Transient 500-mA Digitally Assisted Analog LDO With 30-μV/mA Load Regulation and 0.0073-ps FoM in 65-nm CMOS. *IEEE J. Solid-State Circ.* **2021**, *56*, 511–520. [CrossRef]
15. Or, P.Y.; Leung, K.N. An Output-Capacitorless Low-Dropout Regulator with Direct Voltage-Spike Detection. *IEEE J. Solid-State Circ.* **2010**, *45*, 458–466. [CrossRef]
16. Leung, K.N.; Ng, Y.S. A CMOS Low-Dropout Regulator with a Momentarily Current-Boosting Voltage Buffer. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2010**, *57*, 2312–2319. [CrossRef]
17. Hurst, P.J.; Lewis, S.H.; Keane, J.P.; Aram, F.; Dyer, K.C. Miller Compensation Using Current Buffers in Fully Differential CMOS Two-Stage Operational Amplifiers. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2004**, *51*, 275–285. [CrossRef]
18. Giustolisi, G.; Palumbo, G.; Spitale, E. Robust Miller CompensationWith Current Amplifiers Applied to LDO Voltage Regulators. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2012**, *59*, 1880–1893. [CrossRef]
19. Zarate-Roldan, J.; Wang, M.; Torres, J.; Sanchez-Sincencio, E. A capacitor-less LDO with high-frequency PSR suitable for a wide range of on-chip capacitive loads. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2016**, *24*, 2970–2982. [CrossRef]
20. Adorni, N.; Stanzione, S.; Boni, A. A 10-mA LDO With 16-nA IQ and Operating From 800-mV Supply. *IEEE J. Solid-State Circ.* **2020**, *55*, 404–413. [CrossRef]