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Implementation of an Adaptive Method for Changing the Frequency Division of the Counter Clock Signal in a Frequency-to-Code Converter

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Abstract: Processing physical quantities into an indirect signal is a standard method of transferring information about the measured quantity to the master system, which analyzes the data obtained from the acquisition system. The intermediate signal is very often the voltage, but another transmission medium can be the frequency of the output signal of the "physical quantity-to-frequency" converter. The article presents the implementation of the adaptive method of selecting the clock signal frequency of the counter working in the converter. The issue of selecting the clock signal frequency for the required processing range of the transducer is discussed in detail. The application of the method using the STM32L476RG microcontroller is presented. The principle of checking the processing range of the developed transducer model is discussed. The algorithms of transducer operation in basic and adaptive modes of measuring the period of the variable frequency signal are proposed. The results of operation, in both modes, of the transducer model of frequency processing are presented, along with the metrological analysis of the results. The influence of selected approximations used to reconstruct the measured quantity on the final presentation of the measurement result is discussed.

Keywords: instantaneous frequency; frequency measurement; frequency-to-code converter

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1. Introduction

The conversion of physical quantities into an indirect signal is a constantly developing field of metrology [1–5]. It is used for data transmission and processing in master systems, which can be, for example, PCs or other microprocessor systems with sufficient computing performance for a given application. Very often, the intermediate signal is the voltage [6,7], which can be easily converted into a digital form using an analog-to-digital converter. Another possibility is to use the frequency of the transducer's output signal as an intermediate carrier of information [8]. The frequency itself can also provide information about the examined phenomenon, such as, for instance, the stability of power grid operation, the variability of the voltage generated by photovoltaic inverters, power plant frequency control capabilities [9], etc. The frequency of the signal can be directly processed into numerical values [6,10], but in the case of time-varying values, this issue is still the subject of many publications [1,11–16] and research on new solutions [17–24]. The intensity of the research is favored by: high availability of converters of physical quantities into frequency (X/f) [25], low sensitivity of the information transmission channel using the frequency signal to electromagnetic interference and amplitude attenuation [26,27], high accuracy of constant frequency measurement, and widely available programmable systems containing counters enabling high accuracy frequency measurement [28,29].

The increasing offer of X/f converters and the continuous development and creation of new innovative constructions enabling the measurement of time-varying parameters have entailed the need to develop methods of variable-frequency processing [30].

Constant-frequency measurement is most often carried out using the digital method. Systems for digital measurement of constant frequency and period are well-known and widely described in the literature on metrology [6]. The frequency meter usually includes a counter system, a standard frequency generator, an input signal conditioning system, and a decoder to convert the information about the measured frequency read from the counter into readable form. The result of this decoding is presented on the display or passed to another part of the system. The operation of the frequency counter is based on the principle of summing up the pulses signaling the end of the current period and the beginning of the next period of the measured frequency signal [25]. The quotient of the number of summed pulses and the measurement time is an approximation of the measured frequency. In the case of period measurement, the pulses from the reference generator are summed up during the full period of the processed signal [17].

The length of the period is determined by the product of the counter state and the length of the clock signal period. Provided that the design of the instrument for measuring frequency and period has been developed correctly, i.e., a Schmitt trigger [25] is used in the input channel of the meter, and the conditions for stable operation of the reference signal generator have been ensured, the main source of the measurement error is the quantization error [31]. The constant frequency measurement result is stable and can be presented in a readable form on the instrument's display.

Unlike a constant frequency meter, processing a variable frequency signal into a clear presentation of the measurement data requires a more complex measurement system, which will allow for more advanced data processing. Although counter systems are also often used in this case [6,25], the further data processing procedure is more complicated. The variable frequency of the signal makes a direct presentation of the result on the display impossible. In addition, due to its variability, it seems reasonable to measure the frequency indirectly, through digital measurement of the period, or more precisely, subsequent periods of the processed signal. Knowledge of the length of successive periods will enable the most complete mapping of changes in the quantity processed by the X/f converter. The consequence of the proposed method of frequency measurement is the need to collect the measurement data in order to present it in a clear form on a graph of the measurand $x(t)$ as a function of time. Typically, this data is later used to create other, more complex reports. Due to the nature of the operation of the system converting frequency into numerical values, this type of device is called a "frequency-to-code" converter and is marked with the symbol f/N [10]. An example of the structure of the f/N converter that allows continuous processing of the signal period using a single counter is shown in Figure 1.

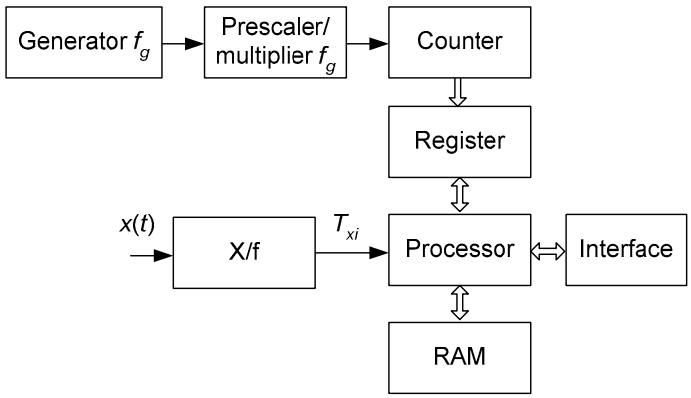

Figure 1. Sample structure of the f/N converter with single counter.

It is obvious that the acquisition of a volume-relevant set of numerical values for subsequent visualization, analysis, and archiving requires an adequately capacious memory in the system [32] and an interface that will allow for the effective transfer of the measurement data from the f/N converter to the master computer. An alternative to storing the data in the RAM of the f/N converter may be the transmission of consecutive numerical values

obtained during the measurement directly to the master computer. However, this requires a careful analysis of the possibilities of data acquisition and transmission by the f/N converter and the possibility of receiving and archiving the measurement data sent by the computer controlling the measurement process [33]. As a consequence, taking into account the need to store a large amount of data, regardless of the storage method, it becomes reasonable to develop methods to reduce the memory occupied by the stored data. One of the possibilities is to limit the transmitted single numerical values to a variable with an acceptable number of bits, corresponding to the number of bits in the counter register used. Usually, 8- and 16-bit counters are available, but some microprocessor systems also offer 32-bit counters. Often, universal counters in microprocessor structures can be configured to create a counter structure with a larger capacity. Figures 2–4 show three graphs of theoretically achievable frequency measurement range for different sizes of the counter register. Each measurement range is limited by the assumption that the relative value of the quantization error will not exceed 1%, i.e., the minimum number of pulses registered by the counter of the f/N converter is 100. The quantization error is calculated according to the formula:

$$\delta_k = \frac{T_g}{T_{xi}} 100\%, \tag{1}$$

where: T_g—is the period of the clock generator signal with frequency f_g, and T_{xi}—is the period of the processed signal.

The lower limit of each of the presented ranges is the product of the maximum meter state and the length of the period T_g.

Figure 2 shows the measurement ranges for a meter with an 8-bit register, which gives a data set consisting of numbers with the least use of the measurement system memory. It can be seen that for the clock signal used by the counter with the frequency f_g = 80 MHz, it is theoretically possible to measure the maximum frequency of 800 kHz, while the lowest measurable frequency for f_g = 1 MHz and the maximum state of the counter 255 is about 3921.57 Hz.

Unfortunately, it can be seen that the three selected frequencies f_g allow processing only in a discontinuous frequency range of the processed signal. In order to enable measurement in a continuous range, a more frequent change of the f_g frequency division degree would be required, which would generate additional data informing about the set frequency division degree [31]. As a consequence, the effect of memory saving would be minimal, while continuous changes in the frequency division could lead, in extreme cases, to unstable operation of the measurement system.

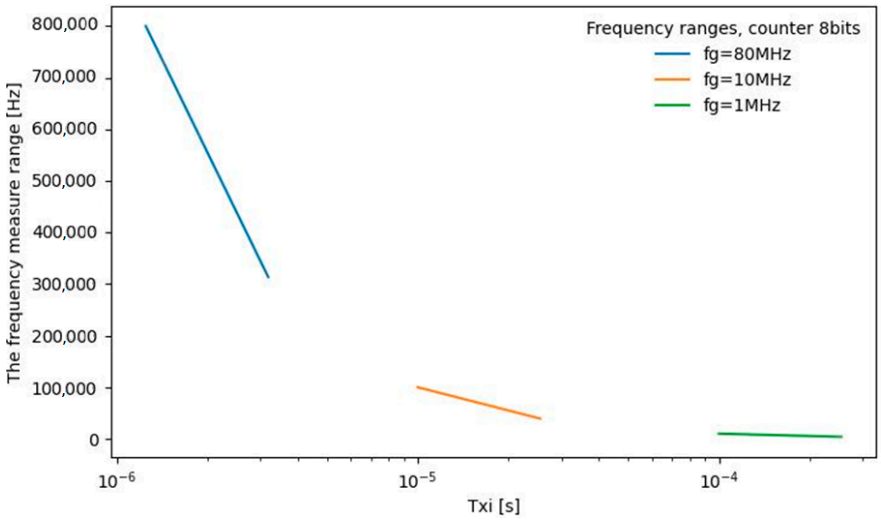

Figure 2. Measuring ranges for a counter with an 8-bit summing register.

Figure 3 shows the measurement ranges for a meter using a 16-bit register. The proposed frequencies of the clock signal allow obtaining a continuous measuring range, whereby for f_g = 80 MHz, the maximum range of 800 kHz is obtained, as before, while the minimum frequency for f_g = 1 MHz and the maximum state of the counter 65535 is about 15.26 Hz.

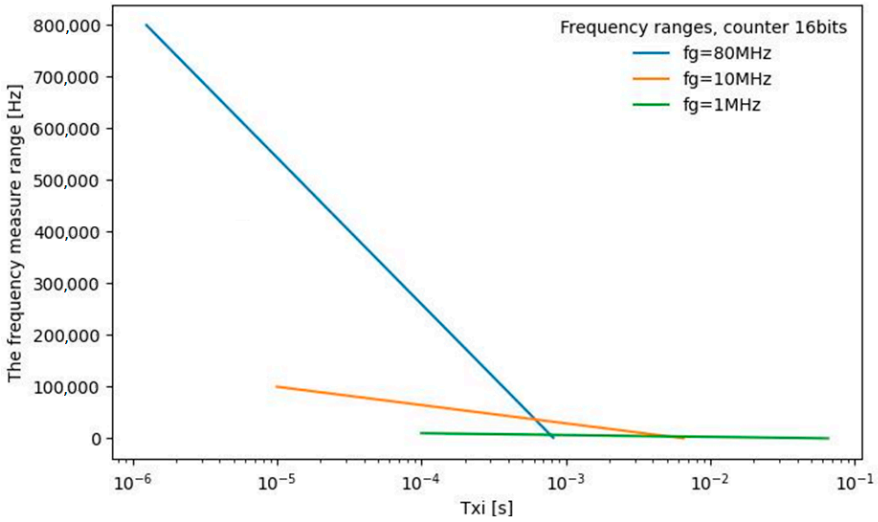

Figure 3. Measuring ranges for a counter with a 16-bit summing register.

Figure 4 shows the measurement ranges for a counter with a 32-bit register. In this case, it can be seen that the measuring range is the widest. Like for the previous counters, for f_g = 80 MHz, the limit value of the 800 kHz range is obtained, as imposed by the value of the minimum state of the counter register. In the range of the lowest frequencies, for f_g = 1 MHz and the maximum counter value of 4,294,967,295, a very significant reduction of the measurable values to the level of about 232 µHz is obtained. However, the wide measurement range of the 32-bit counter requires twice as much memory to store the measurement data as the 16-bit counter.

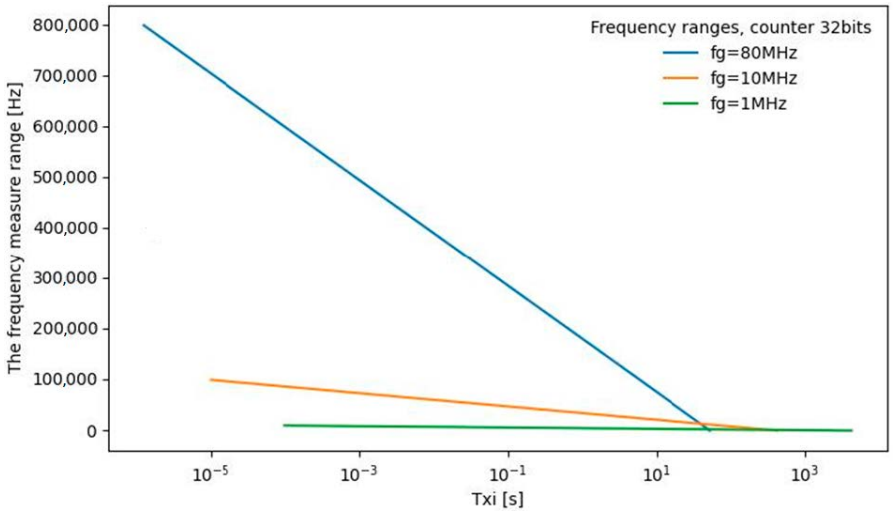

Figure 4. Measuring ranges for a counter with a 32-bit summing register.

In summary, it is reasonable to say that the f/N converter with a 32-bit counter can be used when it is necessary to measure very low frequencies, while in other cases it seems better to use a 16-bit counter with switching the division degree of the clock signal frequency f_g in the prescaler, depending on the instantaneous value of the measured frequency.

Taking into account the above considerations, it was assumed in the further part of the work that a 16-bit counter will be used in the tests, which will allow counting in the range from 0 to 65,535 and saving the instantaneous value of the summing register in an additional register.

The aim of the article is to present an example of the implementation of the method to change adaptively the frequency division of the counter clock signal working in the f/N converter and thus extend the range for low frequencies processed by the f/N converter with a 16-bit counter.

2. Processing of Successive Periods of the Signal

The test signal frequency f_{xi} corresponding to each successive period of T_{xi} is determined indirectly. The value of f_{xi} is calculated from the formula:

$$f_{xi} = \frac{1}{T_{xi}} \tag{2}$$

Neglecting the quantization error (1), the approximate value of T_{xi} is calculated as the product of the period T_g and the state N_{xi} of the f/N converter counter:

$$T_{xi} \approx T_g N_{xi} \tag{3}$$

One of the possible implementations of the functionality of the f/N converter is the use of a microprocessor system [34], which typically includes counter circuits, memory, interfaces, and a reference frequency generator. Its structure enables the design of a system that implements the functionality of digital signal processing [33].

The principle of continuous processing of the period T_{xi} of a variable frequency signal (hereinafter referred to as the frequency signal) by means of a system containing one counter (Figure 1) is shown in Figure 5 [31]. The first graph from the top presents the quantity $x(t)$ processed in the physical quantity-frequency converter, while the next graph shows the signal of the output voltage $U_{Xf}(t)$ of the X/f converter. The period of this signal is proportional to the instantaneous value of quantity $x(t)$. The third graph shows the voltage $U_g(t)$ generated at the output of the clock signal generator, and finally, the last graph presents the time-varying state $N(t)$ of the counter of the f/N converter working continuously. The instantaneous values of the counter state N_i are read at times t_i of the occurrence of pulses constituting the boundary of successive periods T_{xi}.

$$x(t) = \frac{1}{ST_{xi}} = \frac{1}{ST_g(N_{i+1} + N_{\max} * O - N_i)}, \tag{4}$$

where O is the number of recorded meter overflows and S is the sensitivity of the X/f converter.

In normal practice, if only hardware processing of successive N_{xi} values is required, only one case of overflow can be recorded. Storing the information about successive overflows requires the use of RAM to create an additional software counter. In applications requiring the fastest possible processing of subsequent T_{xi} periods, a much better solution will be to use another counter that counts overflows or to replace the used counter with another unit with a larger capacity.

The absolute value of the total absolute error of processing the information about the quantity $x(t)$ carried by the frequency of the input signal by the f/N converter is the sum of two errors. The first is the absolute frequency measurement error Δ_{fT} resulting from the formation of the quantization error in the T_{xi} measurement. The frequency f_{xi} is calculated indirectly from the measured values of T_{xi}; hence, this error should be calculated using the total differential method:

$$\Delta_{fT} = \left|\frac{\partial f_{xi}}{\partial T_{xi}}\right| |\Delta T_{xi}|. \tag{5}$$

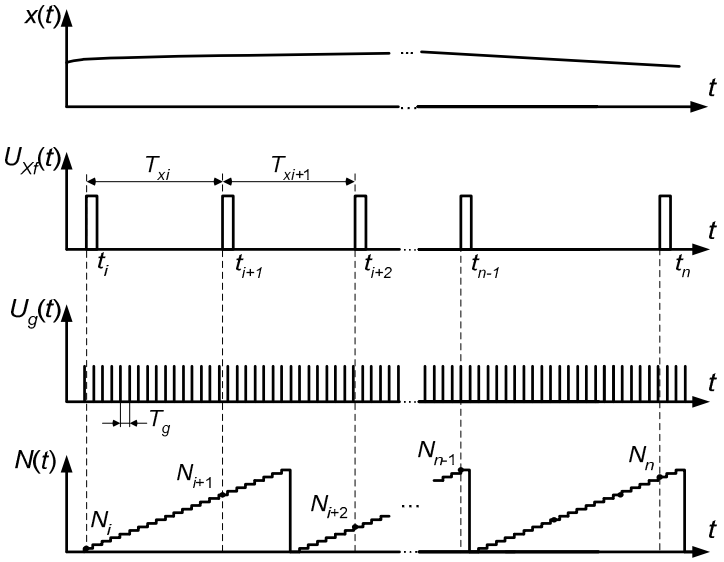

Figure 5. The principle of processing the period of variable frequency signal using a system with one counter [31].

Taking into account relations (2) and (4) and that the absolute quantization error of the T_{xi} measurement is $\pm T_{xi}$, after relevant substitutions the relation for Δ_{fT} takes the form:

$$\Delta_{fT} = \left| \frac{\partial\left(ST_{xi}^{-1}\right)}{\partial T_{xi}} \right| T_g. \tag{6}$$

Determining the derivative in the above relation gives the final formula for the error Δ_{fT}:

$$\Delta_{fT} = \frac{ST_g}{T_{xi}^2}. \tag{7}$$

The other component of the total error is the absolute averaging error [31]. Finally, for a sinusoidal test signal:

$$x(t) = X_0 + X_m \sin(2\pi Ft), \tag{8}$$

where F is the frequency of $x(t)$, X_m is the amplitude of $x(t)$, and X_0 is the constant component of $x(t)$, the absolute total error is given by the formula:

$$\Delta_{\Sigma} = \frac{ST_g}{T_{xi}^2} + SX_m\left(1 - \frac{\sin \pi FT_{xi}}{\pi FT_{xi}}\right). \tag{9}$$

On the other hand, the total relative error of information processing related to the current value of the frequency f_{xi} is given by the formula:

$$\delta_{\Sigma} = \left(\frac{T_g}{T_{xi}} + \frac{f_m\left(1 - \frac{\sin \pi FT_{xi}}{\pi FT_{xi}}\right)}{f_{xi}} \right) \cdot 100\%. \tag{10}$$

where f_m is the amplitude of the frequency change calculated as the product of the amplitude of $x(t)$ and the sensitivity of the X/f converter.

The graphs of the total error of information processing by the f/N converter are shown in Figure 6 for different selected values of the converter counter clock frequency and the assumed frequency of the waveform $x(t)$ equal to 1 Hz.

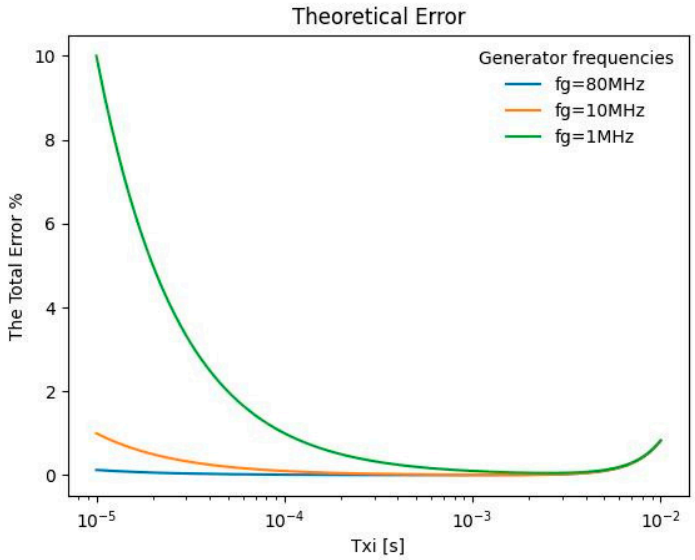

Figure 6. Examples of total error graphs for F = 1 Hz.

3. The f/N Converter Model

This article is intended to present a practical implementation of the method presented in [31] with the use of a selected microcontroller system. The experiments carried out during past studies [33] have revealed that there is a discrepancy between the theoretically achievable measurement range for a counter with a specific pulse summing capacity at a selected clock frequency f_g and the range achievable in real conditions. The performed experiments have shown that the speed of implementation of many transducer functionalities is very important, including the execution of numerical operations by the processor, counter service, communication with the memory, and the interface used for communication with the master computer. The size of the operational memory needed for calculations and data storage is also important. It turned out that the performance of the popular 8-bit microcontrollers of the AVR family [33] allowed theoretically to process signal frequencies in a wide range. After assuming a quantization error of 1% and using a clock frequency of 16 MHz and a 16-bit counter, it should theoretically be possible to measure frequencies up to 160 kHz. Unfortunately, popular microcontrollers usually have a small amount of RAM, which significantly limits their ability to collect data. An attempt to transmit the measurement data directly resulted in a dramatic limitation of the measurement range down to about 10 kHz. Increasing the frequency of the tested signal meant that the microprocessor did not correctly detect limit pulses for subsequent T_{xi} periods (Figure 5), and, as a result, the frequency was twice as high as that actually measured. The number of undetected limit pulses and the number of incorrect measurements increased with the increase in frequency measured [33].

Taking into account the above considerations, it was assumed that a more efficient 32-bit microcontroller with a memory size sufficient to collect enough data to evaluate the operation of the method would be used.

To create the f/N converter model, the NUCLEO-L476RG runtime board was chosen to contain a 32-bit STM32L476RG microcontroller equipped with an ARM Cortex-M4 core.

In addition, the Nucleo-L476RG set was equipped with an ST-LINK programmer that allows the microcontroller to be programmed directly into the operating system via the USB interface and a dedicated application. The programmer also allows for debugging the processor's operation, i.e., for current analysis of the program stored in the flash memory of the microcontroller. Various programming languages and environments can be used to create the code for the microcontroller, e.g., Keil, IAR, and the environment developed by STM Microelectronics. A set of programming tools included in the STM32Cube was used in the work on the project of the f/N converter discussed in the article.

A 16-bit general-purpose counter, T3, was selected to implement the f/N converter. According to the technical documentation of the module, this counter can be controlled at a maximum frequency of 80 MHz. The microcontroller clock signal frequency can be produced in various ways. After purchase, the development kit is configured to work with an internal RC resonant system producing a frequency of 16 MHz. Other useful alternatives for the implementation of the f/N converter, which will give a more stable clock signal, are the external resonator and the resonator of the ST-LINK programmer. Measurement experiments were carried out to check the stability of the f/N converter by measuring selected frequencies in the range of 1221 Hz to 200 kHz, each time collecting a set of data representing 24,000T_{xi} periods. Due to the stability of the RC generator specified by the manufacturer at a level of ±1%, it was concluded that carrying out the test of the RC system was unnecessary. The operation of the checked f/N converter was controlled sequentially from three clock signal sources: two external quartz resonators produced by different manufacturers with a resonant frequency of 16 MHz and the ST-LINK programmer generating a clock frequency of 8 MHz. For each set input frequency of the f/N converter, the average value from a series of 24,000 results was calculated, and then the absolute error was calculated as the difference between the calculated average value and the value that should be measured if the set frequency was measured without error. The results of the calculations in the form of the absolute error vs. frequency plot are shown in Figure 7. The waveforms f_{g1} and f_{g2} describe the graphs of errors obtained for clock signals from external resonators, while the graph f_{g3} represents the measurement error when using the clock signal from the ST-LINK programmer.

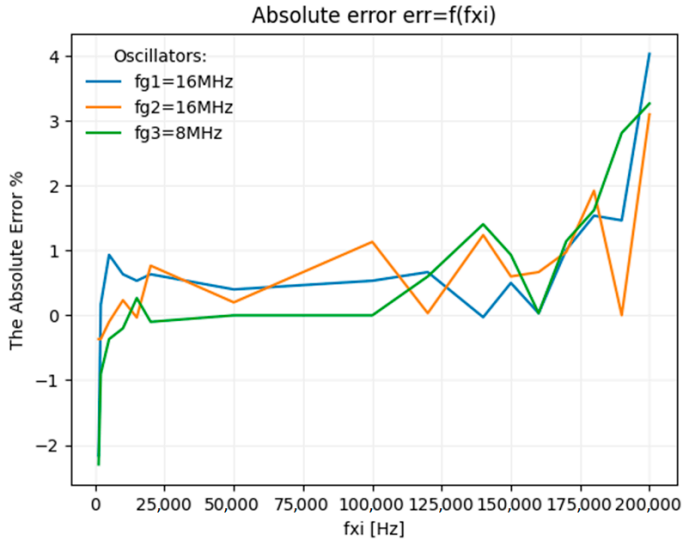

Figure 7. Absolute error of constant frequency measurement for individual resonators.

The average values of the absolute deviation of the N_{xi} value from the set value show that the work with the clock signal sent from the programmer is the most stable, where the error for frequencies up to 100 kHz is practically negligible. The clock signals from the 16 MHz crystal oscillators are basically comparable to each other. In these two cases, some instability can be observed, but its scale is not high.

The next comparison criterion used to assess the operation of the f/N converter was the number of large measurement errors generated, i.e., the frequency readings differing by more than 5% from the set value. The results are presented in Figure 8. The markings of the waveforms on the graph are analogous to those in Figure 7. Due to the need to present the stability of the f/N converter, the maximum of the y-axis representing the number of registered deviations is limited to 3. It can be seen that the occurrence of measured values deviating from the N_{xi} value by more than 5% is a great problem in the field of

measurement errors. In this case, the transducer worked most stably using the programmer resonator.

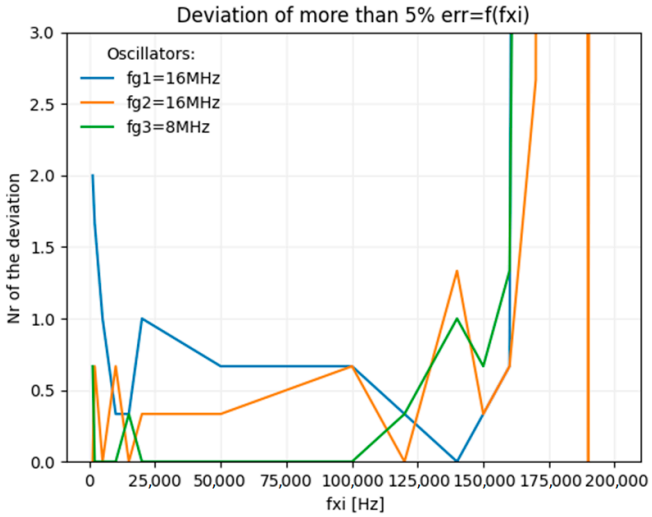

Figure 8. The average number of recorded deviations above 5% for individual resonators.

As a result of the conducted experiments, it was found that the clock signal generated in the programmer has the highest accuracy and stability and ensures the best working conditions for the f/N converter. Consequently, it was assumed that the clock signal generated by the programmer of the development kit would be used for further work. The configuration of the microcontroller enabling the generation of the clock frequency f_g = 80 MHz for the counter is shown in Figure 9.

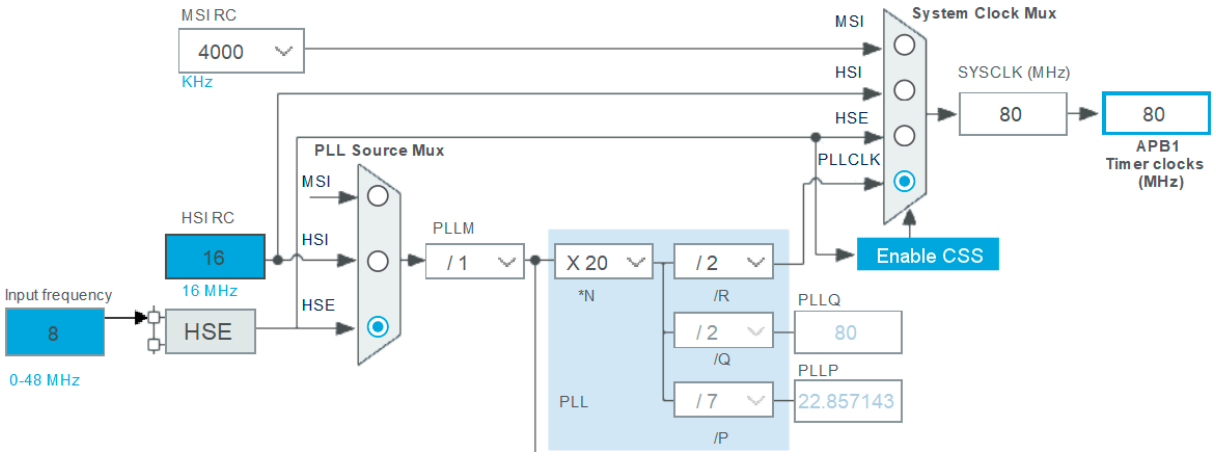

Figure 9. Clock frequency configuration in the STM32CubeIDE environment.

The converter has been developed according to the structure shown in Figure 1. A 16-bit T3 counter was selected to work as the working counter of the f/N converter. The counter was connected to the processor's internal APB1 bus. The maximum settable clock frequency of 80 MHz was used (Figure 9).

The T3 counter allows you to select and change the frequency division of the counter's clock signal. It also has a register that captures the current value stored in the summing register. A global interrupt for the T3 counter with the number 1 has been set to handle the operation of the counter.

Instead of the X/f converter, a programmable Agilent 33220A generator was used as the reference signal source [35]. The manual for the previous model of the generator marked HP 33120A [36], contains the information that the frequency signal is generated with an

accuracy of 0.05% for each pulse for a modulation frequency F less than 600 Hz. Taking into account that the frequency F expected to be set in the tests is in the range $0 < F \leq 50$ Hz [31], this accuracy was found satisfactory. The use of a programmable generator instead of the X/f converter additionally made it possible to resign from the analysis of the X/f converter error, which was considered unnecessary from the point of view of the present work.

The generated frequency signal was passed to the PA6 line of the microcontroller. A total of 90 kB of RAM was used for data collection, which allowed for the collection of 45,000 two-byte numbers representing successive T_{xi} periods. The USART2 interface was used for data transmission to the master computer.

4. The Working Algorithm of the f/N Converter Model in the Basic Mode

Figure 10 shows the working algorithm that performs the processing of successive periods of the frequency signal in the basic mode. Turning on the microcontroller power supply starts the initialization of internal microcontroller modules and sets the default values of the system registers. The next step is to set the required configuration of the microcontroller pins and configure the USART2 interface. To obtain an acceptable transfer time, the data transfer rate was set to 1 Mb/s. A frame of 8 data bits, 1 stop bit, and no parity check was used. After the configuration, communication with the PC is started. The last step is setting the parameters of the T3 counter. It can be seen that saving the counter state during the processing of successive T_{xi} values will be forced at the rising edge of the frequency signal.

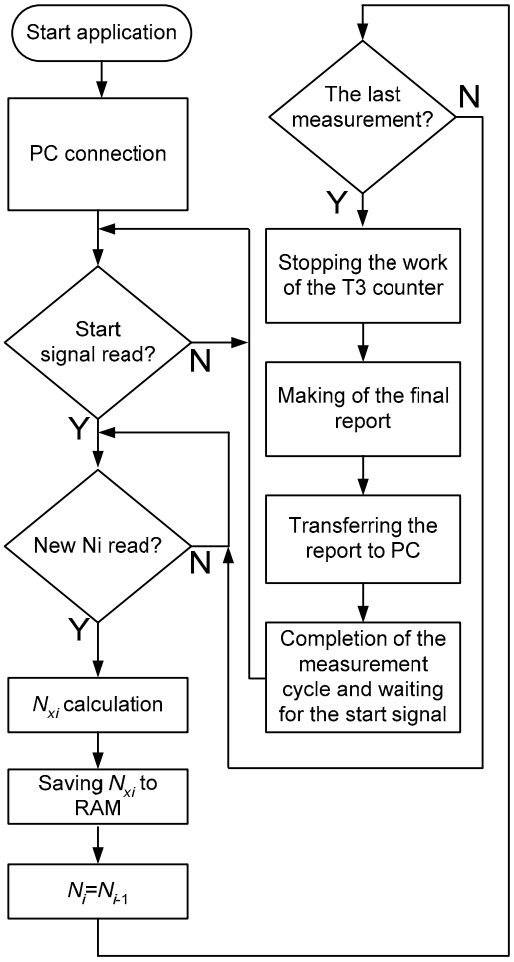

Figure 10. Algorithm of the f/N converter implementing the basic operating mode.

After completing the configuration, the f/N converter program sends its readiness for measurements to the PC.

Sending the command to start measurements by the PC starts the procedure of processing subsequent T_{xi} periods. It is carried out by the main program in cooperation with the interrupt handling procedure generated when the T3 counter detects the rising edge of the frequency signal. The working algorithm of the procedure handling the interrupt generated by the counter is shown in Figure 11. Due to the need to obtain the maximum speed of the f/N converter, the procedure contains only the commands necessary to carry out the measurements. Its task is to read the number N_i from the counter, assign it to a variable in the program, and set a flag informing the main program about the readout.

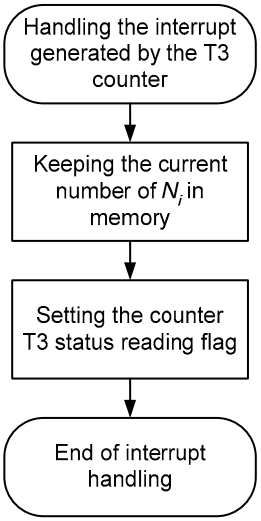

Figure 11. Algorithm of the procedure reading the current state of the T3 counter summing reg.

Further processing of the read information is performed in the main program. The stored value Ni is used to calculate the number N_{xi}, which represents the measured period T_{xi}. The current value of N_{xi} is calculated from the formula:

$$N_{xi} = N_{i+1} + N_{\max} * O - N_i. \tag{11}$$

The counter overflow is detected by analyzing the sign of the difference between N_i and N_{i-1}. A negative difference sign indicates that an overflow has occurred. Then, the maximum number of states that can be recorded by the counter is added to the difference; for a 16-bit counter, it is 2^{16}. The calculated N_{xi} is stored in the RAM. Controlling the sign of the difference between the numbers N_i and N_{i-1} is sufficient under the assumption that T_{xi} will not be greater than the product of $T_g * N_{max}$. Otherwise, it is necessary to use the counter overflow count control.

The value of N_i, after calculating N_{i-1}, is stored as N_{i-1} for calculation in the next iteration of the program. After reaching the complete set of data, the program stops the work of the T3 counter and generates the final report containing the saved data set and additional information about the measurement performed. The report is passed to the PC. Finally, the f/N converter program waits for the next measurement start command.

Before testing the f/N converter model, it was necessary to define the upper and lower measurement range limits. As already mentioned, the lower limit of the measurement range is the product of the period T_g of the clock signal used and the capacity of the meter used. For the assumed clock frequency f_g = 80 MHz and the counter capacity of 16 bits, the lower measurement limit is approximately equal to 1221 Hz.

Next, the upper limit of the measuring range was determined. It was assumed that a satisfactory method of determining the upper limit of the measurement range would be to analyze 1 million consecutive constant frequency measurements and verify that the measurement results are consistent with theoretical considerations and do not exceed the expected total error range (10). Measuring a frequency twice as low as expected would

mean that the f/N converter model failed to detect the boundary between the T_{xi} data and summed up their lengths, thus producing an erroneous result. The maximum frequency for which erroneous measurements are not recorded was considered the upper limit of the measurement range. Due to the need to expose the exact maximum and minimum values of all measurements, it was decided that instead of a histogram, a graph of the measured frequency in time would be presented.

The results of the measurements performed are shown in Figures 12–14. Figure 12 shows that the measured frequency of 111 kHz is processed correctly, and all results can be considered correct.

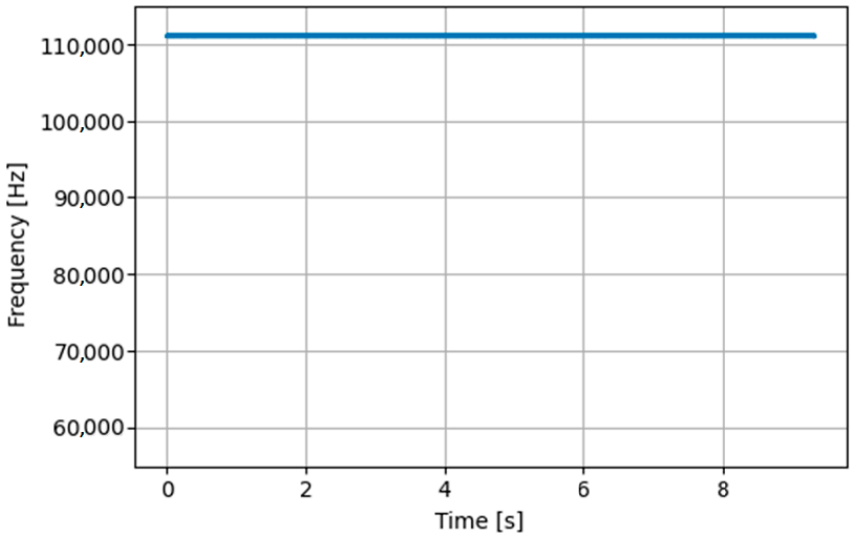

Figure 12. Measurement of f_{xi} = 111 kHz.

Figure 13 shows the effect of processing the 112 kHz frequency. It can be seen that there is a single frequency measurement with the value at half the set point range. In this case, there was also a problem with detecting the boundary between successive periods of the frequency signal.

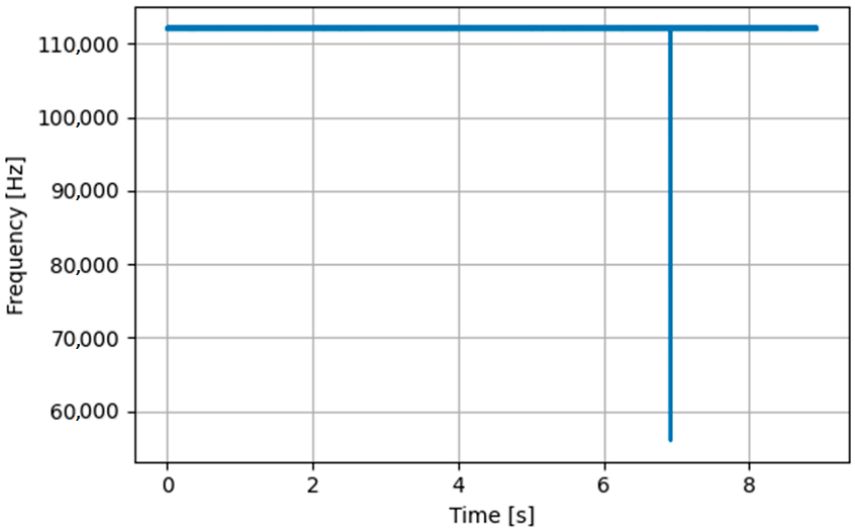

Figure 13. Measurement of f_{xi} = 112 kHz.

Figure 14 shows the effect of processing the frequency of 113 kHz. It can be seen that the measurement problem occurred for ten T_{xi} periods.

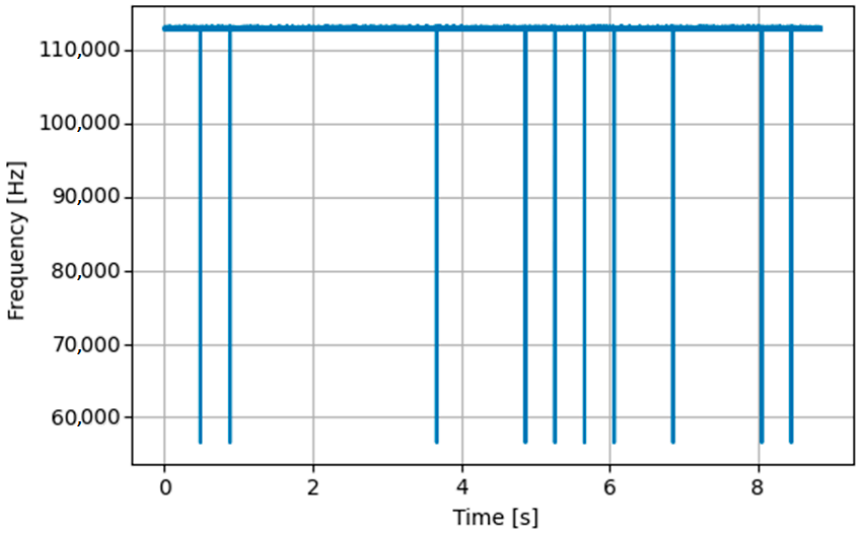

Figure 14. Measurement of f_{xi} = 113 kHz.

When converting the frequencies into numerical values, each subsequent measurement of the period is treated as a single measurement, and each incorrect reading of T_{xi} will have a significant impact on the presentation of the final result. To minimize incorrect reproduction of the graph of frequency changes and, consequently, the processed physical quantity, a decision was made to consider the frequency of 111 kHz as the upper limit of the measurement range.

The total error graphs of the developed model of the f/N converter are shown in Figure 15. The graph of the theoretical error is marked in red (10), while that of the error obtained from the experiment is marked in blue.

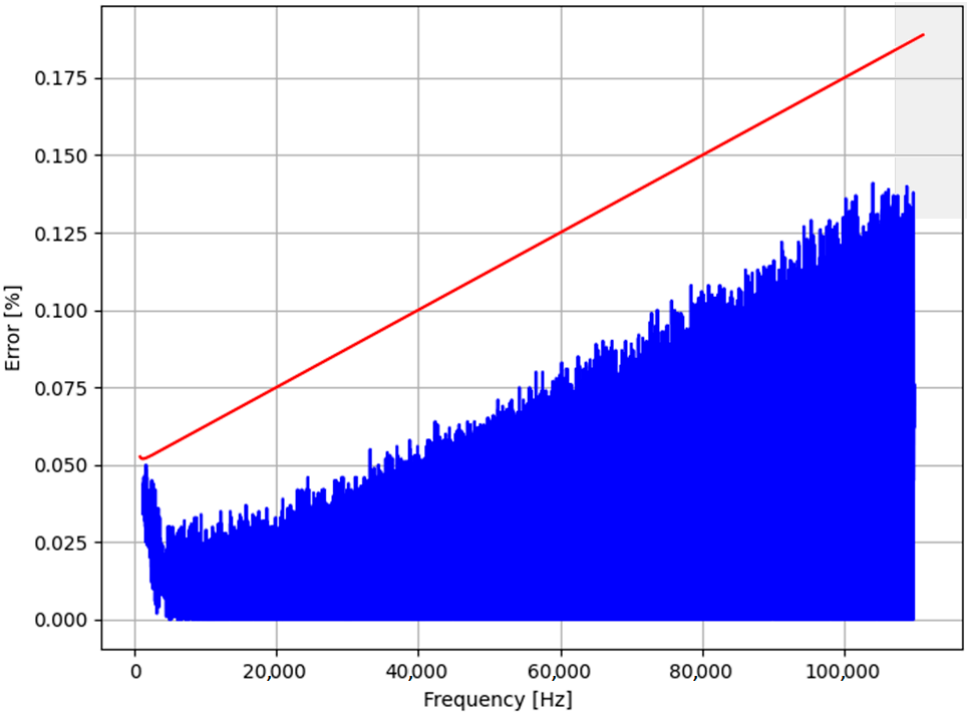

Figure 15. f/N converter error graph for f_g = 80 MHz.

It can be seen that the error recorded in the experiment does not exceed the theoretical value. There is also a significant influence of error averaging in the lower part of the measuring range. In order to determine the switching limit of the f_g frequency division for

adaptive operation, the zoom of the obtained error graph for lower frequencies is shown in Figure 16. It can be seen that between 4 kHz and 5 kHz, there is an irregularity in the graph, after which the error value obtained from the experiment begins to increase noticeably. It was decided that the frequency of 5 kHz, located in the stable part of the graph, would be convenient and allow for stable operation of the f/N converter.

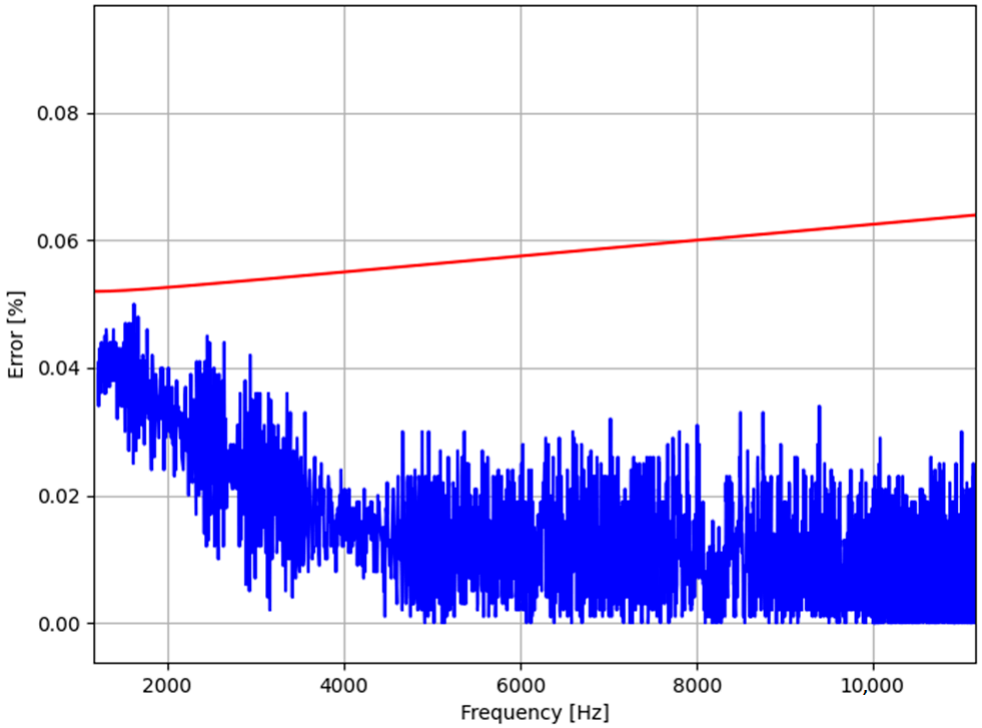

Figure 16. Zoom of the error graph for the lower part of the range.

5. Error Graph of the f/N Converter Model

The next stage of the research was creating an algorithm for the adaptive work of the f/N converter and introducing relevant modifications to the program code.

The f/N converter application should continuously analyze the current length of the T_{xi} period and change the degree of frequency division according to the established requirements if the threshold values are reached.

The details of the adaptive work of the method to change the degree of division of the clock frequency used by the counter are described in [31]. The results of the simulation analysis of this method for various operating conditions are also included there.

It was assumed that in the adaptive mode when reducing the measured frequency f_{xi} below 5 kHz, the frequency f_g would be divided by 8 in the prescaler. As a result, the T3 counter will add up the pulses occurring at a frequency of 10 MHz. The lower limit of the measurement range is 160 Hz, which is the product of the T_g period and the maximum capacity of the meter, rounded off to full tens.

The Increase of f_{xi} above 5 kHz will force the return of the division degree to 1 and set the clock signal for the counter T3 to the frequency of 80 MHz.

The adaptive operating mode changes the shape of the theoretical error graph. For the period T_{xi} with the value 20^{-4} s, corresponding to f_{xi} = 5 kHz, there is a step change in the total error value forced by the change in the quantization error. Figure 17 shows the error graph for the adaptive mode, plotted as a bold red line. For comparison, the waveforms of the theoretical total error graphs for f_g = 10 MHz and f_g = 80 MHz are added. Certainly, the change in the counter clock frequency division does not have to take place only for values close to f_{xi} = 5 kHz. The graph shows that the degree of frequency division can be switched for longer T_{xi} periods, which will further reduce the error. The presented

threshold of change in the f_g division degree should be treated as an example, illustrating the effectiveness of the presented method.

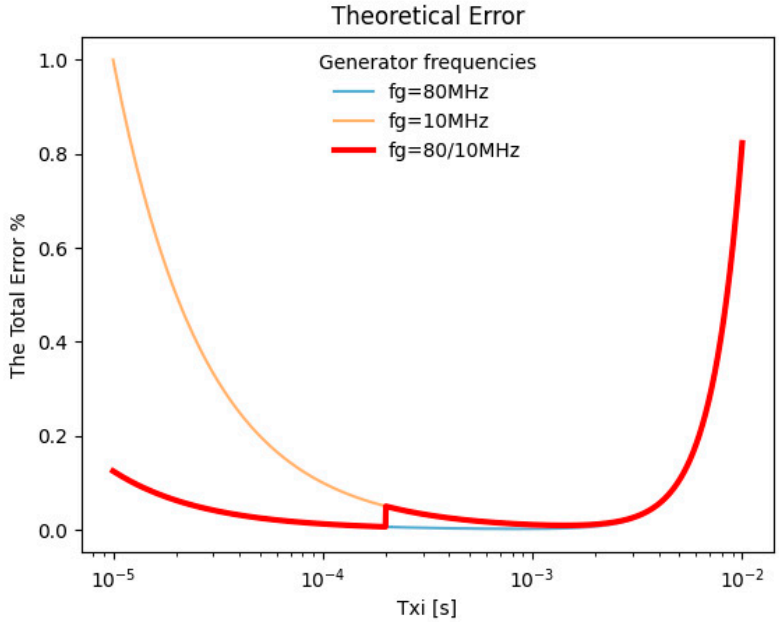

Figure 17. Graph of theoretical error for the f/N converter working in adaptive mode.

The algorithm for the adaptive work of the f/N converter is shown in Figure 18. Part of the functionality is identical to the algorithm presenting the converter's work in the basic mode (Figure 10). The blocks with unchanged functionality have a white filling, while new blocks and blocks with changed functionality are marked with a green filling.

The first modification of the algorithm consists of adding the start of f_g frequency division in the part initializing the counter T3 setting. Initially, the frequency division degree is set to 1, and the divider does not work.

The second modification is the inclusion of blocks that analyze the calculated current value of N_{xi} and, according to the obtained result, change the frequency division degree. When N_{xi} reaches a value of 16,000 or more, the division degree is set to 8. The program iteration number for the time of changing the division degree is also stored in a dedicated table. This allows the actual clock frequency to be decoded for subsequent N_{xi} when analyzing the data at a later time. In addition, in order to maintain subsequent division by 8, the program sets a dedicated memory location—a flag signaling that the division degree is currently set to 8. Thanks to this flag, the division coefficient is not changed until the next N_{xi} decreases below 2000, which corresponds to the frequency of 5 kHz for f_g = 10 MHz. Reducing the value of N_{xi} below 2000 forces the start of the procedure of setting the division degree to 1. Like in the previous case, the number of program iterations at which the division degree has been changed is stored for later use, but this time in the table storing the data about setting the f_g division by 1. In order to block duplicate settings in the f_g division, the division by 8 flags is cleared at the same time.

Depending on the calculated values of N_{xi}, the program changes the division degree in the prescaler on an ongoing basis, adjusting the counter clock frequency to the values set in the algorithm.

The last change introduced in the adaptive work algorithm refers to a different way of generating the final report. In order to be able to calculate T_{xi} from the transmitted N_{xi}, the N_{xi} strings for a given division degree are preceded by a division degree marker. Thanks to this, the software of the master computer, when reading subsequent data from the report, is able to calculate the duration of subsequent T_{xi} periods on an ongoing basis.

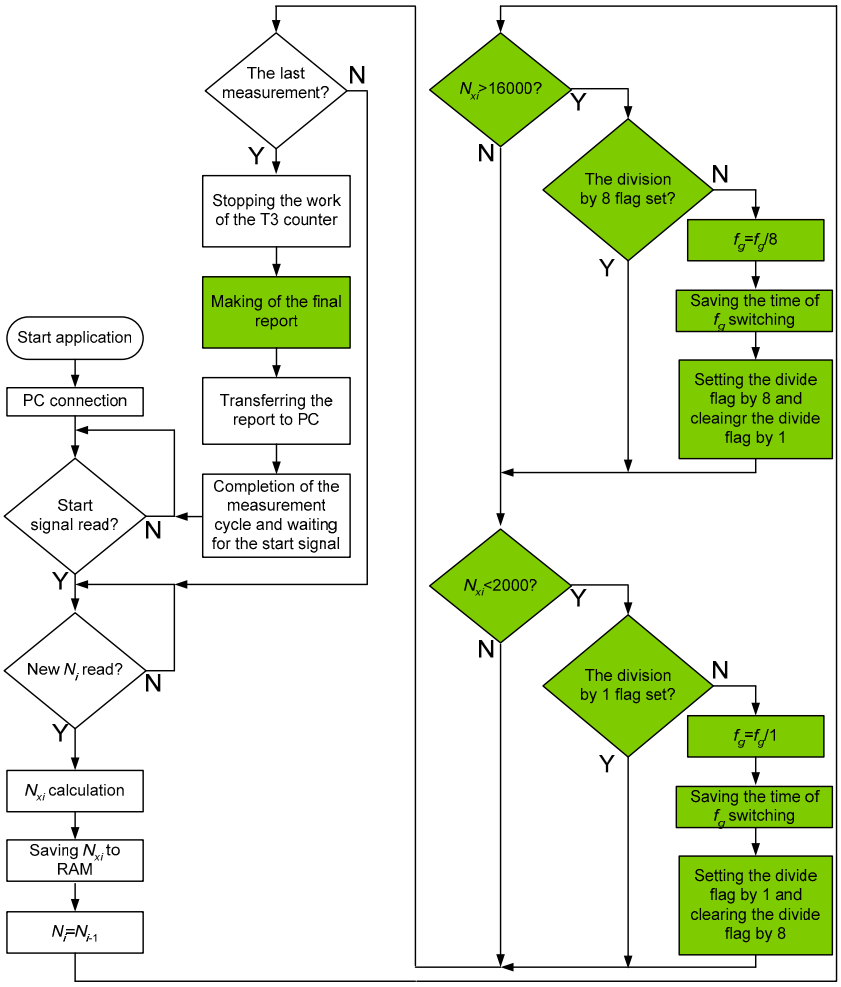

Figure 18. Algorithm of adaptive work of the f/N converter.

6. Verification of the Adaptive Work of the f/N Converter

The tests of adaptive operation of the converter consisted of checking how the converter works for frequencies in the lower part of the measurement range, the switching range in particular, by analyzing the increase in total error caused by the averaging error. It was assumed that the applied test signal is calculated based on the following relationship:

$$f_t = f_0 + f_m \sin(2\pi F t). \tag{12}$$

The following parameters were set: DC component f_0 = 5.160 kHz, amplitude f_m = 5 kHz, and frequency F = 1 Hz. For these conditions, it was possible to determine the error graph in the range of 160 Hz ÷ 10,160 Hz. The recorded variable frequency waveform is shown in Figure 19.

The analysis of the error graph for the entire recorded waveform would result in multiple plottings of the error curve on one graph, thus making the graphical presentation illegible. For this reason, it was assumed that the graph would show a data sequence representing one frequency change from the minimum to the maximum of the given test waveform f_t. The magnification of this waveform is shown in Figure 20. It can be seen that the division degree change generates a jump in the calculated f_{xi}. An incorrect value of f_{xi} is read when the procedure sets the new division degree value in the counter and reinitializes the counter after changing the setting.

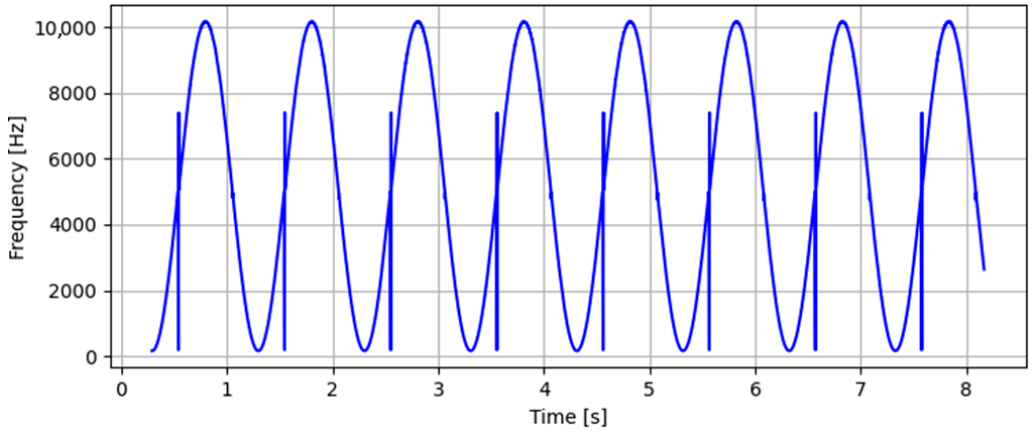

Figure 19. Result of recording the test signal after starting the adaptive mode.

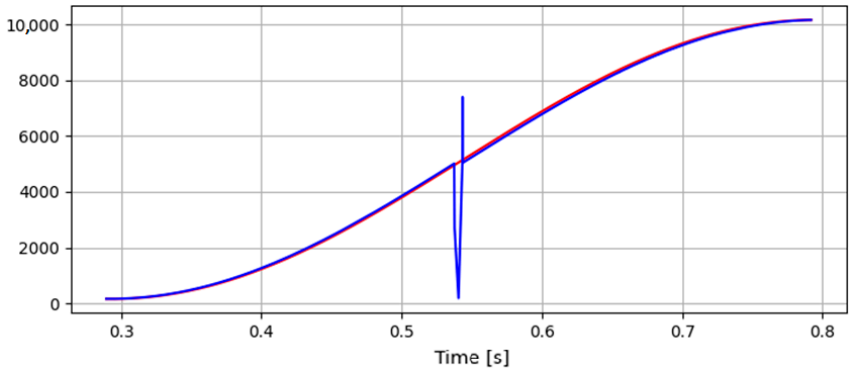

Figure 20. Graph of measurement results in which the process of adding clock pulses to the counter has been disturbed.

The presented magnification shows that for a threshold frequency close to 5 kHz, the reproduced waveform (blue) deviates significantly from the test waveform (red), with the difference between these waveforms reaching a value close to the amplitude f_m. Taking into account that the change of f_{xi} differs significantly from the set test waveform, it was concluded that an approximation should be used to reconstruct the waveform in the graph part covering the switching time of the counter's clock frequency division degree.

The first approximation used was extrapolation with a zero-degree polynomial replacing the incorrectly determined values with the last correct one. Figure 21 shows the error graph reconstructed in the above way. It can be seen that the theoretical error graph is consistent with that obtained from the experiment. The effect of reducing the processing error to a value of about 0.27% has been obtained.

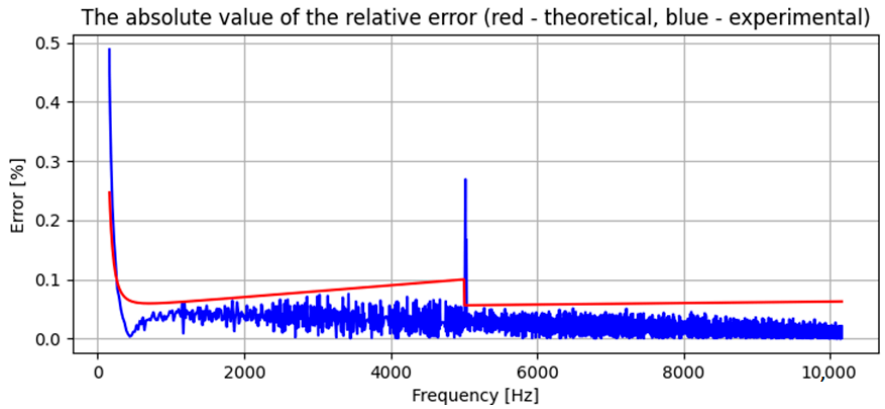

Figure 21. The error graph after zero-degree polynomial extrapolation.

Due to the rather large error value of the approximation used, it was decided to additionally test the extrapolation with a first-degree polynomial and the interpolation with zero and first-degree polynomials. It is obvious that the tested approximations caused differences in the experimentally obtained error graphs only in the switching range.

A decision was made that, in order to make the approximation effects comparable, a summary of the error graphs for all the approximations used will be presented in an enlarged form showing only the frequencies near 5 kHz, i.e., in the range in which the T3 clock frequency division degree was switched. This summary of graphs is shown in Figure 22. It can be seen that the best approximation of the test signal change trend is provided by linear interpolation.

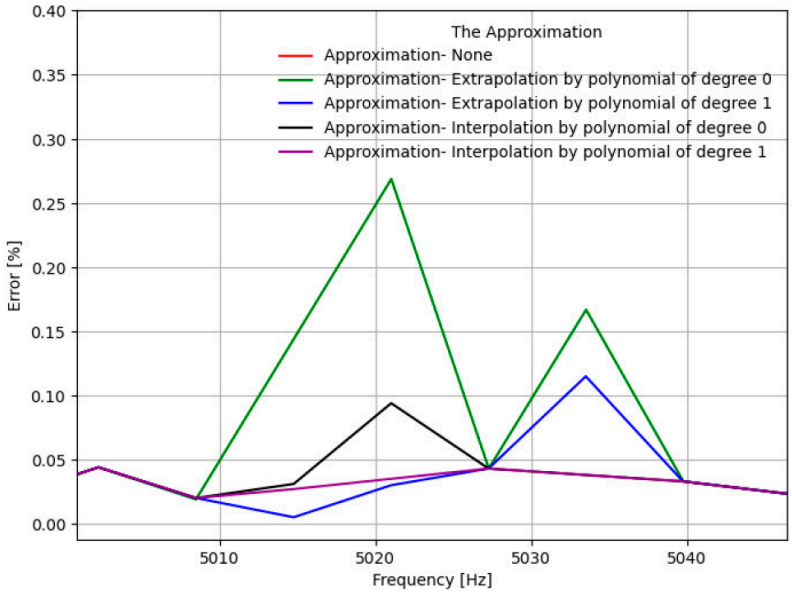

Figure 22. Enlarged error graphs for the approximations used in the range of T3 counter clock frequency switching.

Figure 23 shows the examined waveform after applying the first-degree polynomial interpolation. The applied approximation method caused the waveform to be undistorted in the regions of frequency division degree in the prescaler and to well correspond to the given test signal.

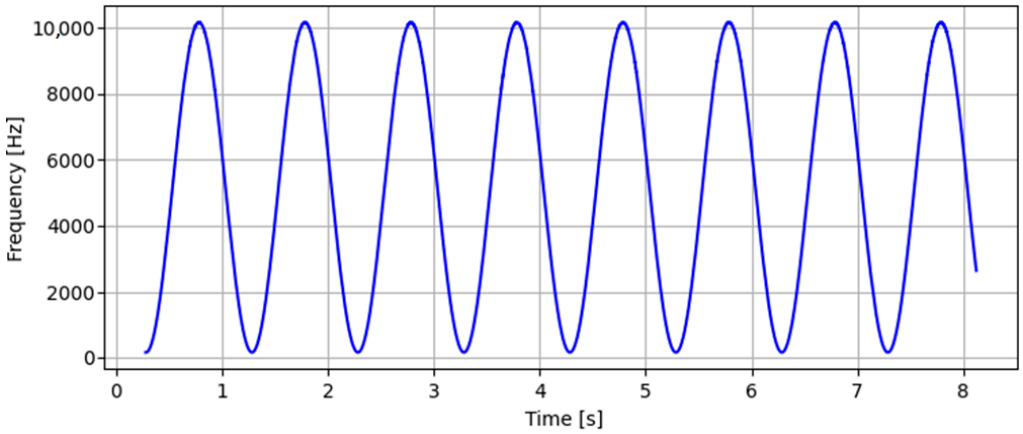

Figure 23. Signal recorded after first-degree polynomial interpolation.

7. Conclusions

A number of challenges had to be met when implementing an adaptive method for changing the frequency division of the counter clock signal in a frequency-to-code

converter. The first was the selection of a microcontroller to implement the frequency-to-code converter. Due to the limitations of the factory-applied RC clock signal in the microcontroller, it was necessary to select and test a more stable signal source. The next challenge was to determine a method to check the upper limit of the measurement range. The main and most time-consuming challenge was to implement the basic and adaptive algorithms in the microcontroller structure. An additional challenge, not discussed in the article, was the development of software in Python to analyze the data and create final reports on each measurement. The measurement experiments conducted allow us to conclude that it is possible to implement the f/N converter structure in the STM32L476RG microcontroller. The obtained results confirm the compliance of the metrological analysis of the f/N converter model with the experimentally obtained error graph.

The efficiency of the microcontroller used allowed us to modify the operation of the f/N converter and improve its operating parameters. The design of the frequency-to-code converter developed in an earlier work [33] using an 8-bit microcontroller allowed error-free processing of successive periods of a waveform with a maximum frequency of 10.25 kHz. As shown in the paper, the device using a 32-bit microcontroller allowed the upper range of the measured frequencies to reach 111kHz. The above result proves the desirability of using microcontrollers with higher computing power in cases where processing of successive periods of the signal over a wider range is needed or when the computing power is used for additional data processing in the microcontroller. The implementation of an adaptive algorithm that allows for the extension of the lower limit of the f/N converter measurement range without requiring the use of a counter with increased capacity is presented.

This limit can be easily extended by selecting the clock frequency division degree of the meter to the value required in the measurements. The microcontroller used in the research allowed for the effective selection of the division degree of the meter's clock frequency to the required extent. If frequencies in other ranges need to be processed, the f/N converter system allows the user to divide the frequency within a very wide range.

When using a software change of the counter clock frequency division degree, one should take into account that during the division degree change, the meter's operation is disturbed and, as a result, a small number of incorrect measurement results are generated. In this case, good interference filtering effects are obtained using linear interpolation.

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Data Availability Statement: The data presented in this study is available on request from the corresponding author. The data is stored in a custom format implemented in the software. Some of the data was stored only temporarily in computer memory while Python was processing it. If necessary, it is possible to repeat the calculations presented and generate a summary containing the necessary information.

Conflicts of Interest: The authors declare no conflict of interest.

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