Hybridized PWM Strategy for Three- and Multiphase Three-Level NPC Inverters

Arkadiusz Lewicki, Dmytro Kondratenko, and Charles I. Odeh

***Abstract*—A simple hybridized pulsewidth modulation (PWM) algorithm for three- and multiphase three-level neutral point clamped (NPC) inverters is proposed. The proposed solution is based on classical space vector PWM (SVPWM) algorithms for two-level inverters but can also be based on sinusoidal PWM with min–max injection. An additional level of output voltage is obtained by modifying the resulting switching patterns taking into account the actual dc-link voltages. In the case of SVPWM algorithms, such an approach eliminates the need to find the subsector where the reference voltage vector is located. It is also not necessary to analyze the changes in the position and length of active vectors in the case of dc-link voltage imbalance. DC-link voltage balancing is achieved by modifying the switching pattern, taking into account the values and direction of phase currents and actual dc-link voltages. Also, the algorithm optimizes the switching pattern and eliminates unnecessary switching instances. The proposed approach utilizes both space vector analysis and independent control of individual inverter-legs. The latter is peculiar to carrier-based PWM; hence, the proposed solution is termed hybridized PWM. Presented experimental tests and results validated the proposed control concept and algorithm for three- and multiphase NPC inverters.**

***Index Terms*—DC-link voltage balancing, sinusoidal pulsewidth modulation (SPWM), space vector pulsewidth modulation (SVPWM), three-level NPC inverter.**

I. Introduction

THE properties of multilevel inverters make them interesting alternatives for two-level voltage source inverters (VSIs). Among multilevel inverter configurations, the most popular is the three-level diode-clamped neutral point clamped (NPC) inverter. This topology has been in existence since the early 1980s [1]. Compared to two-level VSIs, its output voltage can be greater than the blocking voltage of the constituting power switches; the shape of its output voltage is closer to sinusoid; and the rate of voltage change (*du/dt*) is smaller. In the medium-voltage range, they can be a better replacement for classic two-level inverters [2]. For an obvious reason of low-cost power switches with low blocking voltage rating, they can be used also in low-voltage applications. The popularity of NPC inverters is evidenced by the presence of similar topologies: T-type [3], [4], [5]; F-type [6]; active NPC (ANPC) [7], and T-type ANPC [8] inverters.

Due to the diverse deployment of NPC inverters in various applications, their modulation/control algorithms have attained research maturity that allows them to be categorized. The modulation algorithms can basically be classified as: multicarrier-based sinusoidal pulse width modulation (SPWM) [9], [10]; selective harmonic elimination PWM (SHEPWM) [11], [12], [13]; and space vector pulsewidth modulation (SVPWM) [14], [15]. SVPWM and SPWM are the most popular modulation schemes for NPC [16], [17], [18], [19], [20]. The SVPWM algorithms are, however, more often utilized in multilevel inverters with a smaller number of levels (such as three-level inverters). As the number of levels increases, the SPWM algorithms are more likely used to control the inverter switches [10], [19], [21]. This is due to the difficulties in identifying the sectors and subsectors where the reference voltage vector is located in SVPWM [15], especially in the case of unbalanced dc-link voltages. Some of the SVPWM algorithms are dedicated to the correct generation of the output voltage in the case of unbalanced voltages [14].

DC-link voltage balancing methods in three-phase NPC inverters depend on the utilized modulation algorithms. The SHEPWM algorithms compute the switches' triggering instants to generate the output voltage with a desired harmonic content [11], [12], [13]. Such control methods are best suited for the steady-state operation of the inverter. Based on the load currents, the switching instants can also be computed to control the neutral-point potential of the dc link [22]. The angle computations of SHEPWM algorithms are determined based on the steady-state status and, thus, require knowledge of the load to determine the effects of the load currents on the dc-link voltages.

SVPWM algorithms are based on the combination of active vectors [14]. The dc-link voltages are controlled by activating the vectors that connect the load currents to the neutral point of dc-link capacitors. A similar effect can be obtained with the use of virtual vectors, which, in practice, are created by active vectors

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with appropriate durations [23]. While the SVPWM control approaches ensure full dc-link voltage utilization and minimum harmonic content in the generated voltage waveform, the dc-link voltage balancing possibilities are restricted. The active vectors that can be used for balancing are assigned to the sectors where the output voltage vector is located [14]. This means that the balancing vectors must be predefined; and, in practice, the active vectors other than those assigned to the sectors are not utilized. Other solutions use discontinuous PWM methods to balance the dc-link capacitors [24]. This, in practice, allows to change the time of connecting the load current to the neutral point of the dc-link capacitor bank.

Control algorithms in SPWM are usually based on: introduction of the appropriate value of zero-sequence component to the reference voltage [25], [26]; forcing commutation between multiple voltage levels by modifying the modulating signal [27]; or adjusting the duty cycles in the phases operating in the multistep (MS) switching mode [28], [29]. Some of the solutions combine these methods: the common mode voltage reference is introduced to ensure an appropriate value of dc-link neutral point current; and the duty cycle in the phases operating in the MS switching mode is modified for further control of the dc-link current [9]. The limitation of these methods is related to relatively complicated algorithms. These methods necessitate the determination of the changes in the neutral point current given by the common mode voltage (to find the most appropriate value of common mode voltage with regard to dc-link voltage balancing). In turn, their great advantage is the ease of implementation in inverters with any number of phases [20], [25] compared to SVPWM methods.

Multiphase drives are recently becoming more and more popular. A single multiphase motor with quasi-rectangular rotor field distribution can operate with enhanced electromagnetic torque due to the use of higher current harmonics [30], [31]. A single multiphase VSI can be used to independently control several multiphase motors with sinusoidal rotor field distribution and phase transposition [32]. Such an application requires generating several output voltage vectors with independent rotating frequencies, positions, and lengths.

Classical approaches to SVPWM algorithms (usually used in three-phase inverters) require the determination of the sector where the reference voltage vector is located. The vector durations are determined for the active vectors surrounding this sector. The dc-link voltage can be optimally utilized if the vectors are well chosen (if they surround the sector).

In the case of multiphase inverters and the need to independently generate the reference voltage vectors in many orthogonal coordinate systems, the SVPWM algorithms are significantly complicated. If several reference voltage vectors have to be independently generated in a multiphase inverter, the calculation of the durations for the active vector nearest to the reference voltage vectors can deliver values greater than the switching period or even negative. This is because, in a multiphase VSI, all the active vectors in all the orthogonal spaces depend on one another.

Most proposed SVPWM solutions give the possibility of generating a reference voltage vector in only one coordinate system or many reference voltage vectors with a mutually dependent location. This enables the control of a single multiphase motor [33]. However, in drive systems where a single inverter controls a few motors independently, the reference voltage vectors should be generated independently [32], [34]. Consequently, the SPWM modulation schemes are usually used in such systems as simpler and less cumbersome control solutions [20].

In the case of three-level multiphase NPC inverters, the synthesis of space vectors requires the analysis of a large number of active vectors defined simultaneously in many orthogonal systems [35]. At the same time, the position and length of these vectors depend on the dc-link voltage asymmetry. Due to this, the direct or predictive torque control algorithms [36], [37] or SPWM control methods are often utilized [20].

Herein, a simple PWM algorithm for a three- and multiphase three-level NPC inverter with dc-link voltage balancing ability is proposed. In the case of three-level, three-phase NPC inverters, the proposed solution is based on the well-known SVPWM approach for three-phase two-level VSIs. In the case of multiphase, three-level NPC inverters, the proposed solution utilizes the SVPWM algorithm for multiphase two-level inverters proposed in [34]. Since the introduction of SPWM algorithms with min-max injection, the differences between the effects of SPWM and SVPWM have practically disappeared. This means that the proposed solution can also be based on SPWM with min–max injection.

While the durations of active and zero vectors are determined using SVPWM or SPWM methods, balancing the dc-link voltages is achieved by modifying the time of connecting the load current to the neutral point of the dc-link capacitors. In the last step of the algorithm, the obtained switching pattern is optimized to eliminate unnecessary switch transitions. For the fact that the algorithm is partly based on the SVPWM and partly uses the duty cycle control in each of the phases separately (as in SPWM methods), the control approach is termed hybridized PWM. In the following subsequent sections, analyses, experimental tests, and results carried out on both three- and five-phase three-level NPC inverters are presented.

II. SVPWM Algorithm

A. SVPWM Algorithm for Two-Level VSIs

The main difference between a three-level and a two-level inverter topologies is the ability of using additional output voltage potential (the neutral point of the dc link). The three-level inverter can work as a two-level inverter if, in Fig. 1, both upper (S_{x1} and S_{x2}) or both lower switches (S_{x3} and S_{x4}) are activated simultaneously in individual phases. It is worth noting that the switching actions are complementary

$$S_{x3} = !S_{x1};\ S_{x4} = !S_{x2} \tag{1}$$

where $S_{x1\ldots4}$ are the gate signals for the switches in the "x" phase ($x = a \ldots n$). The ON and OFF statuses of the switches are denoted with the numerals 1 and 0, respectively.

Active vectors in the three-phase, three-level NPC inverter form a regular hexagon, even in the case of dc voltage imbalance (see Fig. 2). In such cases, only the long active vectors (obtained

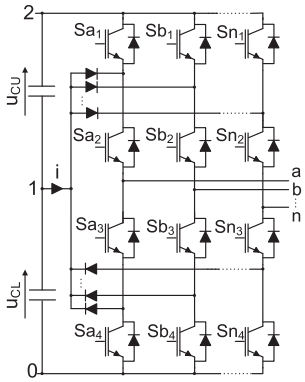

Fig. 1. *n*-phase three-level NPC inverter.

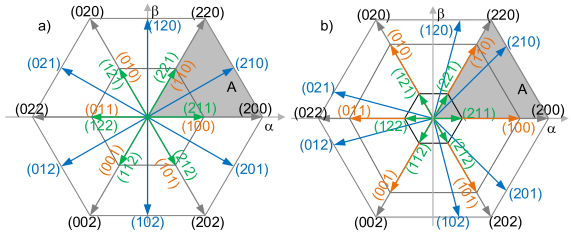

Fig. 2. SVD of a three-level, three-phase VSI. (a) $u_{CU}/u_{CL} = 1/1$. (b) $u_{Cu}/u_{CL} = 0.3/0.7$. A—one of the SVD sectors, and "012" are the output voltage potentials (see Fig. 1) in phases "a," "b," and "c."

for two-level operation) do not change their length and position. The position and length of medium active vectors (120, 021, 012, …) or only the length of short active vectors (221, 110, 211, ….) (see Fig. 2) depend on the dc-link voltage imbalance. In the case of multiphase three-level NPC inverters, the number of available active vectors is greater and only the long active vectors (obtained for two-level operation) do not change their length and position. Similar to the three-phase VSIs, the parameters of medium and short active vectors depend on the dc-link voltage imbalance. The active vectors are simultaneously located in many orthogonal systems that generate additional problems in the implementation of SVPWM algorithms.

Classical SVPWM methods require indicating the sector and subsector in a space vector diagram (SVD), where the end of the reference voltage vector is located (see Fig. 2). In three-phase inverters, the active vectors adjacent to a given sector/subsector are selected to generate the output voltage. It should be noted that in the case of dc-link voltages imbalance, the shape of the sectors remains unchanged (long vectors do not change their position and length) while the shape of the subsectors is changing (see Fig. 2). Simplification of the SVPWM algorithm can, therefore, be obtained by synthesizing only the long active vectors, while the remaining vectors (short and/or medium) will be introduced by modifying the resulting switching pattern. In Fig. 2, for the reference voltage vector located in sector A, the duration of the long active vector (200) and (220) can be determined as

$$t_{(1)(200)} = T_{\text{sw}} \frac{u_{o\alpha} \cdot V_{\beta(220)} - u_{o\beta} \cdot V_{\alpha(220)}}{V_{\alpha(200)} \cdot V_{\beta(220)} - V_{\beta(200)} \cdot V_{\alpha(220)}}$$

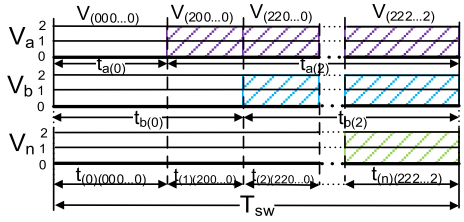

Fig. 3. Switching pattern of the three-level NPC inverter working in a two-level mode; $V_a, \ldots, V_n$—output voltage potentials (see Fig. 1).

$$t_{(2)(220)} = T_{\text{sw}} \frac{-u_{o\alpha} \cdot V_{\beta(200)} + u_{o\beta} \cdot V_{\alpha(200)}}{V_{\alpha(200)} \cdot V_{\beta(220)} - V_{\beta(200)} \cdot V_{\alpha(220)}} \tag{2}$$

where $u_{o\alpha}$, $u_{o\beta}$ are the components of reference voltage vector, $V_{\alpha(220)}$, $V_{\beta(220)}$, $V_{\alpha(200)}$, $V_{\beta(200)}$ are the components of active long vectors surrounding sector A (see Fig. 2), T_{sw} is a switching period represented by $1/(2{\cdot}f_{\text{sw}})$ in symmetrical PWM, f_{sw} is the switching frequency, and $t_{(1)(200)}$, $t_{(2)(220)}$ are the active vector durations.

The duration of zero vectors (000) and (222) is determined as

$$t_{(0)(000)} = t_{(3)(222)} = 0.5 \cdot \left(T_{\text{sw}} - t_{(1)(200)} - t_{(2)(220)}\right). \tag{3}$$

Assuming that the zero vectors are located at the beginning and at the end of the switching pattern, the activation times for the pair of upper transistors in individual inverter phases "*a*" …"*c*" can be determined as (see Fig. 3)

$$t_{a(2)} = \sum_{i=0}^{3} a_i \cdot t_{(i)(abc)}; \quad \ldots; \quad t_{c(2)} = \sum_{i=0}^{3} c_i \cdot t_{(i)(abc)} \tag{4}$$

where

$$\begin{aligned} &a_i = 1 \Leftrightarrow t_{(i)(abc)} = t_{(2xx)}, \quad \text{else} \quad a_i = 0 \\ &\ldots \\ &c_i = 1 \Leftrightarrow t_{(i)(abc)} = t_{(xx2)}, \quad \text{else} \quad c_i = 0 \end{aligned} \tag{5}$$

and "*x*" – takes the value "2" or "0". Index 2 denotes the activation time of the potential "2" (see Fig. 1) in the VSI phases.

The determined time values can be directly used to generate the gate signals for inverter switches.

Similar results in the form of gate signal durations for a two-level multiphase VSI can be obtained using the SVPWM proposed in [34]. The duration of the "2" potential pulses [activated two upper transistors Sx_1 and Sx_2, $(x = a, \ldots, n)$] in particular inverter phases is equal to (see Fig. 3)

$$t_{a(2)} = \sum_{i=0}^{n} a_i \cdot t_{(i)(abc\ldots n)}, \ \ldots \ , t_{n(2)} = \sum_{i=0}^{n} n_i \cdot t_{(i)(abc\ldots n)} \tag{6}$$

where

$$\begin{aligned} &a_i = 1 \Leftrightarrow t_{(i)(abc\ldots n)} = t_{(2xx\ldots x)}, \quad \text{else} \quad a_i = 0 \\ &\ldots \\ &n_i = 1 \Leftrightarrow t_{(i)(abc\ldots n)} = t_{(xxx\ldots 2)}, \quad \text{else} \quad n_i = 0 \end{aligned} \tag{7}$$

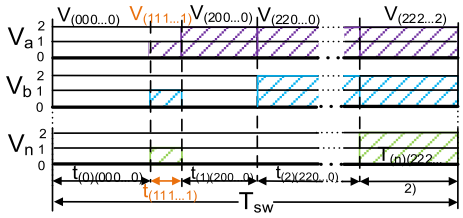

Fig. 4. Switching pattern of the three-level NPC inverter with (111) zero vector.

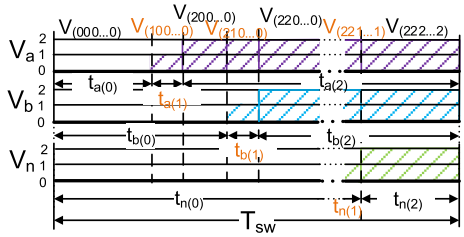

Fig. 5. Switching pattern of the three-level NPC inverter working in three-level mode after shifting the pulses of the (111) zero vector.

and "x" can be "0" or "2," and $t_{(i)(abc....n)}$ represents the duration of zero and active vectors.

The duration of the "0" potential pulses (activated two lower transistors) in particular inverter phases (see Fig. 1) can be determined as

$$t_{a(0)} = T_{\text{sw}} - t_{a(2)},\ \ldots\ , t_{n(0)} = T_{\text{sw}} - t_{n(2)}. \tag{8}$$

In the case of two-level modulation, the upper and lower switches are activated in pairs: $S_{x1} = S_{x2}$ and $S_{x3} = S_{x4}$ (see Fig. 1).

B. SVPWM Algorithm for Three-Level VSIs

The switching pattern shown in Fig. 3 is for two-level operation. It is necessary to introduce an additional voltage level—the potential of the neutral point of dc-link capacitors ("1" in Fig. 1). This can be achieved by introducing an additional zero vector with the duration $t_{(111\ldots1)}$ into the switching pattern. Its duration can be any but not more than a sum of durations of existing zero vectors

$$0 \le t_{(111\ldots1)} \le t_{(0)(000\ldots0)} + t_{(n)(222\ldots2)} \tag{9}$$

where the duration of zero vectors $V_{(000\ldots0)}$ and $V_{(222\ldots2)}$ is identical (3).

The resulting switching pattern for the multiphase NPC VSI will take the form shown in Fig. 4. The zero vector $V_{(111\ldots1)}$ will partially replace two zero vectors $V_{(222\ldots2)}$ and $V_{(111\ldots1)}$. Due to further modifications of the switching sequence, it is convenient to adopt the duration of an additional zero vector closer to the lower limit of the range in (9).

Introducing an additional zero vector $V_{(111\ldots1)}$ (see Fig. 4) will cause additional switching operations into the switching pattern. However, it is possible to shift individual pulses with the potential "1" to reduce the number of additional switching operations. Because the duration of these pulses is the same in each inverter phase and equal to the zero vector duration $t_{(111\ldots1)}$

$$t_{a(1)} = t_{b(1)} = \ldots = t_{n(1)} = t_{(111\ldots1)} \tag{10}$$

such an operation does not change the average value of the output voltage. The above operation requires the recalculation of the duration of the potentials "0" and "2"

$$\begin{aligned} t_{a(2)} &= t_{a(2)} - t_{a(1)} \cdot 0.5, \quad \ldots\ , \quad t_{n(2)} = t_{n(2)} - t_{n(1)} \cdot 0.5 \\ t_{a(0)} &= t_{a(0)} - t_{a(1)} \cdot 0.5, \quad \ldots\ , \quad t_{n(0)} = t_{n(0)} - t_{n(1)} \cdot 0.5. \end{aligned} \tag{11}$$

As a result, the additional active vectors $V_{(100\ldots0)}$, $V_{(210\ldots0)}$ .... $V_{(222\ldots1)}$ are obtained (see Fig. 5). It is worth noting that each of them connects the inverter load current to the neutral point of the dc-link capacitors. Since the durations of "1" pulses: $t_{a(1)} \ldots t_{n(1)}$ are the same, it does not affect the balancing the dc-link voltages. Changing the durations of these pulses allows the control of the neutral-point potential.

C. Balancing the DC-Link Voltages

The neutral point current affects the voltages on both dc-link capacitors (see Fig. 1)

$$u_{CU}(t) = \frac{1}{C}\int_0^t \left(\frac{i(\tau)}{2}\right) d\tau, \quad -u_{CL}(t) = \frac{1}{C}\int_0^t \left(\frac{i(\tau)}{2}\right) d\tau \tag{12}$$

hence, the difference between the voltages of the upper and lower capacitors is

$$\Delta u = u_{CU}(t) - u_{CL}(t) = \frac{1}{C}\int_0^t (i(\tau))\, d\tau \tag{13}$$

where "i" is a dc-link neutral-point current (see Fig. 1).

The coefficient q_{act} specifies an actual voltage imbalance on the dc-link capacitors and can be determined from (13) as

$$q_{\text{act}} = i \cdot t = C \cdot \Delta u \tag{14}$$

where "t" is the time to balance the voltages in dc link when the neutral point current is equal to "i." This current is supplied to the neutral point of the dc link by the individual inverter phases.

During the balancing process, the time of connecting the "0" and "2" potentials to the inverter terminals (see Fig. 1) is shortened, while the time of connecting the "1" potential is increased. Since the average value of the phase voltage cannot be changed, it is necessary to determine the range of these changes for each phase separately. The durations of "2" and "0" potentials can be reduced maximally by

$$\begin{aligned} &\text{if } \left(t_{x(2)} \cdot u_{CU} < t_{x(0)} \cdot u_{CL}\right) \Rightarrow t_{x(\max)} = t_{x(2)} \text{ or} \\ &\text{if } \left(t_{x(0)} \cdot u_{CL} < t_{x(2)} \cdot u_{CU}\right) \Rightarrow t_{x(\max)} = t_{x(0)} \end{aligned} \tag{15}$$

where $t_{x(2)}$ and $t_{x(0)}$ are the times of generating the "2" and "0" potentials in phase "x"($x = a, b, \ldots n$) (see Fig. 5) (11).

Because the durations of the potentials "2" and "0" are shortened at the same time, the charge "q" that can be supplied from individual inverter phases to the dc-link neutral point to

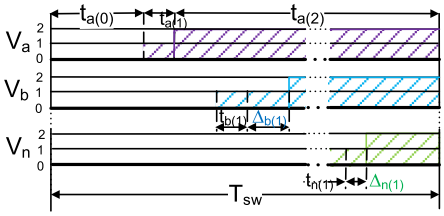

Fig. 6. Resulting switching pattern for $i_a<0$, $i_b>0$, $i_c>0$ and $u_{CU}<u_{CL}$ ($\Delta_{1(a)}=0$).

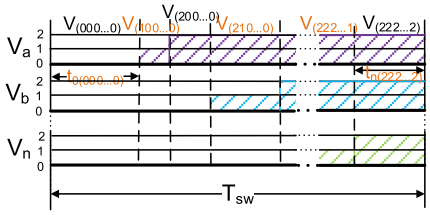

Fig. 7. Resulting sequence of active and zero vectors.

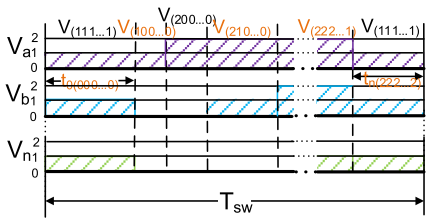

Fig. 8. Switching pattern with replaced zero vectors.

counteract the dc-link voltage imbalance is equal to

$$q_{x(\max)} = 2 \cdot t_{x(\max)} \cdot i_x \tag{16}$$

taking into account the condition

$$\text{if } \left(\operatorname{sgn}\left(q_{x(\max)}\right) \neq \operatorname{sgn}\left(q_{\text{act}}\right)\right) \Rightarrow q_{x(\max)} = 0 \tag{17}$$

where sgn() is sign (+ or −), and x is VSI phase ($x = a, b, \ldots .n$).

Equation (17) prevents further increase in dc-link voltage imbalance.

The maximum charge that can be delivered to the dc-link neutral point can be determined as

$$q_{\text{all}(\max)(\text{all})} = \sum_{x=a}^{n} q_{x(\max)} \tag{18}$$

where "x" is an inverter phase, and n is the number of VSI phases.

The dc-link voltages can be balanced with the use of the charge supplied from individual inverter phases in any proportion. The solution proposed here uses the charge provided by individual phases according to the relation

$$q_{x(\text{bal})} = q_{x(\max)} \cdot \frac{q_{\text{act}}}{q_{\text{all}(\max)}}, \quad x = a, b, \ldots, n. \tag{19}$$

When a small charge is needed to balance the dc-link voltages $0 \leq \text{abs}(q_{\text{act}}) \leq \text{abs}(q_{\text{all}(\max)})$, they will be balanced in the current switching period T_{sw}; otherwise, it will take more than a single switching period using the maximum available charge (18).

In order to balance the dc-link voltages, the duration of "1" pulses in individual VSI phases has to be extended by the value (see Fig. 6)

$$\Delta_{x(1)} = \frac{q_{x(\text{bal})}}{i_x}. \tag{20}$$

While maintaining the unchanging average value of the phase voltages, the durations of the individual potentials (10), (11) must be corrected according to

$$t_{a(2)} = t_{a(2)} - \Delta_{a(1)} \cdot \frac{u_{CL}}{u_{CL}+u_{CU}}, \quad t_{a(1)} = t_{a(1)} + \Delta_{a(1)}$$
$$t_{a(0)} = t_{a(0)} - \Delta_{a(1)} \cdot \frac{u_{CU}}{u_{CL}+u_{CU}}$$
$$..$$
$$t_{n(2)} = t_{n(2)} - \Delta_{n(1)} \cdot \frac{u_{CL}}{u_{CL}+u_{CU}}, \quad t_{n(1)} = t_{n(1)} + \Delta_{n(1)}$$
$$t_{n(0)} = t_{n(0)} - \Delta_{n(1)} \cdot \frac{u_{CU}}{u_{CL}+u_{CU}}. \tag{21}$$

Because of (15), the obtained times $t_{x(0)} \ldots t_{x(2)}$ will not be negative. The resulting switching pattern and utilized active vectors are shown in Fig. 7.

The average output phase voltage [in relation to the neutral dc-link point "1" (see Fig. 1)] will be equal to

$$\frac{1}{T_{\text{sw}}} \left(\begin{array}{l} \left(t_{x(2)} - \Delta_{x(1)} \cdot \frac{u_{CL}}{u_{CL}+u_{CU}}\right) \cdot u_{CU} + \left(t_{x(1)} + \Delta_{x(1)}\right) \cdot 0 \\ - \left(t_{x(0)} - \Delta_{x(1)} \cdot \frac{u_{CU}}{u_{CL}+u_{CU}}\right) \cdot u_{CL} \end{array} \right)$$
$$= \frac{1}{T_{\text{sw}}} \left(t_{x(2)} \cdot u_{CU} - t_{x(0)} \cdot u_{CL}\right). \tag{22}$$

This means that the balancing procedure does not affect the average value of the obtained voltages.

D. Optimization of Switching Pattern

The last step of the algorithm is optional and aims at optimizing the resulting switching pattern by reducing the number of switch commutations. This can be done by replacing the zero vectors $V_{0(000\ldots0)}$ and $V_{n(222\ldots2)}$ with a zero vector $V_{(111\ldots1)}$ (see Fig. 8). The durations of zero vectors $V_{0(000\ldots0)}$ and $V_{n(222\ldots2)}$ are equal to the shortest of $t_{x(0)}$ times and to the shortest of $t_{x(2)}$ times, respectively, where ($x = a, b, \ldots, n$)

$$t_{0(000\ldots0)} = t_{x(0)(\min)} = \min\left(t_{a(0)} \ldots . t_{n(0)}\right)$$
$$t_{n(222\ldots2)} = t_{x(2)(\min)} = \min\left(t_{a(2)} \ldots . t_{n(2)}\right). \tag{23}$$

The switching pattern shown in Fig. 8 can be optimized by grouping the potentials "1," as shown in Fig. 9. This operation does not change the average value of the output voltage.

The durations $t_{a(2)}, \ldots, t_{n(2)}$ and $t_{a(0)}, \ldots, t_{n(0)}$ can be recalculated as

$$t_{a(0)} = t_{a(0)} - t_{0(000\ldots0)}, \ldots, \; t_{n(0)} = t_{n(0)} - t_{0(000\ldots0)}$$
$$t_{a(2)} = t_{a(2)} - t_{n(222\ldots2)}, \ldots, t_{n(2)} = t_{n(2)} - t_{n(222\ldots2)} \tag{24}$$

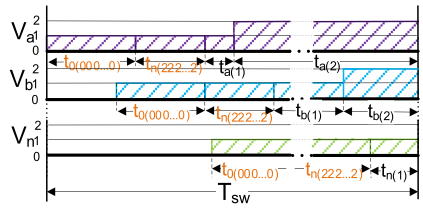

Fig. 9. Optimization of the switching pattern.

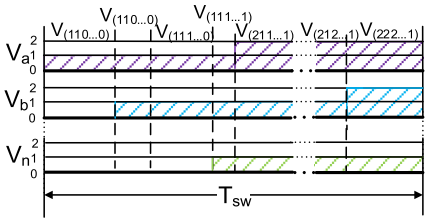

Fig. 10. Optimized sequence of active and zero vectors.

TABLE I
EXPERIMENTAL SETUP SPECIFICATION

Component	Specification
Capacitor banks	2x500μF, 600V
RL load	20Ω, 20mH
Switching frequency	3.3kHz
Fundamental frequency	50Hz
Power switches	AIKW50N60C

while the durations $t_{a(1)} \dots t_{n(1)}$ will be equal to

$$t_{a(1)} = t_{a(1)} + t_{0(000\dots0)} + t_{n(222\dots2)}$$
$$\dots$$
$$t_{n(1)} = t_{n(1)} + t_{0(000\dots0)} + t_{n(222\dots2)}. \quad (25)$$

The resulting switching pattern is shown in Fig. 9, and the sequence of space vectors is shown in Fig. 10. The gate signal durations of the switches' gate signals in Fig. 1 can be determined as

$$t_{Sx1} = t_{x(2)}, \quad t_{Sx2} = t_{Sx3} = t_{x(1)}, \quad t_{Sx4} = t_{x(0)} \quad (26)$$

where $x = (a, b, ..., n)$ is the VSI phase.

The execution steps of the proposed algorithm are presented in Fig. 11.

III. EXPERIMENTAL RESULTS

Experimental tests were carried out using a five-phase 3L-NPC VSI, which can be configured to operate in three-phase and five-phase modes. The laboratory prototype of the inverter is shown in Fig. 12 and the load parameters are given in Table I. The inverter was supplied by an autotransformer. The voltage from it was set in such a way as to place 400 V in the dc link in no-load condition. The effect seen in experimental waveforms (see Fig. 13) is the effect of the autotransformer's inductance: a change in the load results in a slight voltage change.

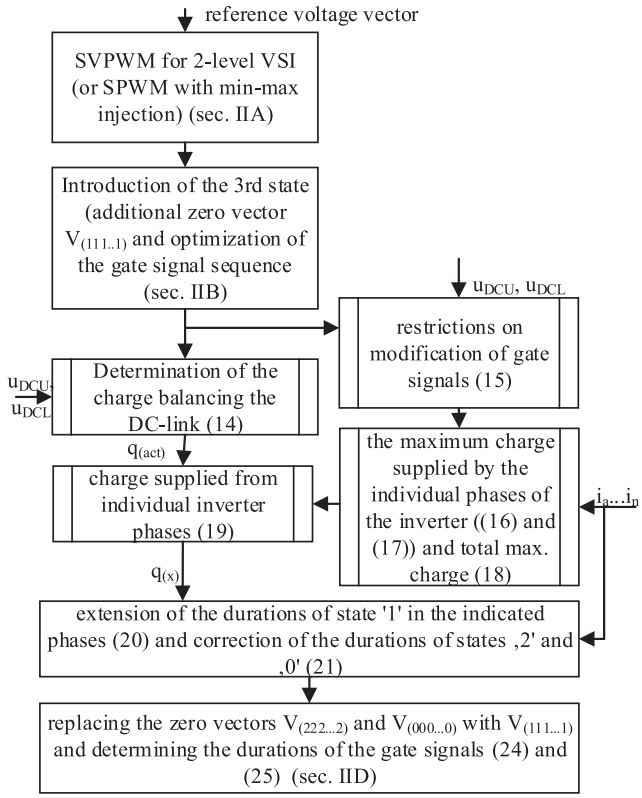

Fig. 11. Flowchart for the proposed modulation and balancing algorithm.

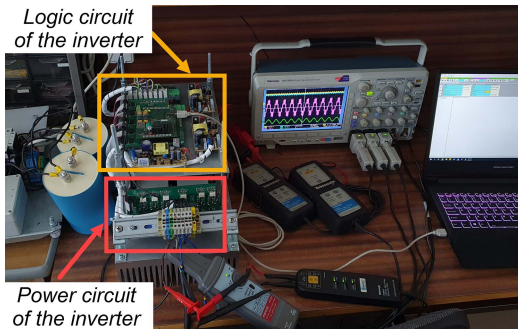

Fig. 12. Laboratory prototype setup of the three-level, five-phase NPC inverter.

For comparison, the proposed modulation strategy and the carrier-based pulse width modulation (CBPWM) method shown in [9] have been implemented in the inverter processor. To validate the effectiveness of the proposed PWM technique, experimental studies were conducted for three-phase (see Figs. 13–21) and five-phase (see Figs. 22–25) modes.

Fig. 13 displays the line-to-line voltage, output current, and dc-link voltages during a step change in the modulation index: from 1 to 0.5 and back to 1 again for both modulation methods. The output voltage waveform is generated correctly for both modulation techniques.

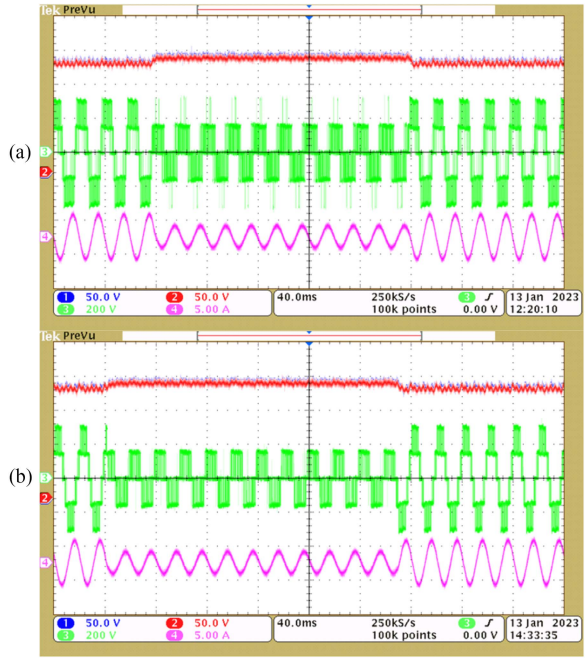

Fig. 13. Three-phase inverter step changes for the modulation indexes from 1 to 0.5 and back to 1. DC-link voltages: 1), 2) 50 V/div; line-to-line voltage: 3) 200 V/div; output current: 4) 5 A/div; time scale: 40 ms/div; output voltage frequency: 50 Hz. (a) Proposed PWM. (b) CBPWM.

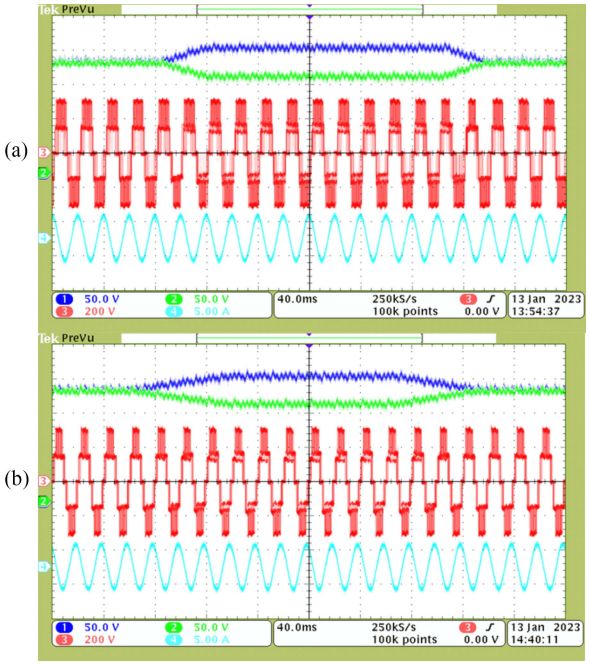

Fig. 14. Balancing algorithm performance for modulation index $m = 1$. DC-link voltages: 1), 2) 50 V/div; line-to-line voltage: 3) 200 V/div; output current: 4) 5 A/div; time scale 40 ms/div; output voltage frequency: 50 Hz. (a) Proposed PWM. (b) CBPWM.

In Fig. 14, for the unity modulation index ($m = 1$), the changes in dc-link capacitor voltages obtained using both modulation methods are compared. In detail, the balancing algorithm performance under different modulation index conditions for proposed and conventional modulation methods is shown in Fig. 15 and compared in Fig. 16. The proposed method is characterized by the shorter time of dc-link voltage equalization over a wide range of modulation index values, except in the interval: $m = 0.4, \ldots, m = 0.7$, where the balancing speeds of both methods are similar.

Fig. 17 presents the waveforms of a phase voltage, line-to-line voltage, and output current, as well as the results of harmonic analysis of line-to-line voltage obtained using the proposed [see Fig. 17(a)] method and CBPWM [see Fig. 17(b)]. For the proposed solution in steady-state operation, additional voltage levels in the output voltage waveforms can be observed. These additional levels are the effect of precise balancing of dc-link voltages. Even a small difference in the dc-link voltages results in a direct duration change of the potential "1" (20). When the dc-link voltages are close to being balanced, a small charge is required to be delivered to the capacitors. Consequently, only small duration changes of "1" potential (20) in the phases with the appropriate current directions are required. This makes the switching patterns contain all the states "0," "1," and "2" (see Fig. 6). In the proposed approach, the balancing charge is divided between all the phases (19) so it affects the changes in the durations of "1" potential. The charge division between phases does not take into account the duration of "2" and "0" pulses of individual legs. As a result, these durations remain different in individual inverter phases.

The final step of the algorithm (see Section II-D) is to optimize the obtained switching patterns. This optimization is based on replacing the zero vectors $V_{0(000\ldots0)}$ and $V_{n(222\ldots2)}$ with the zero vector $V_{0(111\ldots1)}$ and modifying the resulting switching patterns. This results in the elimination of the highest and the lowest voltage levels ("2" and "0") in at least one of the phase voltages. The rest of the phase voltages can be generated using all voltage levels.

In order to show the properties of the proposed method, the ac components of dc-link voltages for the proposed PWM and CBPWM are compared in Fig. 18. The proposed control approach leads to precise dc-link voltage balancing, wherein the capacitor voltages are extremely close to each other. Conventional technique, on the other hand, provides differences in dc-link voltages, up to 4 V [see Fig. 18(b)]. The comparison of the common mode voltage for both modulation methods is presented in Fig. 19. For both methods, the amplitudes of CMV are at the same level.

The harmonic spectra (up to 50th harmonic) of line-to-line voltages of both modulation methods are shown in Fig. 20 for the unity modulation index. Therin, THD values of 1.54% and 2.42% were obtained for the proposed algorithm and CBPWM modulation techniques, respectively. Additionally, THD values of 2.92% and 2.82% were obtained for the proposed algorithm and CBPWM modulation techniques, respectively, while the 100 harmonics (including switching frequency) were taken into consideration for analysis.

A plot of THD (up to 50th harmonic) versus modulation index is shown in Fig. 21(a). In this figure, THD values for

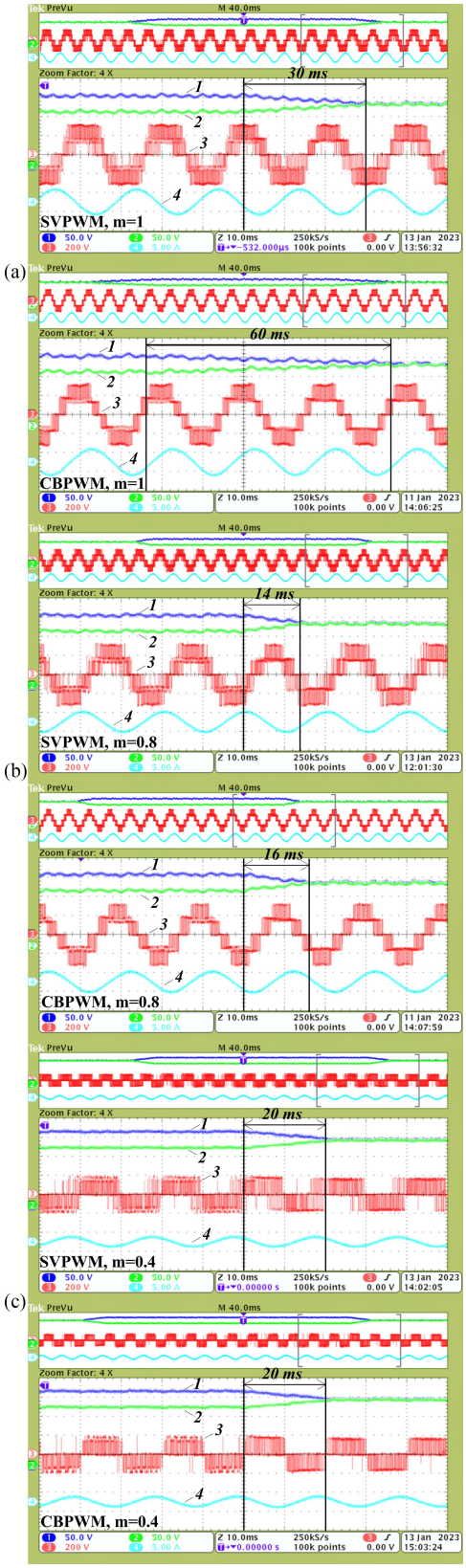

Fig. 15. Balancing algorithm performance for modulation indexes: (a) $m = 1$; (b) $m = 0.8$; (c) $m = 0.4$. DC-link voltages: 1), 2) 50 V/div; line-to-line voltage: 3) 200 V/div; phase current: 4) 5 A/div; time scale: 20 ms/div; output voltage frequency: 50 Hz. Proposed PWM on the top and CBPWM on the bottom.

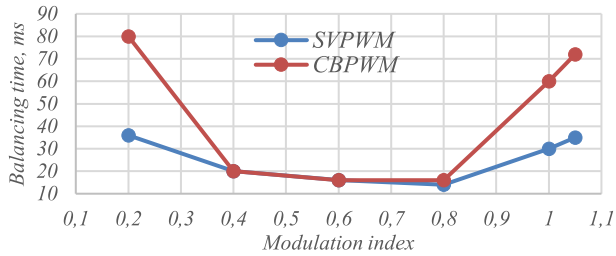

Fig. 16. Balancing speed for the proposed PWM technique and conventional CBPWM with different modulation indexes.

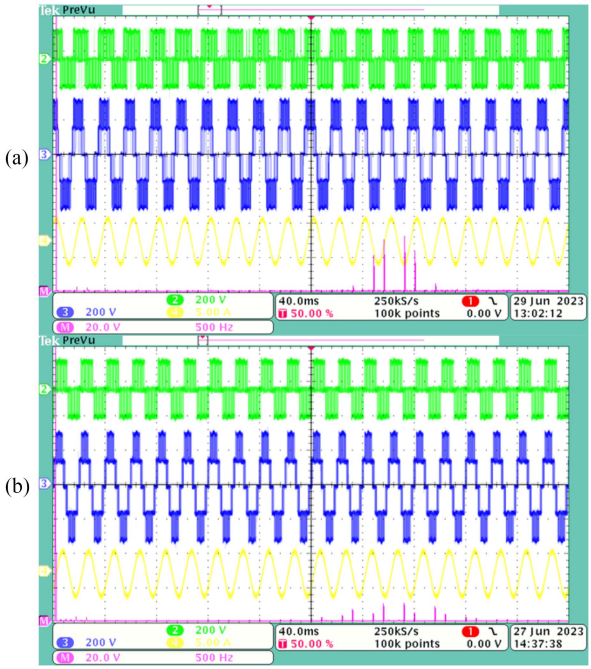

Fig. 17. Waveforms of the inverter phase voltage: 2) 200 V/div; line-to-line voltage: 3) 200 V/div; current: 4) 5 A/div; FFT analysis of the line-to-line voltages (20 V/div, 500 Hz/div) for (a) proposed and (b) CBPWM techniques. Time scale: 40 ms/div. Modulation index: $m = 1$.

both modulation methods are comparable for lower modulation indexes $m < 0.45$. Slight differences in THD values for the proposed and convenient modulation techniques may be noticed when the modulation index is higher than $m = 0.5$. Fig. 21(b) presents the plot of THD up to the 100th harmonic. Obtained THD values are comparable for higher modulation index $m > 0.8$. However, the CBPWM provides lower THD values in the modulation index range of 0.2 to 1. Switching frequency of 3.3 kHz was used for the analysis and THD calculation.

The computation time in three-phase configuration for hybrid PWM and for CBPWM techniques are 1.65 μs and 1.79 μs, respectively. Both algorithms were executed on the ADSP21363L DSP processor.

Figs. 22–25 present the experimental test results from the five-phase 3L NPC inverter with the proposed modulation method. Fig. 22 shows the output voltages during the step change of the modulation index. The voltage harmonic spectrum for a

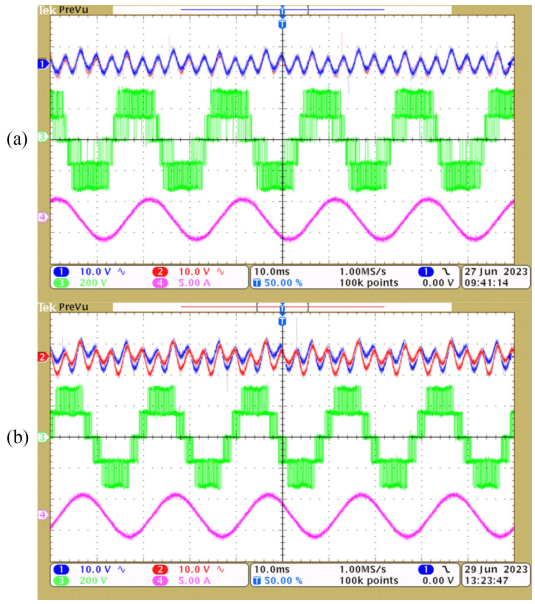

Fig. 18. Waveforms of ac components of both dc-link voltages for the (a) proposed PWM strategy and (b) CBPWM. Modulation index: $m = 1$; dc-link voltages: 1), 2) 10 V/div; output voltage: 3) 200 V/div; phase current: 4) 5 A/div; time scale 10 ms/div.

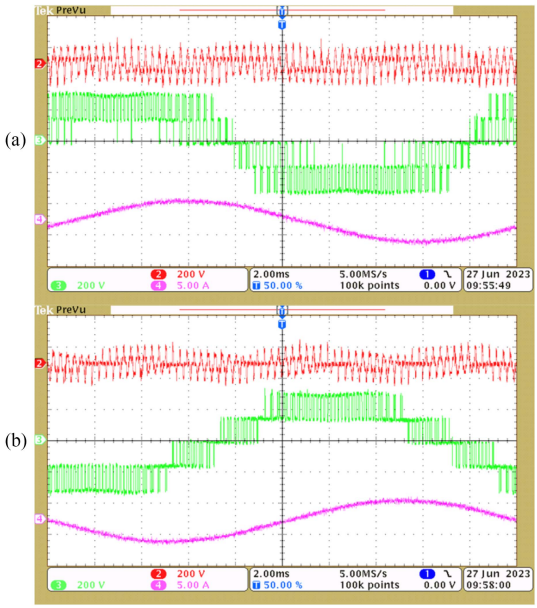

Fig. 19. Waveform of common mode voltage of the three-level, three-phase NPC inverter controlled using the (a) proposed modulation method and (b) CBPWM. CMV: 2) 200 V/div; line-to-line output voltage: 3) 200 V/div; output current: 4) 5 A/div; time scale: 2 ms/div.

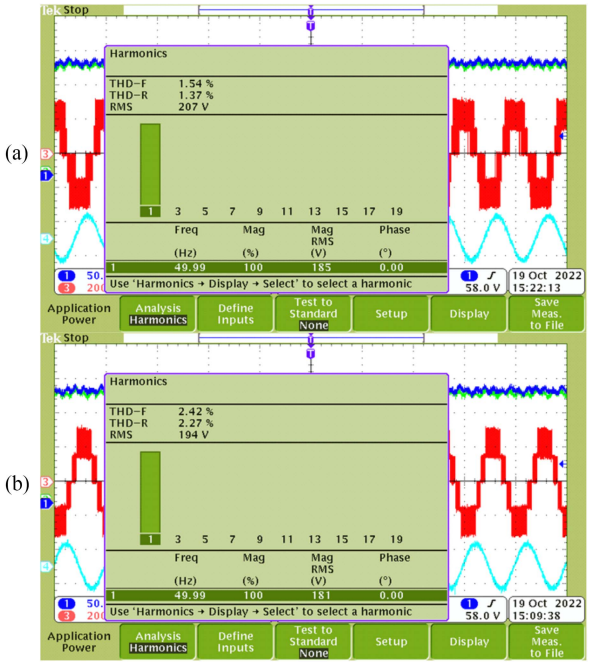

Fig. 20. FFT analysis (up to 50th harmonic) of the line-to-line voltages for the proposed and conventional modulation techniques; modulation index: $m = 1$. DC-link voltages: 1), 2) 50 V/div; line-to-line voltage: 3) 200 V/div; output current: 4) 5 A/div; time scale: 20 ms/div. (a) Proposed PWM. (b) CBPWM.

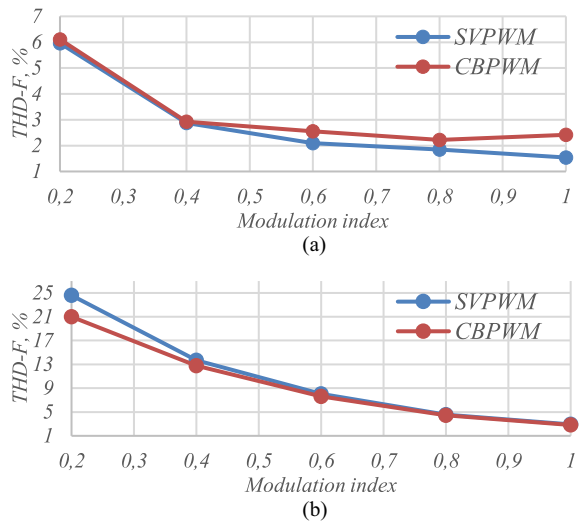

Fig. 21. FFT analysis of the line-to-line voltages for the proposed PWM and conventional CBPWM modulation techniques. (a) Up to 50th harmonic. (b) Up to 100th harmonic.

modulation index of 1 is shown in Fig. 23. The THD value is 2.68%.

The possibility of dc-link voltages balancing in five-phase VSI is shown in Fig. 24. When only a single fundamental output voltage harmonic was generated with the unity modulation index, the balancing time was 18 ms [see Fig. 24(a)]. In the case of simultaneous generation of fundamental (1st), $m_1 = 0.52$, and additional (4th), $m_4 = 0.87$, output voltage harmonics, the balancing time was 22 ms [see Fig. 24(b)]. The waveforms of both dc-link voltages, phase current, and line-to-line voltage, as well as the fast Fourier transform (FFT) analysis of the line-to-line voltage, are shown in Fig. 25. The time of computation in the five-phase configuration for the proposed algorithm is 1.91 μs.

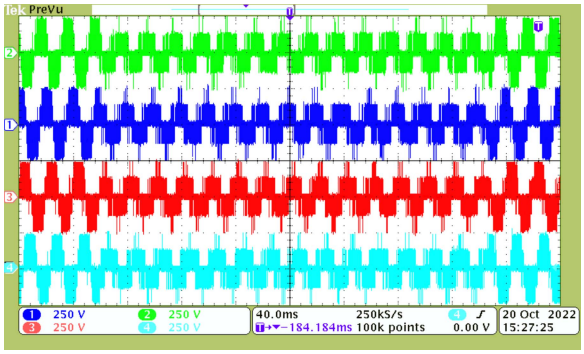

Fig. 22. Five-phase inverter step changes in the modulation index from 1 to 0.5 and back to 1. Output voltage waveforms: 250 V/div, 40 ms/div.

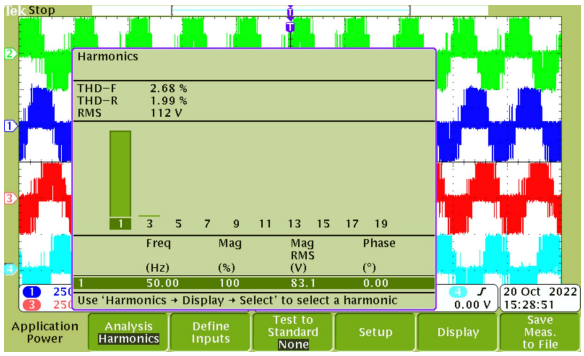

Fig. 23. FFT analysis of the line-to-line voltage for the proposed hybrid modulation technique in a five-phase configuration; modulation index: $m = 1$.

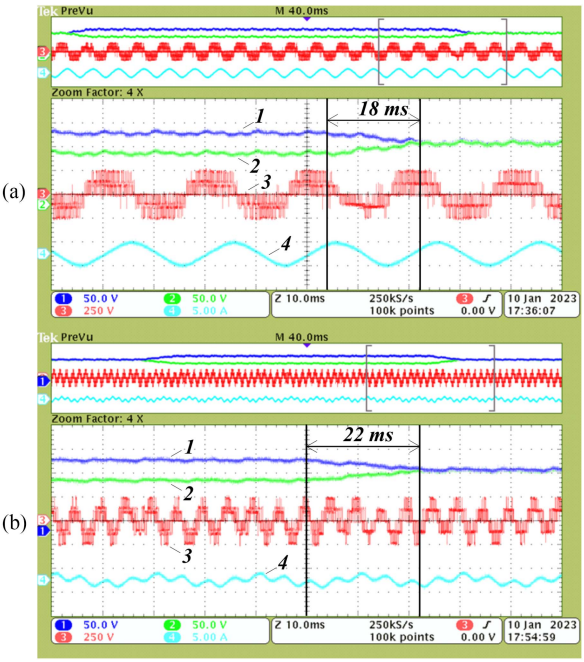

Fig. 24. Balancing algorithm performance for the proposed hybrid modulation technique in five-phase configuration. (a) Fundamental (1st–50 Hz) harmonic only; modulation index: $m = 1$. (b) 1st (50 Hz) and 4th (200 Hz) harmonics generation. DC-link voltages: 1), 2) 50 V/div; line-to-line voltage: 3) 250 V/div; output current: 4) 5 A/div, 10 ms/div.

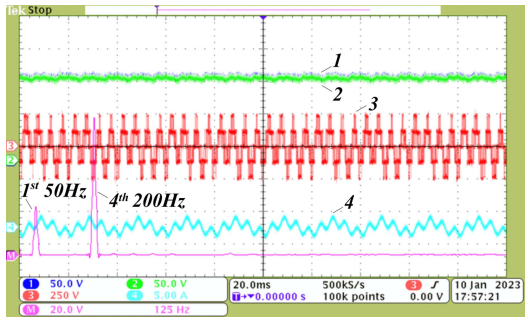

Fig. 25. FFT analysis (M) of the line-to-line voltage 3), phase current 4), and dc-link voltages 1), 2) for the proposed hybrid modulation technique in five-phase configuration, with 1st (50 Hz) and 4th (200 Hz) harmonics generation. The modulation indexes: 0.52 and 0.87. Scale: dc-link voltages: 50 V/div; line-to-line voltage: 250 V/div; current: 5 A/div, 20 ms/div; harmonics 20 V/div, 125 Hz/div.

IV. Conclusion

In this article, a simplified hybridized PWM strategy for three- and multiphase three-level NPC inverters was proposed. In the presented algorithm, the subsector searching problem was eliminated by treating the three-level inverter as a two-level inverter. The third level of the output voltage waveform is added by modifying the resulting switching pattern. The widths of these potential pulses are changed in the dc-link voltage balancing algorithm based on the energy-exchange concept. The resulting switching pattern is further optimized to reduce the number of commutations by modifying the zero vectors. The proposed modulation method was compared with the CBPWM technique for three-phase application. Compared to the CBPWM technique, the proposed modulation approach leads to faster and more precise balancing of the dc-link voltages. However, the switching losses are compromised since the commutation number is increased in the proposed solution. These features are the main advantages and disadvantages of the proposed hybrid PWM. The control approach was extended to multiphase, three-level NPC inverter operation. Laboratory tests were carried and experimental results were adequately presented for the five-phase, three-level NPC inverter.

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