IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 24 May 2024, accepted 20 June 2024, date of publication 26 June 2024, date of current version 9 July 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3419265

RESEARCH ARTICLE

Single-Phase 15-Level Switched-Capacitor Boost Multilevel Inverter Topology for Renewable Energy Applications

AHMED AWADELSEED[1], (Student Member, IEEE), ARKADIUSZ LEWICKI[1], (Senior Member, IEEE), AND ATIF IQBAL[2], (Fellow, IEEE)
[1]Faculty of Electrical and Control Engineering, Gdańsk University of Technology, 80-233 Gdańsk, Poland
[2]Department of Electrical Engineering, Qatar University, Doha, Qatar

Corresponding author: Ahmed Awadelseed (ahmed.awadelseed@pg.edu.pl)

ABSTRACT Galvanic isolation is a vital part of a grid-connected solar PV system. With the growth of multilevel inverters for grid-connected applications, the multilevel inverters having isolation are not sufficiently discussed in the literature. In this paper, a 15-level isolated multilevel inverter topology requiring only thirteen switches is proposed. The envisaged configuration includes two cells, designated as upper and lower cells. The upper cell includes a standard H-bridge, and the lower cell is a switched capacitor-based 5-level inverter. The outputs of the lower and upper cells are supplied to the load through single-phase isolation transformers. The proposed single-phase isolated inverter requires reduced switches to generate 15-level AC output voltage with a voltage gain of 7. In comparison to the MLIs mentioned in the literature, the switches connected in the proposed inverter experienced less voltage stress. The proposed inverter construction is contrasted with state-of-the-art MLIs described in the literature. PLECS software is used to simulate the inverter under various working environments, the proposed MLI able to maintain capacitor voltage balance and generate good power quality even at low values of modulation index. The experimental results achieved on a low-power laboratory prototype are utilized to validate the proposed inverter's performance. The claimed efficiency of the inverter calculated using simulation results is found to be 97.1%. However, the efficiency calculated using experimental results is 96.4% at 700W.

INDEX TERMS Multilevel inverter, switched capacitor (SC), self-voltage balancing, boost capability, isolated converter.

I. INTRODUCTION

Multilevel converters are becoming increasingly popular in the industry due to their high-power applications in a variety of systems such as variable speed drives, photovoltaic (PV) grid integration, electric locomotives, power quality improvement devices such as static reactive power compensation, and DVR. In addition to meeting increased power rating and power quality requirements, multilevel inverters also have the ability to eliminate harmonic distortion and the effects of electromagnetic interference [1]. Power semiconductor switching components, capacitor voltage sources, and regulating units make up multilevel inverters. Multilevel inverters are frequently utilized these days because of the several benefits they provide, such as lower switching losses, the capacity to operate at high voltages, fewer EMI losses, and improved efficiency [2].

The primary challenges associated with traditional MLIs are the lack of voltage gain, the requirements for the high number of components to generate higher output voltage, and the number [3], [4].

Reducing the number of components needed in MLIs is the primary objective of the research efforts in recent years. Researchers in academia and business are motivated by the above-mentioned limitations to propose circuits requiring lower component counts. The higher output voltage can be

The associate editor coordinating the review of this manuscript and approving it for publication was Poki Chen.

achieved by using a cascaded connection of a single H-bridge. However, this configuration makes the system bulky and increases the total cost, the lack of input voltage boosting factor (BF) is another drawback of the topologies presented in [5], [6], and [7].

The outcome of the study's effort to reduce the overall element requirement has resulted in many interesting structures, switched capacitor-based multilevel inverter (SC-MLI) is developed to address the issues of classical MLIs by reducing the number of elements with the capability of increasing the output ac voltage. In [8], a 13-level inverter utilizes four dc sources and 10 switches. which has a negative impact on efficiency. The work reported in [9] proposed an inverter using fewer switch counts to achieve higher output voltage levels. However, the topology requires multiple DC sources which increases the cost of the overall system. A new basic unit has been developed in [10] which includes a cross-network with two sources to generate 17 levels. The involvement of a high number of capacitors, however, increased the control complexity. In [11], the presented asymmetrical structure was implemented to increase the output voltage levels. These topologies have unique structures, although the number of switches is still quite significant in contrast to their output voltage and achieved gain.

In order to minimize the number of DC voltage sources. A solution proposed in [12] is addressed by replacing the DC source with switched capacitors to achieve high gain. Nonetheless, lacks self-balancing ability, and requires complex control to balance all used capacitors. The attempt to explore voltage boosting using a single DC source is presented in [13]. The proposed topology achieved high output voltage levels, however, the use of highly voltage-stressed switches restricts its applications. While in [14], a triple-mode SC unit, a double-mode SC-MLI unit, and two inverting half-bridges construct the 13-level inverter. Nevertheless, it suffers from significant capacitor voltage ripple. In [15] MLI topology uses less switch count with a voltage boost gain of 4. However, it requires 4 switched capacitors to obtain 15 output voltage levels. The work presented in [16] developed a switched capacitor MLI that can increase the output voltage to 6 times the input voltage with fewer components. However, this topology demand switches having higher values of peak inverse voltage (PIV). Similarly, a nine-level boost inverter using a unique and efficient switched capacitor topology is developed [17]. It obtains a voltage gain of 4 by employing a few possible switches. Nevertheless, some of the switches also need to withstand the maximum output voltage.

To overcome the issue with capacitor balance and the need for complex control techniques, a significant research interest among researchers is found in solving the capacitor voltage unbalancing problem, by developing new topologies capable of self-capacitor voltage balancing. self-voltage balancing of switched capacitors is handled in [18] by linking external circuits, which raises the system cost. The capacitor voltage balancing issue becomes more severe with an increase in the number of levels of output voltage. Further, a complex control strategy is required to ensure capacitor voltage balancing. The coupling of two back-to-back T-type converters resulted in a 13-level inverter employing two asymmetrical sources [19]. Similar to this, a K-type inverter structure has been proposed in [20], providing a multilayer structure capable of balancing capacitor voltages without the use of external circuits or control approaches. However, the proposed design has limited practicality for real-world applications due to the demand for more isolated DC voltage sources and a greater number of switching capacitors. D. Upadhyay introduces UXE-Type topology in [21] consisting of 12 switches and a single DC source with two switched capacitors able to produce thirteen output voltage levels. However, the voltage stress across some of the power switches and capacitors is greater than the input DC source. Various topologies, on the other hand, aim to achieve high output voltage gain while demanding switches with lower voltage stress. Reference [22] proposes a capacitor-based MLI capable of outputting 17 levels, which requires 14 switches, 4 capacitors, and 2 DC sources to raise the output AC voltage. However, the more the number of capacitors utilized, the greater the total blocking voltage (TBV), and the maximum voltage stress equals three times the input voltage. In [23], one configuration can generate up to 9 levels using 12 switches. The AC output voltage can be produced with the help of two switching capacitors. The inverter proposed in [24] demands two DC input voltage sources and one capacitor to generate 15-level AC output voltage. The topology suggested in [25] includes five DC sources and ten switches, which increases the overall cost of the inverter. These topologies [23], [24] require a smaller number of semiconductor devices. However, it is not possible to increase the BF more than unity and higher TBV appears across the devices.

To address the TBL problem, the MLI family utilizes multi-input DC sources to generate asymmetrical and symmetrical topologies. References [26] and [27] describe a 15-level inverter that requires three DC input voltage sources. Although these topologies use fewer components, the BF obtained is not cost-effective due to the increased number of switched capacitors. The SC-MLI structure proposed in [28] has a voltage gain of 6 and can accomplish good compromises in terms of the number of DC sources, component count, and TBV. However, the split capacitors employed cause voltage balancing issues and necessitate elaborate management approaches to ensure the capacitor's voltage balance. Further, all these topologies lack galvanic isolation.

To tackle the issues raised above, several transformer-based MLIs and techniques to estimate the magnitudes of DC voltage sources have been proposed in order to improve the number of output voltage levels while using fewer power semiconductor devices. To elevate the voltage level, tie together H-bridge cells (HBCs) in series as demonstrated in [29], [30], and [31]. Three h-bridges are utilized per leg in these topologies, and three transformers are required to boost the voltage level from 7 to 21. In the structure

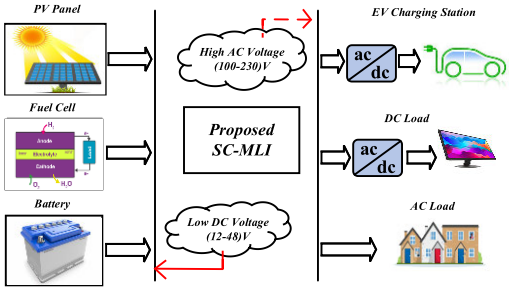


FIGURE 1. Block diagram of proposed SC-MLI used to interface various sources and loads.

proposed in [32], a single transformer is also employed. However, the proposed construction demands the use of a flying capacitor and a large number of clamping diodes. Two transformers are used in [30] to provide a 15-level single-phase alternating current output voltage. The primary constraints of the arrangement outlined in [33] are the need for extra transformers and separate DC sources, which increase the system's cost, size, and weight.

To address above mentioned limitations, this paper presents an isolated SC-MLI structure capable of generating a maximum of 15-level AC output voltage. The suggested inverter construction provides a higher number of levels in AC output voltage using a smaller number of semiconductor devices. This topology consists of 13 switches, 2 single-phase transformers and one switched capacitor, which is fed from a single input DC source. Nearest level control (NLC) implemented by the proposed inverter for gate pulse generation. Under various load situations, this control approach can attain all output voltage levels. The main objective of this study is to introduce a novel isolated inverter that is based on a switched capacitor-based multilevel inverter with the following salient features:

- The proposed converter requires a single DC input source to generate a 15-level AC output voltage.
- The proposed converter ensures self-voltage balancing across the capacitor under different loading conditions.
- The proposed converter offers a voltage gain of 7 (V_o: $V_{dc} = 7$).
- The transformers provide galvanic isolation between load and source.
- The magnitude of ripples in the output current of the proposed converter is reduced due to the inherent filtering capability of the transformer leakage inductance.

These features allow the proposed inverter to be employed in applications such as solar PV, fuel cells, battery power applications, industrial motors, and so on, as illustrated in Fig. 1. The suggested topology can also be employed in applications such as microgrids, which provide remote electrification facilities.

II. WIND PROPOSED 15-LEVEL MLI TOPOLOGY

A. DESCRIPTION OF PROPOSED TOPOLOGY

Fig. 2 depicts the proposed inverter configuration used to produce a single AC output voltage, which includes

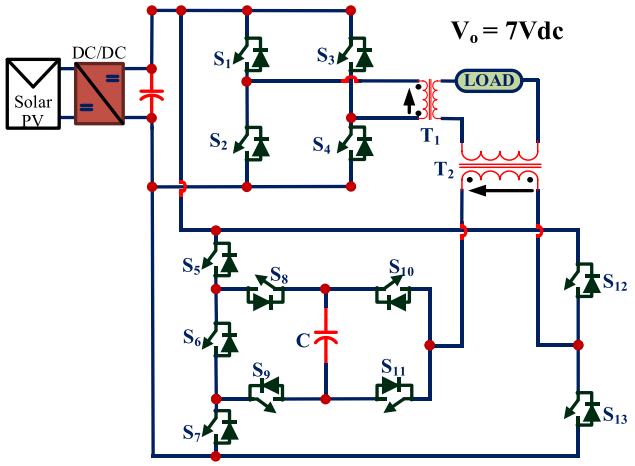


FIGURE 2. Proposed 15-Level SC-MLI.

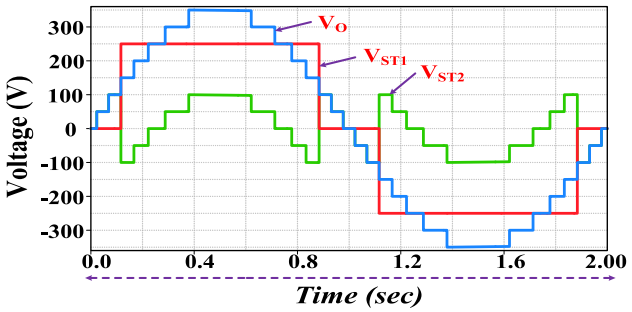


FIGURE 3. Induced voltage waveforms for V_{ST1}, V_{ST2} and V_O.

13 unidirectional switches, one switched capacitor, and two transformers, T_1 and T_2. The proposed converter produces a 15-level output AC voltage with a voltage gain of 7. The suggested 15-level structure comprises dual voltage-boosting components, namely a switching capacitor, C, and a transformer, T_1. The switched capacitor, C, is utilized to feed energy to the load symmetrically during the positive and negative cycles, and the voltage across the capacitor remains balanced, demonstrating the proposed MLI's self-balancing capacitor voltage.

The output of H-bridge is applied to the primary winding of the transformer, T_1, while the load is connected in series to the secondary windings of the transformers, T_1 and T_2. The voltage across the primary winding of T_1 with N_{PT1} turns can be derived as a switching function of power electronic devices, S_1 and S_3 given by:

$$V_{PT1} = V_{dc}(S_1 - S_3) \tag{1}$$

where, V_{dc} input dc source. Using (1), the voltage of the secondary side of T_1 with N_{ST1} turns can be expressed as

$$V_{ST1} = \left(\frac{N_{PT1}}{N_{ST1}}\right) * [V_{dc}\,(S_1 - S_3)] \tag{2}$$

Fig.3 represents the output voltage, V_{ST1} of h-bridge, while V_{ST2} corresponding to the voltage across the second cell. The

overall output voltage of the inverter V_O is a combination of voltages of H-bridge and second cell (i.e., V_{ST1} and V_{ST2} respectively), forming a 15-level output voltage.

The proposed topology employs a staircase pulse width modulation technique commonly known as Nearest Level Control (NLC). The output voltage V_O can be represented by Fourier series given by;

$$V_O(\omega t) = \sum_{j=1}^{L} \sum_{n=1}^{\infty} \frac{2V_p}{n\pi} \left[\cos(n\theta_i) - \cos\left[n(\pi - \theta_i)\right]\right] \sin(n\omega t) \quad (3)$$

where L is the total number of levels, n is the harmonic order, θ is the load angle, and V_p is peak voltage divided by the number of levels in a one-quarter cycle. The Fundamental and harmonic components of output voltage, $V_{O(fund)}$, $V_{O(har)}$ evaluated from (3) for L-level inverters are obtained as

$$V_{O(fund)} = \frac{4V_p}{\pi} \sum_{i=1}^{L} \cos(\theta_i) \quad (4)$$

$$V_{O(harm)} = \frac{4V_p}{(2x-1)\pi} \sum_{i=1}^{L} \cos\left[(2x-1)\theta_i\right] \quad (5)$$

where, $x = 2, 3, 4, \ldots$. As per the IEEE Std. 519, the resulting THD in output ac voltage of the converter must not exceed 5% of the magnitude of the fundamental component, of voltage, $V_{o(fund)}$. To check the quality of the resulting output voltage waveform, the total harmonic distortion (THD) is evaluated which is given by the following expression:

$$THD = \frac{\sqrt{\frac{4V_p}{(2x-1)\pi} \sum_{i=1}^{L} \cos\left[(2x-1)\theta_i\right]}}{\frac{4V_p}{\pi} \sum_{i=1}^{L} \cos(\theta_i)} \quad (6)$$

TBV provides information about the specifications, costs, performance, and operation of the switches utilized in the topology. Therefore, the value of the maximum TBV for the proposed structure is obtained as:

$$TBV = \sum_{i=1}^{13} V_{si} \quad (7)$$

where V_{si} stands for the maximum voltage blocked by the i^{th} switch.

$$\begin{cases} S_1 = S_2 = S_3 = S_4 = V_{dc} \\ S_{12} = S_{10} = S_8 = S_9 = V_{dc} \\ S_5 = S_6 = S_{11} = S_{13} = V_{dc} \end{cases} \quad (8)$$

From equations (7) and (8), the expression for the TBV can be written as,

$$TBV = 13V_{dc} \quad (9)$$

B. OPERATION MODES OF PROPOSED MLI

The secondary winding of the transformer T_1 produces voltage levels of $5V_{dc}, 0, -5V_{dc}$, while the transformer of the second cell T_2 generates output voltage with levels of $2V_{dc}$, V_{dc}, 0, $-V_{dc}$ $-2V_{dc}$, to produce a peak output voltage of $V_O = 5V_{dc} + 2V_{dc} = 7V_{dc}$. The conduction states for all positive voltage levels of the proposed topology are shown in Fig. 4. and are discussed below:

- ***State A*** ($V_{ST1} = 0, V_{ST2} = V_{dc}, V_o = V_{dc}$): In this state, the capacitor, C starts charging, the H-bridge at this stage produces zero power and the output voltage level is produced by the second cell as in Fig. 4(b).
- ***State B*** ($V_{ST1} = 0, V_{ST2} = 2V_{dc}, V_o = 2V_{dc}$): During this voltage state, the capacitor, C still discharging, and the output voltage obtained is $2V_{dc}$. The corresponding circuit diagram is shown in Fig. 4(c).
- ***State C*** ($V_{ST1} = 5V_{dc}, V_{ST2} = -2V_{dc}, V_o = 3V_{dc}$): The switching diagram for this stage is shown in Fig. 4(d). In this stage, the capacitor, C continues to discharge through the load, and the load voltage level is equal to $3V_{dc}$.
- ***State D*** ($V_{ST1} = 5V_{dc}, V_{ST2} = -V_{dc}, V_o = 4V_{dc}$): In this voltage state as shown in Fig.4(e), the capacitor starts discharging and the output voltage level having its peak value equal to $4V_{dc}$ is achieved.
- ***State E*** ($V_{ST1} = 5V_{dc}, V_{ST2} = 0, V_o = 5V_{dc}$): In this operating mode, the capacitor, C still charging through the load, and the output voltage level is generated by the upper H-bridge cell while the lower cell produces zero power as shown in Fig. 4 (f).
- ***State F*** ($V_{ST1} = 5V_{dc}, V_{ST2} = V_{dc}, V_o = 6V_{dc}$): During his operating mode, the capacitor, C starts charging and the series connection of secondaries of T_1 and T_2 produces a level with a voltage magnitude of $6V_{dc}$ which is shown in Fig.4 (g).
- ***State G***($V_{ST1} = 5V_{dc}, V_{ST2} = 2V_{dc}, V_o = 7V_{dc}$): In this operational mode, the proposed topology generates zero voltage across the load as shown in Fig.4 (h). For this state, the capacitor C discharging.
- ***State O*** ($V_{ST1} = V_{ST2} = V_o = 0$): As shown in Fig. 4 (a), zero voltage appears across the load, and the capacitor is connected to the DC voltage source and gets charged to V_{dc}.

A similar analysis can be applied over the negative half cycle of the output voltage. The switching pattern used to generate a 15-level output voltage, V_O is presented in Table 1.

C. TRANSFORMER TURNS RATIO CALCULATION

The number of levels represented in the proposed MLI's output voltage and the voltage gain is highly controlled by the transformer turns ratios, T_1 and T_2. The transformer T_1 turns ratio is determined by the input and output voltage requirements, which are provided by,

$$N_{T1} = N_{T2} = \frac{V_{dc}}{4f_s B_m A_c} \quad (10)$$

where, B_m is maximum flux density and A_c is the effective cross-sectional area of the core measured in cm^2. The isolated topology presented in this study employs a distinct transformer (i.e., 1:5 (T_1) and 1:1 (T_2) turns ratio) for achieving maximum output voltage levels. As a result of the varied turn ratios, the power rating (S_T) of utilized

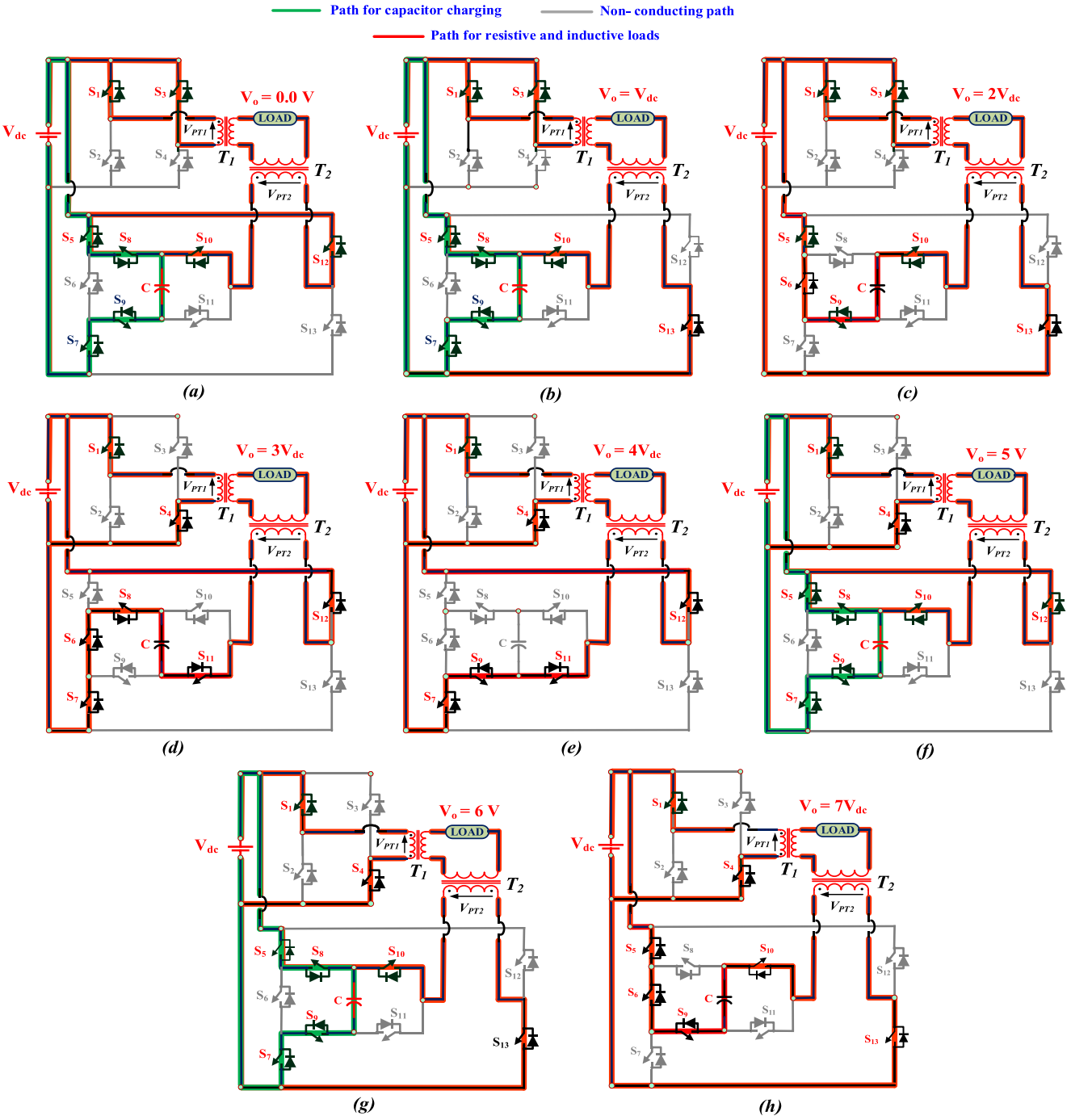


FIGURE 4. Different stages of the proposed single-stage SC-MLI topology, which produces 15-level ac output voltage.

transformers varies. The transformer's power rating may be calculated as follows:

$$S_T = N_{ST} V_{dc} I_o \tag{11}$$

where, I_o is the load current, and N_{ST} is the secondary windings of the transformer T_1 or T_2.

D. SELECTION OF SWITCHED CAPACITOR

As illustrated in Fig. 5., The capacitor C is charged with voltage levels of 0, $+V_{dc}$, $+5V_{dc}$, $+6V_{dc} - 5V_{dc}$, $-6V_{dc}$ and discharges during voltage levels of $+2V_{dc}$, $+3V_{dc}$, $+4V_{dc}$, $+4V_{dc}$, $+7V_{dc}$, $-2V_{dc}$, $-3V_{dc}$, $-2V_{dc}$, $-3V_{dc}$, $-4V_{dc}$, $-4V_{dc}$, $-7V_{dc}$. Over a fundamental cycle of output AC voltage, the charging and discharging times of the capacitors are identical. As a result, regardless of the load characteristics,

TABLE 1. Switching states of proposed topology.

Levels	Switching States	Effect on Capacitor
$+7V_{dc}$	$S_1, S_4, S_5, S_7, S_8, S_{10}, S_{13}$	↓
$+6V_{dc}$	$S_1, S_4, S_5, S_6, S_8, S_9, S_{10}, S_{13}$	↑
$+5V_{dc}$	$S_1, S_4, S_5, S_6, S_8, S_9, S_{10}, S_{12}$	↑
$+4V_{dc}$	$S_1, S_4, S_5, S_6, S_8, S_9, S_{11}, S_{12}$	↓
$+3V_{dc}$	$S_1, S_4, S_6, S_7, S_9, S_{11}, S_{12}$	↓
$+2V_{dc}$	$S_1, S_3, S_5, S_6, S_8, S_9, S_{10}, S_{13}$	↓
$+V_{dc}$	$S_1, S_3, S_5, S_8, S_{10}, S_{13}$	↑
0	$S_1, S_3, S_5, S_7, S_8, S_9, S_{10}, S_{12}$	↑
0	$S_1, S_3, S_5, S_6, S_8, S_9, S_{10}, S_{12}$	↑
$-V_{dc}$	$S_1, S_3, S_7, S_9, S_{11}, S_{12}$	↑
$-2V_{dc}$	$S_1, S_3, S_6, S_7, S_8, S_{11}, S_{12}$	↓
$-3V_{dc}$	$S_2, S_3, S_5, S_7, S_8, S_{10}, S_{13}$	↓
$-4V_{dc}$	$S_2, S_3, S_5, S_6, S_8, S_9, S_{10}, S_{13}$	↓
$-5V_{dc}$	$S_2, S_3, S_5, S_6, S_8, S_9, S_{11}, S_{13}$	↑
$-6V_{dc}$	$S_2, S_3, S_5, S_6, S_8, S_9, S_{11}, S_{12}$	↑
$-7V_{dc}$	$S_2, S_3, S_6, S_7, S_9, S_{11}, S_{12}$	↓

Note: (↑) denotes charging of capacitor; (↓) denotes discharging of capacitor.

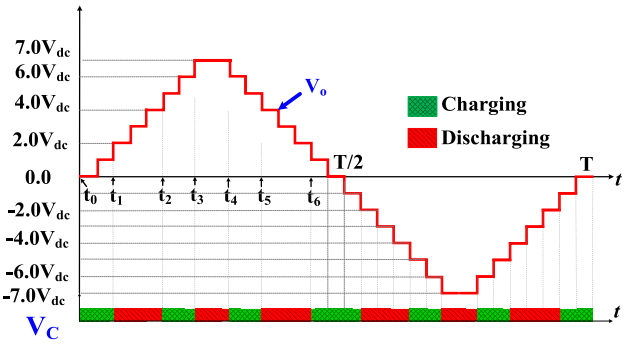


FIGURE 5. Staircase output voltage with capacitor voltage pattern.

the capacitor maintains self-voltage balancing. Depending on the principle of charge balance, capacitor value can be determined using [20] as

$$C = \frac{I_o}{2\pi f_o \Delta V_c} \tag{12}$$

where, I_o is the peak value of load current and f_o is the frequency of the output voltage.

III. MODEL MODULATION TECHNIQUE

The nearest level control (NLC) has been applied, as a low-frequency technique for gate pulse generation. In NLC, the sinusoidal reference signal V_{sine} is compared to the staircase output voltage waveform V_{stair}, as shown in Fig. 6. The

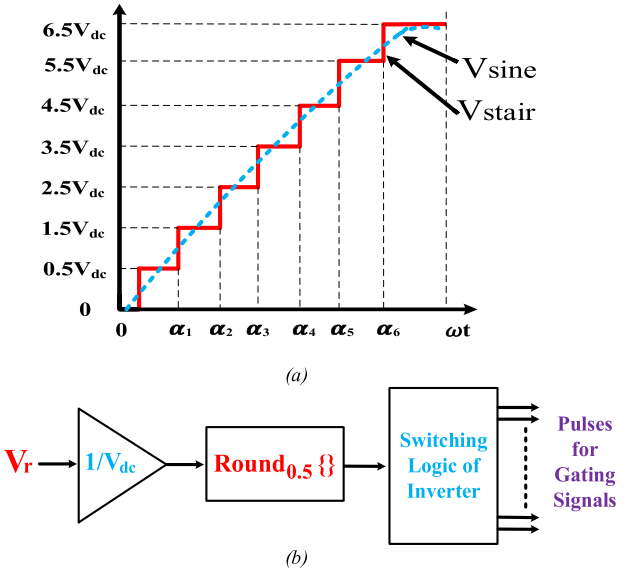


FIGURE 6. a) Level generation in NLC and. b) inverter switching logic.

comparison creates pulses, which are then utilized to generate gate pulses based on the switching logic of the proposed topology shown in Table 1.

By considering Fig. 6, the constant carrier signals L_1 to L_n are represented for N output voltage levels as

$$\begin{aligned} L_1 = 0.5, L_2 = 1 + 0.5, \ldots\ldots : L_{n-1} \\ = (n-2) + 0.5, L_n = (n-1) + 0.5 \end{aligned} \tag{13}$$

where, $n = (N\text{-}1)/2$.

The output voltage with M as the modulation index is obtained as;

$$V_{out} = \mathrm{M} \times \frac{N-1}{2} \times V_{dc} \times \cos(\omega t) \tag{14}$$

The modulation index M can be varied in NLC by changing the Vref and can be defined in (15).

$$\mathrm{M} = \frac{2V_{ref}}{(N-1)V_{dc}} \tag{15}$$

The conventional NLC switching angles can be determined using the following relationship:

$$\alpha_j = sin^{-1}\left(\frac{i-0.5}{n}\right) \tag{16}$$

where α_j = switching angles, $i = 1, 2, 3 \ldots..$ n.

IV. COMPARATIVE ASSESSMENT

A comparative study is carried out in this part to highlight the prominent aspects of the proposed topology and evaluate its feasibility in comparison to existing topologies. Table 2 provides a comparison of the suggested topology with state-of-the-art 15-level MLIs suggested in [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], and [30]. The 13-level MLIs presented in [7], [8], and [14] require switches with high TBV and capacitors

TABLE 2. Comparison table for different MLI-topologies with proposed topology.

Top.	N_L	G	N_{IS}	N_{SW}	N_C	N_{GD}	TBV	N_D	N_T	C_F	η (%)
[7]	13	1:6	1	13	3	13	33	2	0	4.92	95.90
[8]	13	1:6	1	14	3	14	30	1	0	4.77	91.50
[14]	13	1:2	2	14	2	11	18	0	0	4.85	95.35
[15]	13	1:1.5	1	12	4	11	34	0	0	4.69	96.12
[19]	13	1:3	1	13	3	13	14	3	0	4.15	96.5
[20]	15	1:3.5	3	8	0	8	30	0	0	9.20	95.2
[22]	15	1:1	3	10	0	10	12	0	0	7.20	93.8
[26]	15	1:1	4	12	0	11	36	0	0	15.73	96
[27]	15	1:1.5	2	10	1	10	34	1	0	7.47	95.8
[28]	15	1:1	3	10	0	9	36	0	0	7.4	93
[23]	15	1:3.5	1	12	0	12	32	0	3	3.93	93
[24]	15	1:6	1	16	0	16	32	0	1	3.93	90
[25]	15	1:3.5	1	12	0	12	12	0	3	2.60	92
[29]	15	1:0.5	1	24	12	24	4	12	1	5.13	92
[30]	15	1:2	1	12	6	12	21	0	7	4.40	94
[P]	**15**	**1:7**	**1**	**13**	**1**	**13**	**13**	**0**	**2**	**2.8**	**96.4**

N_L= Number of levels, G = voltage boost ratio, N_{IS}= number of input dc sources, N_{SW}= Number of switches, N_C=Number of flouting capacitors, N_C=Number of capacitors, N_{GD}=Number of gate drivers, **TBV** = Total blocking voltage, N_D= Number of diodes, N_T= Number of transformers, C_F =Cost function, η= Efficiency,

with high breakdown voltage, The voltage ratings of these components are high. These factors lead to an increase C_F due to the increased voltage rating of the components. The Topologies presented in [15], [16], and [19] require less components. However, the voltage gain of these converters is reduced which limits the voltage boost action of these converters. The proposed 15-level converter offers a voltage gain of 7 which is the highest among the reported 15-level topologies in [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], and [32].

It is observed from Table 2 that the topologies presented in [15], [20], [21], [22], [26], [27], and [28] demand more than a single dc source. The staircase output can be generated without a capacitor in the case of topologies demonstrated in [20], [22], [26], and [27]. However, these configurations require more input DC sources than the proposed topology which may not be feasible in a given system and is considered a less viable option. The single source MLIs are discussed in [23], [24], [25], [28], [29], and [30]. However, the advantages provided by these MLIs are overshadowed by due to the extra cost of the additional source. Therefore, single source-based MLIs are preferred.

The total blocking voltage (TBV) of an MLI is an important factor for comparison, determining both the price and the requirement for switching devices. The TBV of MLIs proposed in [7], [8], [14], [15], [23], [24], [26], [27], and [28], is higher, whereas in the MLIs proposed in [19], [20], [21], and [22] is less than 20. The topology suggested in [29] has the lowest value of TBV. The next higher value of TBV is 12 which is reported in [22] and [29]. The proposed 15-level isolated converter requires switches having TBV across the switches equal to 13. The reduced value of TBV of the proposed converter shows its cost-effective feature.

The efficiency of the various power switches in the steady state is calculated using PLECS software. An output voltage with a peak magnitude of 350V is produced when the input voltage is set to 50V. The conduction, switching, and power losses of semiconductor devices are included when estimating and comparing efficiency. The proposed topology has a peak performance of 97.1% at a rated power output of 700W.

A cost comparison is also presented in Table 2 to compare the prices of the topologies. The Cost Factor, C_F is determined as follows:

$$C_F = \frac{N_{IS}(N_{SW} + N_D + N_C + N_{GD} + N_T + TBV)}{N_L}. \quad (17)$$

The proposed topology has the lowest cost factor, demonstrating the virtues of the proposed isolated MLI. When contrasted with other topologies, the suggested topology has the lowest component cost, competitive TBV, and higher BF. As a result, the suggested topology's lower cost is reflected in the reduced number of switches.

V. RESULTS AND DISCUSSION

A. SIMULATION RESULTS

The simulation results of the proposed 15-level inverter have been discussed, and PLECS software has been used for this purpose. To examine the effectiveness of the 15-level inverter, a source with a magnitude of 50V is used. For the pulses of different switching elements, Nearest Level control (NLC) technique has been used. The simulation performance

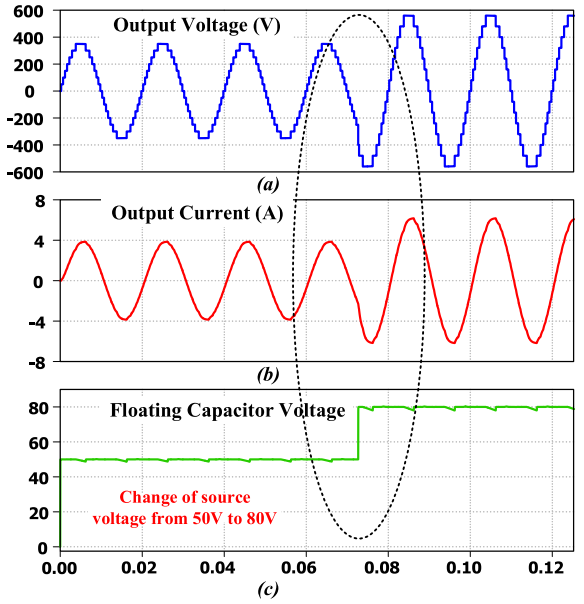


FIGURE 7. Responses of proposed SC-MLI with variations of input voltage from 50V to 80V.

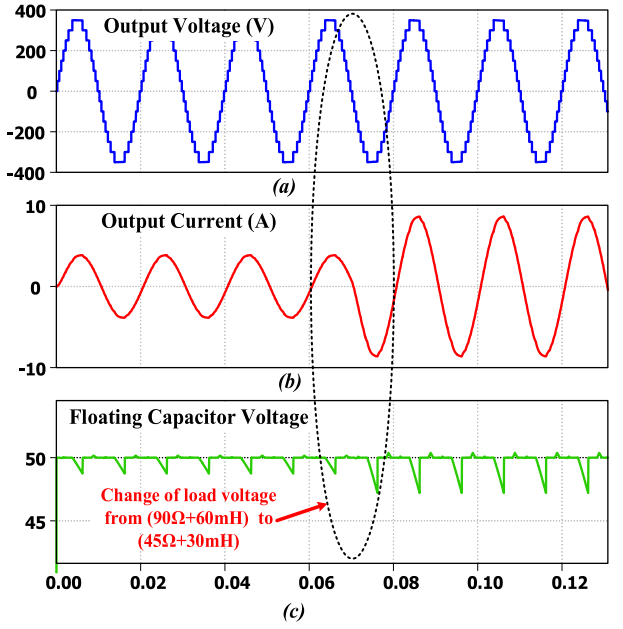


FIGURE 8. Responses of proposed SC-MLI under load change: Output voltage, load current, and capacitor voltages.

analysis of SC-MLI is evaluated for various steady-state and dynamic loading conditions.

The transient test for output voltage when a sudden change in input voltage from 50V to 80V is conducted in simulation when the connected load is (90Ω + 60 mH). Fig. 7 depicts the output voltage, current, and switched capacitor voltage, When the input voltage is increased from 50V to 80V, the capacitor voltage similarly increases from 50V to 80V, as well as the output voltage level is maintained at 15 levels without any oscillation.

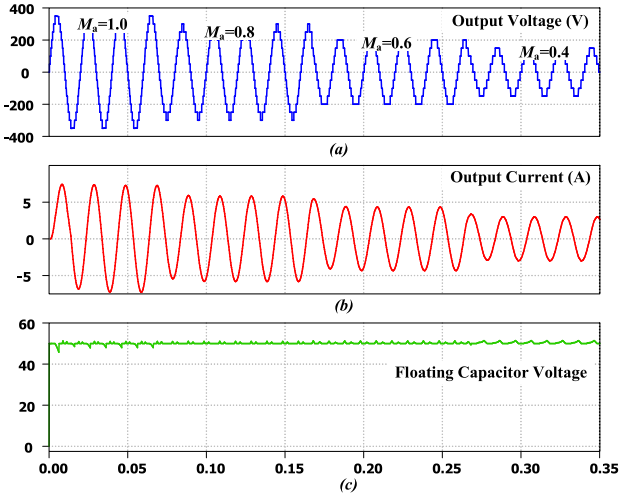


FIGURE 9. Responses of proposed SC-MLI with Modulation index (M_a) change.

Dynamic responses of the proposed SC-MLI from full-load (90Ω+60mH) to half-load (45Ω+30mH) are tested keeping the input fixed (50V). The ripple in the floating capacitor voltage fluctuates within 10% of its maximum value, which is acceptable. As shown in Fig.8, the transient is quite smooth and does not interfere with the functionality of the proposed inverter. The waveform clearly confirms the stability of the proposed SC-MLI under load variations and gives satisfactory results in all operating conditions with self-voltage balancing of the capacitor voltage.

Further, the dynamic responses of the proposed SC-MLI under a varied modulation index are tested. Fig. 9 shows the performance of the proposed SC-MLI under the external disturbance in the modulation index (M_a). in intervals from (t = 0 sec to t = 0.075 sec), the reference phase modulation signals are generated with M_a =1.0 and a frequency of 50Hz. Then another external disturbance is applied in M_a from 1.0 to 0.80, 0.60, and then 0.40, as shown in Fig. 9. As the modulation index decreases, the levels change. It is clearly observed that the proposed SC-MLI has a high response to modulation index changes and also the inverter is able to produce 7 levels with lower modulation index.

VI. EXPERIMENTAL VALIDATION

The proposed 15L isolated MLI topology is validated in the laboratory and the laboratory prototype is shown in Fig. 10. The Texas Instruments (TI) digital signal processor (DSP) F28379D is used to generate the gate pulses using the nearest level control technique (NLC). The battery supply, TDK Lambda GEN300-11 is used as a DC input source and an input voltage of 50V is applied across the input of the proposed converter, which generates a peak output voltage of 350V with a voltage gain of 7. The load is connected to the output terminals of the proposed converter. The parameters of the proposed MLI topology are presented in Table 3. The power ratings transformers, T_1 and T_2 are identical, which

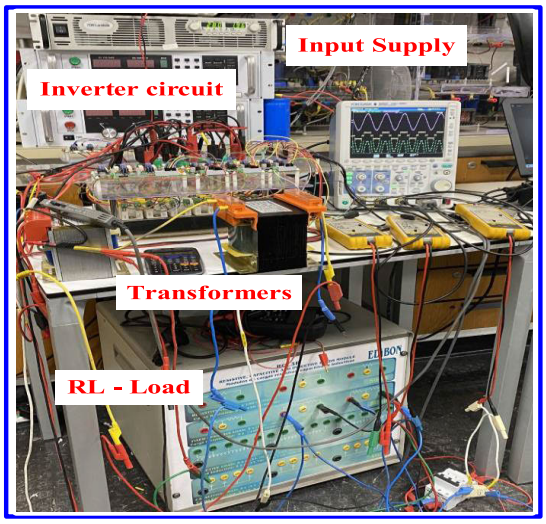


FIGURE 10. Laboratory prototype of the proposed 15-level inverter.

TABLE 3. Specifications of components.

Parameter	Rating
Switches	G60N100 IGBT
Capacitor	PG6DI (450V and 2200μF)
Controller	FPGA Vertix-5 (XC5VLX50T)
Gate Driver	GDA-2A4S1
dc power supply	TDK Lambda GEN300-11
Input dc Link Voltage	50V
Output Voltage	350V (peak)
Fundamental Frequency	50 Hz
Inductor	100mH, 50mH
Resistive Load	25, 50, 150 Ω

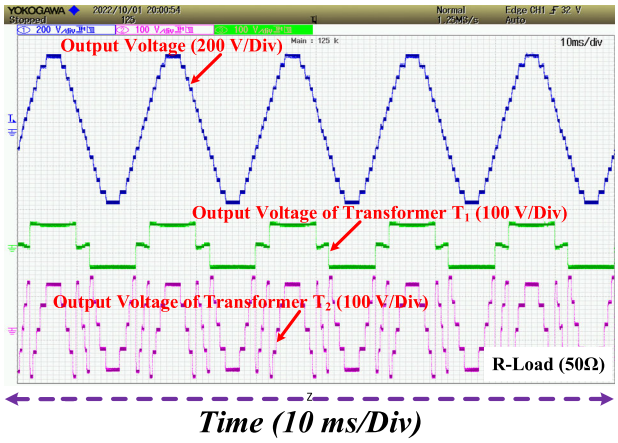


FIGURE 11. Output voltage (V_O), transformer (T_1) voltage and transformer (T_2) voltage for R-Load.

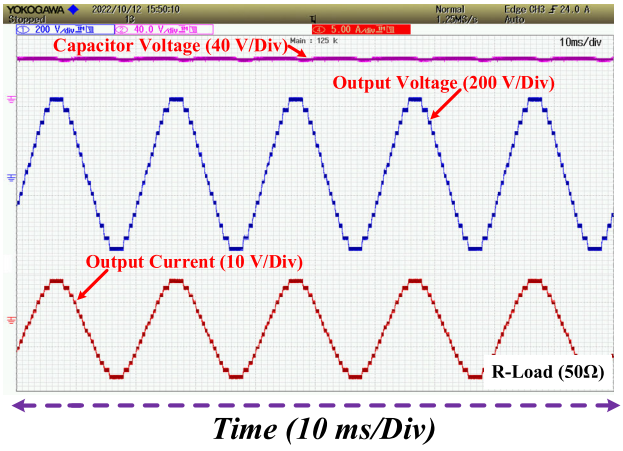


FIGURE 12. Waveforms of output voltage (V_o), load current (I_o), and the voltage (V_c) across the switched capacitor for R-load.

is 1000 W each. The turns ratio of transformers T_1 and T_2 are 1:25 and 1:5, respectively.

Fig. 11 shows the waveforms of the output voltage, V_o, voltage across the secondary of the transformer, T_1, and voltage across the secondary of the transformer, T_1, respectively. From these waveforms, it is observed that the voltage across the secondary of T_1 is quasi-2-level AC output voltage while the voltage across the secondary of T_2 is 5-level AC output voltage. The load is connected across the series connection of secondaries of transformers, T_1 and T_2. A 15-level single-phase output AC voltage appears across the load, and each level is equal to the magnitude of DC input voltage.

Fig. 12 shows the waveforms of voltage across the switched capacitor, C, output voltage, v_o, and load current, i_o. Corresponding to the load demand of 700W, the current waveforms also possess 15 levels.

Now the performance of the proposed 15-level isolated MLI is tested under changing load conditions. For this purpose, the load connected across the output of the proposed converter undergoes a step variation in load demand from 300 Ω to 150 Ω, at a time instant of t=0.5sec. As shown in Fig. 12, this change is reflected in the increase in load current. The initial value of load current, (I_o) as observed in Fig. 13 is 0.84A. After a time interval of t=0.5sec, the load current increases from 0.84 to 1.65A. During the step variation in load demand, the voltage across the switched capacitor, C, remains balanced.

Fig. 14 shows the waveforms of output voltage, V_o, load current, Io, and secondary currents of transformers, T_1 and T_2, respectively. Since the secondaries of T_1 and T_2, are connected in series, therefore, identical values of current flows through the load, secondaries T_1 and T_2. This can be observed from Fig. 14. From all of these experimental findings, it can be concluded that the proposed 15-level MLI operates as anticipated, self-balancing capacitor voltage while preserving boosting capability.

The suggested inverter is tested under RL-Load to investigate further its stability under changing load circumstances. Output waveforms for a sudden inductive load change from (50Ω+100mH) to (25Ω+50mH) are shown in Fig. 15 (a). The number of levels decreases as the modulation index (M_a)

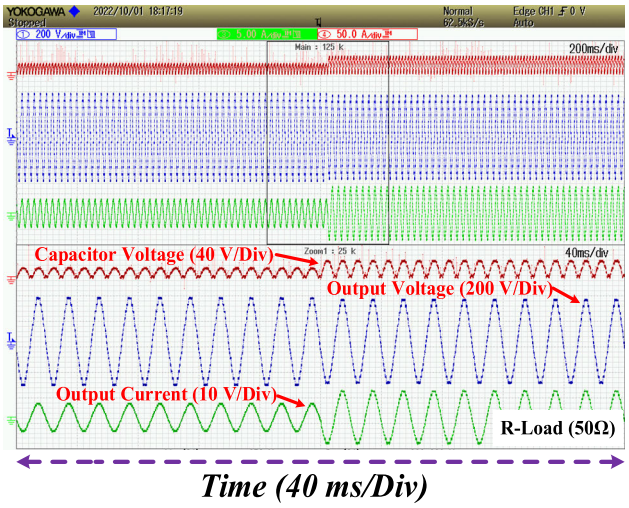


FIGURE 13. Output voltage (V_O), output current (I_O) and capacitor voltage (V_C) for R-load.

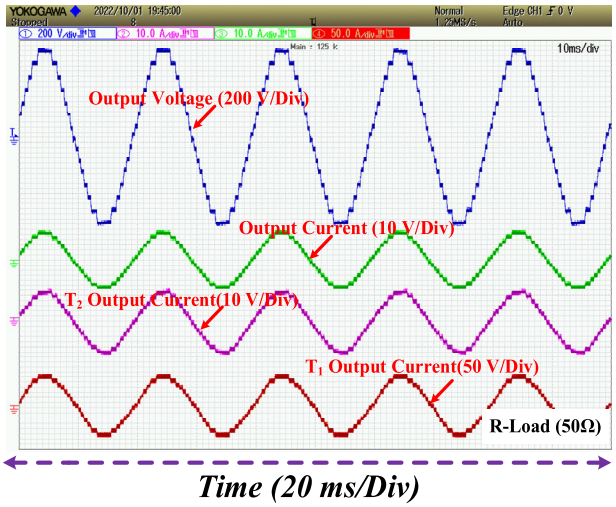
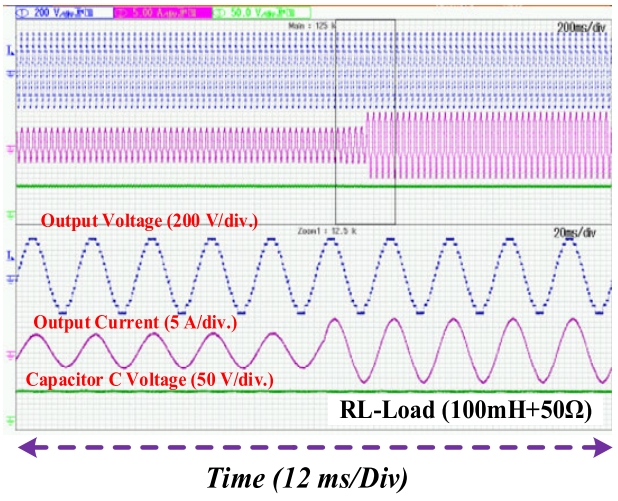
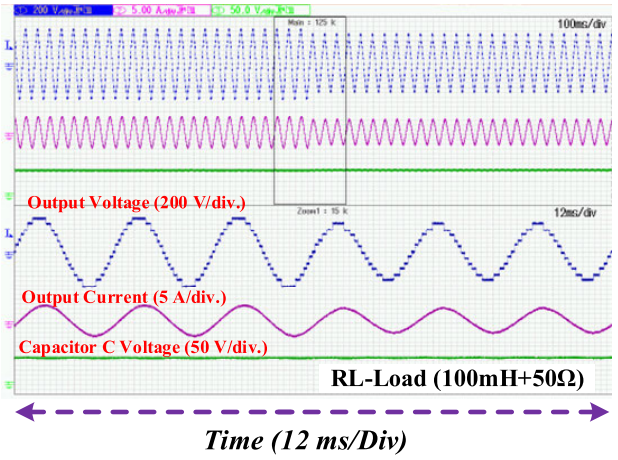


FIGURE 14. Output voltage (V_O), output current (I_O), transformer T_1) current and transformer (T_2) current for R-load.



(a)



(b)

FIGURE 15. Output voltage (V_O), output current (I_O), and voltage across capacitor C for (a) dynamic change of RL-load and (b) change in Modulation Index (Ma).

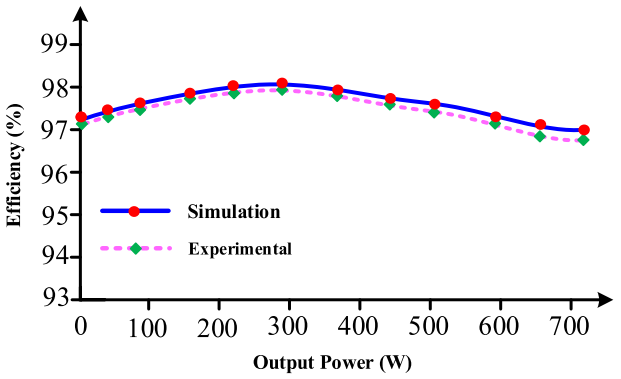


FIGURE 16. Simulation and experimental efficiency.

is decreased. The number of output levels changes from 15 to 13 as the M_a is changed from (1 to 0.8) as shown in Fig. 15 (b). It is observed that as the load varies, the current magnitude varies as well, but the output voltage levels stay constant in both scenarios.

The SC-MLI efficiency is further analyzed at different loads versus the output power using PLECS software and power quality and energy analyzer as depicted in Fig. 16. The efficiency achieved using PLECS software is relatively high 97.1% at an output power of 700W. While the efficiency of the experimental prototype at 700W is 96.4%. The efficiency for various load conditions and proposed inverter output parameters are calculated and presented in Table 4.

The harmonic spectrum of output voltage and load current of the proposed being operated with voltage gain 7 is illustrated in Fig. 17 (a) and (b). THD values in output voltage and load current are 6.9% and 0.7%, respectively, as shown in Fig. 17 (a) and (b).

The various obtained simulation and experimental results for the proposed SC-MLI for resistive and inductive load are illustrated in Table 4.

TABLE 4. Summary of results.

	R - Load		RL - Load	
	Simulation Results	Experimental Results	Simulation Results	Experimental Results
V_{dc}	*50V*	*50V*	*50V*	*50V*
f_s	*50Hz*	*50Hz*	*50Hz*	*50Hz*
V_{rms}	314.5V	312.9V	315V	314.2V
I_{rms}	3.00A	2.94 A	3.10 A	3.08 A
P_o	*700W*	*700W*	*700W*	*700W*
η	*97.41%*	*96.8%*	*97.1%*	*96.4%*

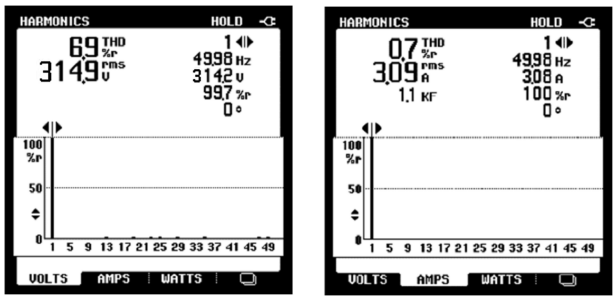


FIGURE 17. Harmonic profile of the (a) 15 level output voltage, and (b) load current (50 Ω, 100 mH).

VII. CONCLUSION

This study proposes a novel multilevel inverter topology. In contrast to existing topologies, the proposed topology has better performance characteristics in terms of the number of switches, capacitor voltage rating for higher voltage gain, self-voltage balancing of capacitor voltage, lower cost, and higher efficiency. A precise comparison investigation has demonstrated the above advantages of the suggested topology. These minimized power loss features of the proposed SC-MLI make it suitable for applications that demand low voltage and higher power ratings such as photovoltaic-based distributed power generation applications. The proposed SC-MLI can sustain voltage across the switched capacitor even during step variations in load demand. The efficiency of the converter for a rated load of 700 W is observed to be 97.1%. Some future works include Optimizing the number of power switches and transformers used to obtain higher levels and the use of SiC devices to minimize the overall losses. Also, the proposed topology will be further extended for three phases to achieve a high-power inverter.

REFERENCES

[1] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," *IEEE Trans. Power Electron*, vol. 31, no. 1, pp. 135–151, Jan. 2016, doi: 10.1109/TPEL.2015.2405012.

[2] K. P. Panda, S. S. Lee, and G. Panda, "Reduced switch cascaded multilevel inverter with new selective harmonic elimination control for standalone renewable energy system," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 7561–7574, Nov. 2019, doi: 10.1109/TIA.2019.2904923.

[3] M. R. J. Oskuee, M. Karimi, S. N. Ravadanegh, and G. B. Gharehpetian, "An innovative scheme of symmetric multilevel voltage source inverter with lower number of circuit devices," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6965–6973, Nov. 2015, doi: 10.1109/TIE.2015.2438059.

[4] S. S. Lee, K.-B. Lee, I. M. Alsofyani, Y. Bak, and J. F. Wong, "Improved switched-capacitor integrated multilevel inverter with a DC source string," *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 7368–7376, Nov. 2019, doi: 10.1109/TIA.2019.2893850.

[5] P. Kakosimos, K. Pavlou, A. Kladas, and S. Manias, "A single-phase nine-level inverter for renewable energy systems employing model predictive control," *Energy Convers. Manag.*, vol. 89, pp. 427–437, Jan. 2015, doi: 10.1016/j.enconman.2014.10.013.

[6] F. Wang and J. Jiang, "A novel static frequency converter based on multilevel cascaded H-bridge used for the startup of synchronous motor in pumped-storage power station," *Energy Convers. Manag.*, vol. 52, no. 5, pp. 2085–2091, May 2011, doi: 10.1016/j.enconman.2010.12.018.

[7] E. Babaei and M. S. Moeinian, "Asymmetric cascaded multilevel inverter with charge balance control of a low resolution symmetric subsystem," *Energy Convers. Manag.*, vol. 51, no. 11, pp. 2272–2278, Nov. 2010, doi: 10.1016/j.enconman.2010.03.022.

[8] N. Sandeep, "A 13-level switched-capacitor-based boosting inverter," *IEEE Trans. Circuits Syst. II: Exp. Briefs*, vol. 68, no. 3, pp. 998–1002, Mar. 2021, doi: 10.1109/TCSII.2020.3017338.

[9] R. S. Alishah, S. H. Hosseini, E. Babaei, and M. Sabahi, "A new general multilevel converter topology based on cascaded connection of submultilevel units with reduced switching components, DC sources, and blocked voltage by switches," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7157–7164, Nov. 2016, doi: 10.1109/TIE.2016.2592460.

[10] J. Sathik Mohamed Ali, R. Shalchi Alishah, N. Sandeep, S. H. Hosseini, E. Babaei, K. Vijayakumar, and U. R. Yaragatti, "A new generalized multilevel converter topology based on cascaded connection of basic units," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 4, pp. 2498–2512, Dec. 2019, doi: 10.1109/JESTPE.2018.2885209.

[11] U. Mustafa, M. S. B. Arif, R. Kennel, and M. Abdelrahem, "Asymmetrical eleven-level inverter topology with reduced power semiconductor switches, total standing voltage and cost factor," *IET Power Electron*, vol. 15, no. 5, pp. 395–411, 2022, doi: 10.1049/pel2.12238.

[12] K. P. Panda, P. R. Bana, and G. Panda, "A reduced device count single DC hybrid switched-capacitor self-balanced inverter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 3, pp. 978–982, Mar. 2021, doi: 10.1109/TCSII.2020.3018333.

[13] T. Roy and P. K. Sadhu, "A step-up multilevel inverter topology using novel switched capacitor converters with reduced components," *IEEE Trans. Ind. Electron.*, vol. 68, no. 1, pp. 236–247, Jan. 2021, doi: 10.1109/TIE.2020.2965458.

[14] Y. Ye, G. Zhang, X. Wang, Y. Yi, and K. W. E. Cheng, "Self-balanced switched-capacitor thirteen-level inverters with reduced capacitors count," *IEEE Trans. Ind. Electron.*, vol. 69, no. 1, pp. 1070–1076, Jan. 2022, doi: 10.1109/TIE.2021.3050378.

[15] K.-M. Kim, J.-K. Han, and G.-W. Moon, "A high step-up switched-capacitor 13-level inverter with reduced number of switches," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2505–2509, Mar. 2021, doi: 10.1109/TPEL.2020.3012282.

[16] M. Ali, M. Tayyab, A. Sarwar, and M. Khalid, "A low switch count 13-level switched-capacitor inverter with hexad voltage-boosting for renewable energy integration," *IEEE Access*, vol. 11, pp. 36300–36308, 2023, doi: 10.1109/ACCESS.2023.3265467.

[17] M. Ali, M. Zaid, A. Sarwar, A. Iqbal, M. I. Hossain, and M. Khalid, "A common-ground seven-level boosting inverter (CG7LI) for solar-PV application," in *Proc. IEEE Int. Conf. Energy Technol. Future Grids (ETFG)*, Dec. 2023, pp. 1–5, doi: 10.1109/etfg55873.2023.10408272.

[18] M. Chen, Y. Yang, P. C. Loh, and F. Blaabjerg, "A single-source nine-level boost inverter with a low switch count," *IEEE Trans. Ind. Electron.*, vol. 69, no. 3, pp. 2644–2658, Mar. 2022, doi: 10.1109/TIE.2021.3065609.

[19] E. Samadaei, M. Kaviani, and K. Bertilsson, "A 13-levels module (K-type) with two DC sources for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5186–5196, Jul. 2019, doi: 10.1109/TIE.2018.2868325.

[20] J. Zeng, W. Lin, D. Cen, and J. Liu, "Novel K-type multilevel inverter with reduced components and self-balance," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 4343–4354, Dec. 2020, doi: 10.1109/JESTPE.2019.2939562.

[21] D. Upadhyay, M. Ali, M. Tariq, S. A. Khan, B. Alamri, and A. Alahmadi, "Thirteen-level UXE-type inverter with 12-band hysteresis current control employing PSO based PI controller," *IEEE Access*, vol. 10, pp. 29890–29902, 2022, doi: 10.1109/ACCESS.2022.3146355.
[22] S. Laali and R. Nasiri-Zarandi, "New cascaded multilevel inverter with series connection of novel capacitor based basic units," *IET Power Electron.*, vol. 16, no. 11, pp. 1796–1813, 2023, doi: 10.1049/pel2.12502.
[23] S. T. Meraj, M. S. A. Rahman, N. Z. Yahaya, P. J. Ker, T. M. Hossain, M. S. H. Lipu, K. M. Muttaqi, and M. A. Hannan, "A pencil shaped 9-level multilevel inverter with voltage boosting ability: Configuration and experimental investigation," *IEEE Access*, vol. 10, pp. 111310–111321, 2022, doi: 10.1109/ACCESS.2022.3194950.
[24] M. Sarebanzadeh, M. A. Hosseinzadeh, C. Garcia, E. Babaei, M. Hosseinpour, A. Seifi, and J. Rodriguez, "A 15-level switched-capacitor multilevel inverter structure with self-balancing capacitor," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 3, pp. 1477–1481, Mar. 2022, doi: 10.1109/TCSII.2021.3123115.
[25] P. R. Bana, K. P. Panda, S. Padmanaban, L. Mihet-Popa, G. Panda, and J. Wu, "Closed-loop control and performance evaluation of reduced part count multilevel inverter interfacing grid-connected PV system," *IEEE Access*, vol. 8, pp. 75691–75701, 2020, doi: 10.1109/ACCESS.2020.2987620.
[26] C. Dhanamjayulu, S. Padmanaban, J. B. Holm-Nielsen, and F. Blaabjerg, "Design and implementation of a single-phase 15-level inverter with reduced components for solar PV applications," *IEEE Access*, vol. 9, pp. 581–594, 2021, doi: 10.1109/ACCESS.2020.3046477.
[27] R. Samanbakhsh, F. M. Ibanez, P. Koohi, and F. Martin, "A new asymmetric cascaded multilevel converter topology with reduced voltage stress and number of switches," *IEEE Access*, vol. 9, pp. 92276–92287, 2021, doi: 10.1109/ACCESS.2021.3092691.
[28] V. Anand and V. Singh, "A 13-level switched-capacitor multilevel inverter with single DC source," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 2, pp. 1575–1586, Apr. 2022, doi: 10.1109/JESTPE.2021.3077604.
[29] M. R. Banaei, H. Khounjahan, and E. Salary, "Single-source cascaded transformers multilevel inverter with reduced number of switches," *IET Power Electron.*, vol. 5, no. 9, pp. 1748–1753, Nov. 2012.
[30] A. J. P. Nascimento, B. F. de Menezes, S. J. de Mesquita, K. R. Costa, F. L. Tofoli, S. Daher, and F. L. M. Antunes, "Bidirectional isolated asymmetrical multilevel inverter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 1, pp. 151–155, Jan. 2023, doi: 10.1109/TCSII.2022.3201601.
[31] O. Lopez-Santos, C. A. Jacanamejoy-Jamioy, D. F. Salazar-D'Antonio, J. R. Corredor-Ramírez, G. Garcia, and L. Martinez-Salamero, "A single-phase transformer-based cascaded asymmetric multilevel inverter with balanced power distribution," *IEEE Access*, vol. 7, pp. 98182–98196, 2019, doi: 10.1109/ACCESS.2019.2930230.
[32] A. Dekka, O. Beik, and M. Narimani, "Modulation and voltage balancing of a five-level series-connected multilevel inverter with reduced isolated direct current sources," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8219–8230, Oct. 2020, doi: 10.1109/TIE.2019.2949537.
[33] A. Farakhor, R. R. Ahrabi, H. Ardi, and S. N. Ravadanegh, "Symmetric and asymmetric transformer based cascaded multilevel inverter with minimum number of components," *IET Power Electron.*, vol. 8, no. 6, pp. 1052–1060, Jun. 2015, doi: 10.1049/iet-pel.2014.0378.

AHMED AWADELSEED (Student Member, IEEE) received the B.Sc. degree in electrical engineering from Kordofan University, Sudan, and the M.Sc. degree in power electronics and drives from the National Institute of Technology (NIT) Warangal, India. He is currently pursuing the Ph.D. degree with the Department of Automatic Control of Electric Drives, Gdańsk University of Technology. He was a Research Assistant with the Department of Electrical Engineering, Qatar University, Doha, Qatar. His research interests include step-up power electronics converters (dc/ac and dc/dc), multilevel inverter topologies, and their control. He is serving as a Regular Reviewer for various journals of IEEE, Wiley, and IET.

ARKADIUSZ LEWICKI (Senior Member, IEEE) received the Ph.D. and D.Sc. degrees in electrical drives from the Faculty of Electrical Engineering, Gdańsk University of Technology, Gdańsk, Poland, in 2003 and 2013, respectively. He is currently with the Institute of Automatic Control of Electric Drives, Gdańsk University of Technology. His scientific activities are concentrated on microprocessor control of converters, multilevel converters, pulse-width modulation techniques, and nonlinear control of drive systems.

ATIF IQBAL (Fellow, IEEE) received the B.Sc. (Hons.) and M.Sc. degrees in engineering (power system and drives) from Aligarh Muslim University (AMU), Aligarh, India, in 1991 and 1996, respectively, the Ph.D. degree from Liverpool John Moores University, Liverpool, U.K., in 2006, and the D.Sc. degree (Habilitation) in control, informatics, and electrical engineering from Gdańsk University of Technology, in 2019. He has been employed as a Lecturer with the Department of Electrical Engineering, AMU, since 1991, where he was a Full Professor until August 2016. He is currently a Full Professor with the Department of Electrical Engineering, Qatar University, Doha, Qatar, and a Former Full Professor with the Department of Electrical Engineering, AMU. He has published widely in international journals and conferences his research findings related to *Journal of Power Electronics*, *Variable Speed Drives*, and *Renewable Energy Sources*. He has authored/co-authored more than 450 research articles and four books and several chapters in edited books. He has supervised several large research and development projects worth more than multi-million USD. He has supervised and co-supervised several Ph.D. students. His principal area of research interests include smart grid, complex energy transition, active distribution networks, electric vehicles drivetrain, sustainable development and energy security, distributed energy generation, and multiphase motor drive systems. He is a fellow of IET in U.K. and IE in India. He was a recipient of the Outstanding Faculty Merit Award academic year 2014–2015 and the Research Excellence Awards 2015 and 2019 from Qatar University. He is the Vice-Chair of the IEEE Qatar Section. He was a recipient of the Maulana Tufail Ahmad Gold Medal for standing first at the B.Sc. Engg. (Electrical) Exams in 1991 from AMU. He has received several Best Research Papers Awards, e.g., IEEE ICIT-2013, IET-SEISCON-2013, SIGMA 2018, IEEE CENCON 2019, IEEE ICIOT 2020, ICSTEESD-20, and Springer ICRP 2020. He is an Associate Editor of IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and IEEE ACCESS, the Editor-in-Chief of *i-manager's Journal on Electrical Engineering*, a Former Associate Editor of IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, the Former Guest Associate Editor of IEEE TRANSACTIONS ON POWER ELECTRONICS.